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ECEN 220

Lab #8

11/5/2013

**MOD4 state graph, truth table, k-maps, and equations**

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**MOD4 Verilog Code**

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| module MOD4(q, inc, reset, clk);    output[1:0] q;  input inc, reset, clk;  wire[1:0] n;  assign n[1] = (~inc & q[1]) | (q[1] & ~q[0]) | (inc & ~q[1] & q[0]);  assign n[0] = (~inc & q[0]) | (inc & ~q[0]);    FF\_DC ff1(q[1], clk, reset, n[1]);  FF\_DC ff0(q[0], clk, reset, n[0]);  endmodule |

**MOD4 TCL file**

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| --- |
| wave add / -radix hex  isim force add clk 0 -time 0 -value 1 -time 5ns -repeat 10ns  isim force add inc 0 -time 0 -value 1 -time 12ns -value 0 -time 27ns -value 1 -time 40ns  isim force add reset 1 -time 0 -value 0 -time 18ns  run 80ns |

**MOD4 simulation waveform**

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**Programmable timer Verilog code**

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| module timerbench(zero, tp, clk, reset);  output zero, tp;  input clk, reset;  prog\_timer timer1(clk, reset, 1'b1, 24'd250000, counter, zero, tp);  endmodule |

**Programmable timer UCF file**

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| --- |
| NET clk LOC = "B8"; # Bank = 0, Pin name = IP\_L13P\_0/GCLK8, Type = GCLK, Sch name = GCLK0  NET reset LOC = "H13"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = BTN3  NET zero LOC = "B4"; # Bank = 0, Pin name = IO\_L24N\_0, Type = I/O, Sch name = R-IO1  NET tp LOC = "A4"; # Bank = 0, Pin name = IO\_L24P\_0, Type = I/O, Sch name = R-IO2 |

**Programmable timer screenshot**

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**4x7 Segment Controller Verilog code**

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| module segcontroller47(Ca, Cb, Cc, Cd, Ce, Cf, Cg,  AN0, AN1, AN2, AN3, DP, tp, zero,  Digit1, Digit2, Digit3, Digit4, System\_Clock,  Reset, Dp0, Dp1, Dp2, Dp3);    output Ca, Cb, Cc, Cd, Ce, Cf, Cg, AN0, AN1, AN2, AN3, DP, tp, zero;  input[3:0] Digit1, Digit2, Digit3, Digit4;  input System\_Clock, Reset, Dp0, Dp1, Dp2, Dp3;  wire[3:0] temp1;  wire[1:0] temp3;  wire[3:0] temp4;  wire[23:0] counter;        //mux164(result, sel, din3, din2, din1, din0);  mux164 Mm1(temp1, temp3, Digit4, Digit3, Digit2, Digit1);    //MOD4(q, inc, reset, clk);  MOD4 mod41(temp3, zero, Reset, System\_Clock);    //prog\_timer (clk, reset, clken, load\_number, counter, zero, tp);  prog\_timer t1(System\_Clock, Reset, 1'b1, 24'd250000, counter, zero, tp);    //decorder24(q,a);  decorder24 d1(temp4, temp3);    not(AN0, temp4[3]);  not(AN1, temp4[2]);  not(AN2, temp4[1]);  not(AN3, temp4[0]);      //Mux41(Q,A,B,C,D,Sel0,Sel1);  Mmux41 mux1(DP, ~Dp3, ~Dp2, ~Dp1, ~Dp0, temp3[0], temp3[1]);      ssdecorder sd1(.a(Ca), .b(Cb), .c(Cc), .d(Cd), .e(Ce), .f(Cf), .g(Cg), .N0(temp1[0]), .N1(temp1[1]), .N2(temp1[2]), .N3(temp1[3]));  endmodule |

**TestBench Verilog code**

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| --- |
| module test\_seg47(Ca, Cb, Cc, Cd, Ce, Cf, Cg,  AN0, AN1, AN2, AN3, DP, tp, zero,  System\_Clock,  Reset, Dp0, Dp1, Dp2, Dp3);    output Ca, Cb, Cc, Cd, Ce, Cf, Cg, AN0, AN1, AN2, AN3, DP, tp, zero;  input System\_Clock, Reset, Dp0, Dp1, Dp2, Dp3;    segcontroller47 seg1(Ca, Cb, Cc, Cd, Ce, Cf, Cg,  AN0, AN1, AN2, AN3, DP, tp, zero,  4'b0001, 4'b1010, 4'b1011, 4'b1000, System\_Clock,  Reset, Dp0, Dp1, Dp2, Dp3);  endmodule |

**TestBench UCF file**

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| --- |
| NET System\_Clock LOC = "B8"; # Bank = 0, Pin name = IP\_L13P\_0/GCLK8, Type = GCLK, Sch name = GCLK0  NET Dp0 LOC = "G18"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW0  NET Dp1 LOC = "H18"; # Bank = 1, Pin name = IP/VREF\_1, Type = VREF, Sch name = SW1  NET Dp2 LOC = "K18"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW2  NET Dp3 LOC = "K17"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW3  NET Reset LOC = "H13"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = BTN3  NET Ca LOC = "L18"; # Bank = 1, Pin name = IO\_L10P\_1, Type = I/O, Sch name = CA  NET Cb LOC = "F18"; # Bank = 1, Pin name = IO\_L19P\_1, Type = I/O, Sch name = CB  NET Cc LOC = "D17"; # Bank = 1, Pin name = IO\_L23P\_1/HDC, Type = DUAL, Sch name = CC  NET Cd LOC = "D16"; # Bank = 1, Pin name = IO\_L23N\_1/LDC0, Type = DUAL, Sch name = CD  NET Ce LOC = "G14"; # Bank = 1, Pin name = IO\_L20P\_1, Type = I/O, Sch name = CE  NET Cf LOC = "J17"; # Bank = 1, Pin name = IO\_L13P\_1/A6/RHCLK4/IRDY1, Type = RHCLK/DUAL, Sch name = CF  NET Cg LOC = "H14"; # Bank = 1, Pin name = IO\_L17P\_1, Type = I/O, Sch name = CG  NET DP LOC = "C17"; # Bank = 1, Pin name = IO\_L24N\_1/LDC2, Type = DUAL, Sch name = DP  NET AN0 LOC = "F17"; # Bank = 1, Pin name = IO\_L19N\_1, Type = I/O, Sch name = AN0  NET AN1 LOC = "H17"; # Bank = 1, Pin name = IO\_L16N\_1/A0, Type = DUAL, Sch name = AN1  NET AN2 LOC = "C18"; # Bank = 1, Pin name = IO\_L24P\_1/LDC1, Type = DUAL, Sch name = AN2  NET AN3 LOC = "F15"; # Bank = 1, Pin name = IO\_L21P\_1, Type = I/O, Sch name = AN3 |

**Anomalies**

This lab took really long. Creating test bench is still giving me a hard time. Combining many Verilog design wasn’t easy because especially for MUX, it’s easy to mix up the order of select inputs. After several hours of trying to debug my code, I found that I ORed with + sign instead of | sign. Thanks TAs. You made me be able to pass-off !