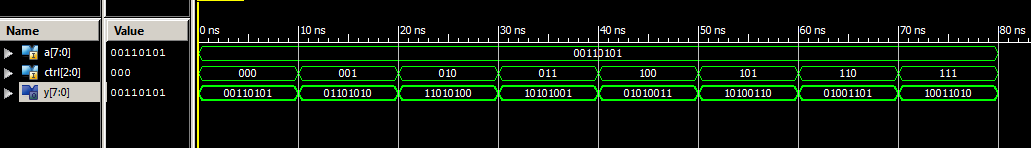
4.6

|  |
| --- |
| library ieee;  use ieee.std\_logic\_1164.all;  entity left\_shift is  port(  a: in std\_logic\_vector(7 downto 0);  ctrl: in std\_logic\_vector(2 downto 0);  y: out std\_logic\_vector(7 downto 0)  );  end left\_shift;  architecture shift\_arch of left\_shift is  begin  y <= a when(ctrl="000") else  a(6)&a(5)&a(4)&a(3)&a(2)&a(1)&a(0)&a(7) when(ctrl="001") else  a(5)&a(4)&a(3)&a(2)&a(1)&a(0)&a(7)&a(6) when(ctrl="010") else  a(4)&a(3)&a(2)&a(1)&a(0)&a(7)&a(6)&a(5) when(ctrl="011") else  a(3)&a(2)&a(1)&a(0)&a(7)&a(6)&a(5)&a(4) when(ctrl="100") else  a(2)&a(1)&a(0)&a(7)&a(6)&a(5)&a(4)&a(3) when(ctrl="101") else  a(1)&a(0)&a(7)&a(6)&a(5)&a(4)&a(3)&a(2) when(ctrl="110") else  a(0)&a(7)&a(6)&a(5)&a(4)&a(3)&a(2)&a(1);  end shift\_arch; |



5.3

|  |
| --- |
| architecture if\_arch of decoder4 is  begin  process(s,en)  begin  if(s="00" and en="1") then  x <= "0001";  elsif(s="01" and en="1") then  x <= "0010";  elsif(s="10" and en="1") then  x <= "0100";  elsif(s="11" and en="1") then  x <= "1000";  else  x <= "0000";  end if;  end process;  end if\_arch; |

5.4

|  |
| --- |
| architecture case\_arch of decoder4 is  signal ens <= en&s;  begin  process(ens)  begin  case ens is  when "000"|"001"|"010"|"011" =>  x <= "0000";  when "100" =>  x <= "0001";  when "101" =>  x <= "0010";  when "110" =>  x <= "0100";  when others =>  x <= "1000";  end case;  end process;  end case\_arch; |