13.1

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| --- |
| library ieee;  use ieee.std\_logic\_1164.all;  entity thousand\_counter is  port(  clk, reset: in std\_logic;  en: in std\_logic;  q\_hundred, q\_ten, q\_one: out std\_logic\_vector(3 downto 0);  p1000: out std\_logic  );  end thousand\_counter;  architecture thou\_arch of thousand\_counter is  component dec\_counter  port(  clk, reset: in std\_logic;  en: in std\_logic;  q: out std\_logic\_vector(3 downto 0);  pulse: out std\_logic  );  end component;  signal p\_one, p\_ten, p\_hundred: std\_logic;  begin  one\_digit: dec\_counter  port map(clk=>clk, reset=>reset, en=>en, pulse=>p\_one, q=>q\_one);  ten\_digit: dec\_counter  port map(clk=>clk, reset=>reset, en=>p\_one, pulse=>p\_ten, q=>q\_ten);  hundred\_digit: dec\_counter  port map(clk=>clk, reset=>reset, en=>p\_ten, pulse=>p\_hundred, q=>q\_hundred);  p1000 <= p\_one and p\_ten and p\_hundred;  end thou\_arch; |

13.2

|  |
| --- |
| library ieee;  use ieee.std\_logic\_1164.all;  entity thousand\_mod is  port(  clk, reset: in std\_logic;  en: in std\_logic;  q\_hundred, q\_ten, q\_one: out std\_logic\_vector(3 downto 0);  p1000: out std\_logic  );  end thousand\_mod;  architecture generic\_arch of thousand\_mod is  component mod\_n\_counter  generic(  N: natural;  WIDTH: natural  );  port(  clk, reset: in std\_logic;  en: in std\_logic;  q: out std\_logic\_vector(WIDTH-1 downto 0);  pulse: out std\_logic  );  end component;    signal p\_one, p\_ten, p\_hundred: std\_logic;  begin  one\_digit: mod\_n\_counter  generic map(N=>10, WIDTH=>4)  port map(clk=>clk, reset=>reset, en=>en, pulse=>p\_one, q=>q\_one);  ten\_digit: mod\_n\_counter  generic map(N=>10, WIDTH=>4)  port map(clk=>clk, reset=>reset, en=>p\_one, pulse=>p\_ten, q=>q\_ten);  hundred\_digit: mod\_n\_counter  generic map(N=>10, WIDTH=>4)  port map(clk=>clk, reset=>reset, en=>p\_ten, pulse=>p\_hundred, q=>q\_hundred);  p1000 <= p\_one and p\_ten and p\_hundred;  end generic\_arch; |

3.

|  |
| --- |
| library ieee;  use ieee.std\_logic\_1164.all;  entity thousand\_93\_counter is  port(  clk, reset: in std\_logic;  en: in std\_logic;  q\_hundred, q\_ten, q\_one: out std\_logic\_vector(3 downto 0);  p1000: out std\_logic  );  end thousand\_93\_counter;  architecture vhdl\_93\_arch of thousand\_93\_counter is  signal p\_one, p\_ten, p\_hundred: std\_logic;  begin  one\_digit: entity work.dec\_counter(up\_arch)  port map(clk=>clk, reset=>reset, en=>en, pulse=>p\_one, q=>q\_one);  ten\_digit: entity work.dec\_counter(up\_arch)  port map(clk=>clk, reset=>reset, en=>p\_one, pulse=>p\_ten, q=>q\_ten);  hundred\_digit: entity work.dec\_counter(up\_arch)  port map(clk=>clk, reset=>reset, en=>p\_ten, pulse=>p\_hundred, q=>q\_hundred);  p1000 <= p\_one and p\_ten and p\_hundred;  end vhdl\_93\_arch; |