Question: How many bits are available in a single device?

* 8192\*1024\*16 = 134217728 bits = 128Mbit

Question: How many bits are in each word of this device?

* 16 bits

Question: What is the purpose of the Bus Conﬁguration Register (BCR)?

* The bus configuration register defines how the CellularRAM device interacts with the system memory bus.

Question: What is the purpose of the LB and UB signals?

* LB signal enables lower byte(DQ[7:0]) and UB signal enables upper byte(DQ[15:8]).

Question: How long does it take to complete the “Power-Up Initialization” of this device? How many 50 MHz clock cycles is this power-up initialization?

* t-powerup is greater than or equal to 150us. 7500 clock cycles.

Question: What value should be applied on the CE# signal during power-up initialization?

* CE# should remain HIGH during the initialization period.

Question: Summarize the difference between the Asynchronous Read Mode and the Page Mode Read operation.

* In page-mode capable products, an initial asynchronous read access is performed, then adjacent addresses can be read quickly by simply changing the low order address.

Question: Determine the values of CE, WE, OE, ADV, LB, and UB needed to perform a read in Asynchronous mode on both the upper and lower bytes.

* CE,OW,LB,UB = LOW.
* WE = HIGH.
* ADV = LOW

Question: What is the minimum read cycle time (TRC) for the device used on our board?

* 70ns

Question: How many 50 MHz clock cycles will be needed to complete a read operation on the Nexys2 FPGA board?

* 4 cycles

Question: What is the purpose of the parameter TAA? This parameter happens to be the same as TRC and they have the same value. Why is TAA in the “maximum” column and TRC is in the “minimum” column?

* t-AA = Address access time
* t-AA is the maximum time that it will take for the data to be valid after changing the address. It is the maximum because it is a hard guarantee on the most time it will take. t-RC is the minimum read time. It indicates that you need at least this much time to do a read.

Question: What is the difference between the timing parameter tOE and the timing parameter tOLZ?

* t-OE = Output enable to valid output, T-OLZ = Output enable to Low-Z output

Question: In page mode, determine the maximum time it will take for the data to be available once the address has changed (TAA in Figure 7)?

* 70ns

Question: In page mode, determine the maximum time it will take for the second piece of data to be available once the address has changed (TAPA in Figure 7)?

* 20ns

Question: Determine the values of CE, WE, OE, ADV, LB, and UB needed to perform a write in Asynchronous mode on both the upper and lower bytes.

* CE,WE,LB,UB = LOW.
* OE = Don’t care, and WE will override OE.
* ADV = LOW

Question: What is the difference between a WE# controlled write (page 53) and a CE# controlled write (page 51)?

* Input changes when CE changes in CE controlled write while input changes when WE changes in WE controlled write. For WE controlled write, CE has already been asserted. The timing for the write operation commences when the address changes. For the CE controlled write, CE is asserted after the address is set. Timing also commences when the address.

Question: What is the minimum asynchronous write cycle time (TWC) for the device used on our board?

* 70ns

Question: How many clock cycles should the WE# pulse be held low for a write operation (see tWP)?

* t-WP = 45ns. So 3 clock cycles.

Question: How long must the data be present on the memory data pins for a write (see tDW)?

* t-DW = 20ns

Question: How long does the data need to be held after WE is de-asserted (see tDH)?

* t-DH = 0ns