Question: What do you think the display will look like if the digits are sequenced too fast?

* I think it will just show 8 for all of digits because we will perceive like every segment is on.

Question: How long will each digit of the display be driven by the controller if the binary counter used for this sequencing is 15 bits? Assume a 50 MHz input clock.

* 655us

Question: Assuming a 15 bit counter, how long will each digit be blanked?

* 492us

Question: What is the purpose of the COUNTER\_BITS generic used in this design? Why would someone want to change the value of this generic?

* COUNTER\_BITS needs to be modified if we want different timing of time-multiplexing.

Question: What command would you use to create a 100 MHz oscillating clock signal with a 50% duty cycle (i.e., the ‘0’ time and the ‘1’ time of the clock are the same)?

* Isim force add clk 1 –value 0 –time 5ns –repeat 10ns

Question: What time does the testbench simulation end?

* 6062070ns

Question: What is the minimum clock period of your circuit (review the “Post-PAR Static Timing Report” and search for “Minimum period”)?

* 5.204ns

Question: Review the “Map Report” and determine the number of “slices” used by your design.

* 52

Personal Exploration

It was really cool to control leds, switches and buttons in a way that I wanted. I could easily do something different from the lab specification with my built seven\_seg\_display. I just had to create top-level input forming logic and output forming logic.