



# GOWIN Semiconductor Corporation

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UAC2 to I2S Reference Design  
V2R5 Jul 2023

[www.gowinsemi.com](http://www.gowinsemi.com)



Nov to March GMT+0 (UTC)  
April to Oct BST (UTC + 1)

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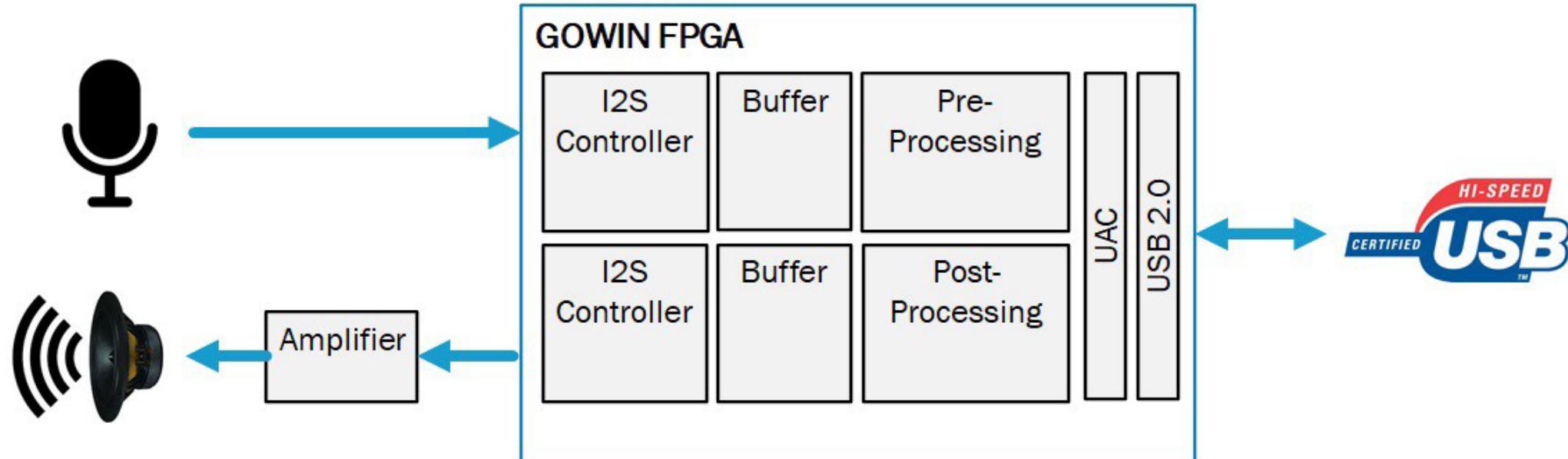
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The GOWIN USB Audio Class 2 (UAC2) reference design integrates the following Soft IP Cores, USB2.0 Soft-PHY & USB2.0 Controller, I2S Receiver and Transmitter, along with basic control logic via USB HID (Human Interface Device).  
Provides a starting point for customers to develop custom USB Audio solutions using GOWIN FPGA.



- Compatible with Native USB Audio Class Drivers on Windows, Linux and MAC OS
- Initializes as a '**GOWIN UAC2**' USB Audio Card
- Uses I2S for audio inputs and outputs
- Provides a loopback mode connecting I2S output to I2S input for comparison tests
- Plays audio from PC through speaker or stream Audio to GPIO.
- Records audio to PC through microphone, or from GPIO.

## USB2.0

- Fully Certified USB2.0 brings the USB-PHY on-chip using a GOWIN Soft-Core IP.

## Data Widths

- Supports 16-bit, 24-bit and 32-bit data.

## Audio Sample Rates

- 768KHz, 705.6KHz, 384KHz, 352.8KHz, 192KHz, 176.4KHz, 128KHz, 96KHz, 88.2KHz, 64KHz, 48KHz, 44.1KHz and 32KHz

## Data Formats – TBC!

- PCM, IIS, DoP & DSD

## Low Latency

- Microsecond (us) type delays – well within the 500us required by UAC2

## Configurable Buffer Size

- The UAC Ref Design Left & Right Audio channels are each allocated a 1024 Byte buffer by default.

## Audio Channels

- So far only the most common scenario has been tested, one I2S output with left & right audio channels.
- Theoretically, users can build USB2.0 to Nx I2S designs.

## Clocking Scheme

- Asynchronous mode, with the clocks derived from an external crystal oscillator.

Website Link

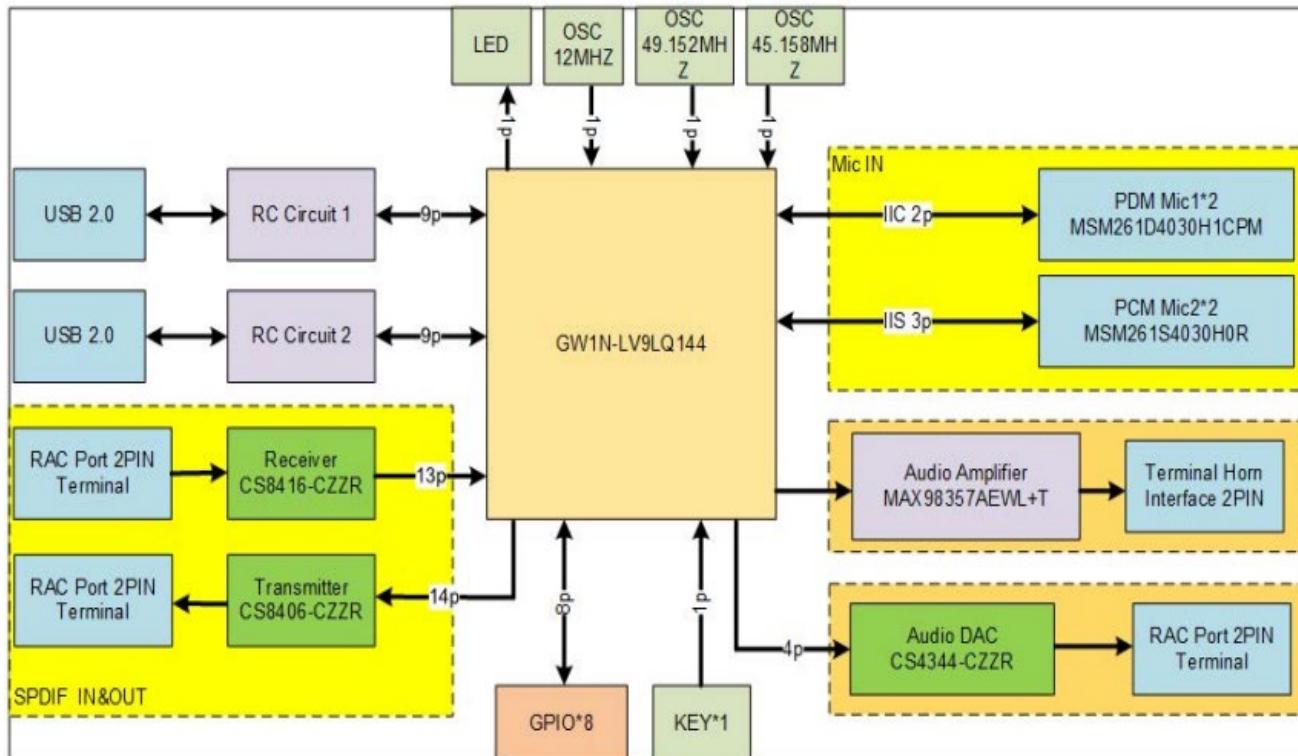
[DK\\_UAC2\\_V2.0](#)

Schematic Link

[DK\\_UAC2\\_GW1N-LV9LQ144C7I6\\_V2.0\\_SCH](#)

User Guide Link

[DK\\_UAC2\\_GW1N-LV9LQ144C7I6\\_V2.0](#)



## GOWIN UAC-2 DVK Features

### Two USB2.0 Interfaces

- USB clock source provided by external 12MHz crystal oscillator

### Audio Clocks

- Provided by 49.152MHz & 45.158MHz external crystal oscillators

### Microphone Left & Right audio input channels x2

- MSM261D4030H1CPM Inter-IC Sound (IIC) PWM inputs
- MSM261S4030H0R I<sup>2</sup>S (IIS) inputs

### SPDIF Interface

- Stereoscopic digital audio input via CS8416-CZZR decoder receiver.
- Stereoscopic digital audio input via CS8406-CZZR encoder transmitter.

### Audio DAC

- Stereoscopic digital audio to analog audio output via CS4344-CZZR DAC

### Audio Amplifier

- PCM digital audio Class-D Amplifier MAX98357AEET driving 5V, 3.2W, 4Ω speaker (not provided)

### Misc

- FPGA Supports JTAG programming.
- Includes GPIO interfaces, LED, and keys to facilitate user test

GOWIN Website UAC2 Link	<a href="#"><u>DK_UAC2_V2.0</u></a>
GOWIN DVK Schematic Link	<a href="#"><u>DK_UAC2_GW1N-LV9LQ144C7I6_V2.0 SCH</u></a>
GOWIN UAC User Guide Link	<a href="#"><u>DK_UAC2_GW1N-LV9LQ144C7I6_V2.0</u></a>
GOWIN UAC2 Demo Guide	UAC2_Demo_SETUP.pdf - included in the database release “UAC2 Docs & Datasheets” folder
GOWIN GW1N Datasheet	<a href="#"><u>DS100 - GW1N Series of FPGA Products Data Sheet</u></a>
GOWIN User Guide	<a href="#"><u>Gowin USB Programming Download Cable User Guide</u></a>
Component Datasheet	<b>MSM261S4030H0R</b> MEMSensing I2S digital output MEMS microphone with Multi-modes
Component Datasheet	<b>MSM261D4030H1CPM</b> MEMSensing PDM digital output MEMS microphone with Multi-modes
Component Datasheet	<b>CS8416-CZZR</b> Cirrus Logic 192KHz Digital Audio Receiver
Component Datasheet	<b>CS8406-CZZ</b> Cirrus Logic 192KHz Digital Audio Transmitter
Component Datasheet	<b>CS4344-CZZR</b> Cirrus Logic 24-Bit, 192KHz Stereo D/A Converter
Component Datasheet	<b>MAX98357AETE+T</b> Analog Devices PCM Class D Amplifier

OneDrive [GOWIN\\_UAC2\\_V2R1\\_21Jul2023](#) Ref Design Download Link

➤ Documentation

- 1) UAC2 to I2S Reference Design User Guide (this document)
  - GOWIN\_UAC2\_V2R5\_Jul\_2023.pdf
- 2) Supporting documentation and device datasheets.
  - UAC2 Docs & Datasheets.zip

➤ Hardware

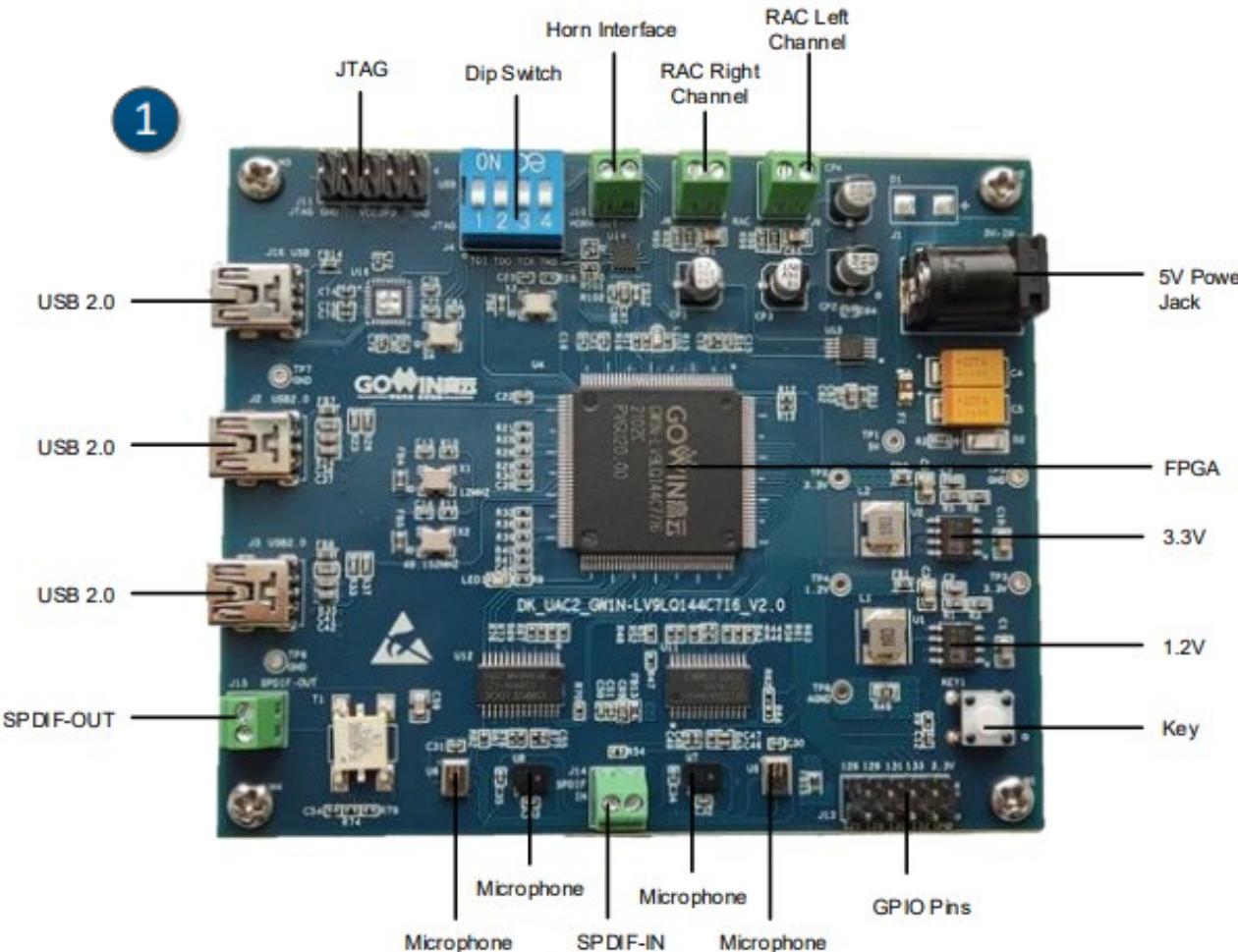
- 3) UAC-2 DVK DK\_UAC2\_GW1N-LV9LQ144C7I6\_V2.0

➤ Firmware

- 4) Project database with partial unencrypted Verilog sources to support user configuration.
  - UAC\_GW1N\_REF\_V2R1\_21Jul2023.zip

➤ Software

- 4) GOWIN EDA Software - Gowin\_V1.9.9Beta\_win.zip
- 5) Vendors default / third-party Audio Streaming Drivers
  - Windows OS PC; MAC PC; Mobile (Android-Linux, AppleOS)



## DK\_UAC2\_V2.0

- (1) Dedicated UAC2.0 Eval Board
  - LittleBee GW1N-LV9LQ144 C7/I6 (Rev-C)
- (2) 5V Power Supply
- (3) USB Min B Data Cable



The table below summarizes the DK\_UAC2\_GW1N-LV9LQ144C7I6\_V2.0 hardware and HDL reference design support. Sample rates and data widths limited by external components.  
The FPGA and HDL design supports the full range of data widths and sample rates.

Input Format	Output Format	Data Widths	Sample Rates	Supported
<b>Latest UAC_GW1N_REF_V2.1_11Apr2023 Reference Design</b>				
GPIO IIS (I2S)	USB2.0	16/24/32-bits	32KHz to 768KHz	YES
USB	GPIO IIS (I2S)	16/24/32-bits	32KHz to 768KHz	YES
MIC IIS (I2S)	USB2.0	16/24/32-bits	32KHz to 96KHz	YES
USB	IIS (I2S) to Audio Amplifier to Speaker or Headset output path.	32-bits	32KHz to 176.4KHz	YES
<b>Future Reference Design (coming soon)</b>				
MIC IIC	USB2.0	16-bit, 32-bit	32KHz to 96KHz	Next Release
MIC IIC	SPDIF L/R	16-bit	32KHz to 96KHz	Next Release
MIC IIS	SPDIF L/R	16-bit	32KHz to 96KHz	Next Release
USB	SPDIF L/R	16-bit	32KHz to 96KHz	Next Release

The UAC\_GW1N\_REF\_V2R1\_27Jun2023 reference design supports the following audio paths.

- 1) Audio Input MEMs Microphone to I2S format to USB2.0.
- 2) Audio Input GPIO Breakout Header (I2S format) to USB2.0.
- 3) Audio Output USB2.0 to I2S format to Audio Amplifier to external Speaker or Headset.
- 4) Audio Output USB2.0 to I2S format to GPIO breakout header.

The HDL reference design supports L&R stereo audio channels and the full range of audio sample rates from 32KHz to 768KHz.

The external Audio DAC and ADC components, however, restrict the overall system performance.

#### Audio Input MEMs Microphone to I2S MSM261S4030H0R Limitations

- 16/24/32-bits, 32KHz to 96KHz sample rates

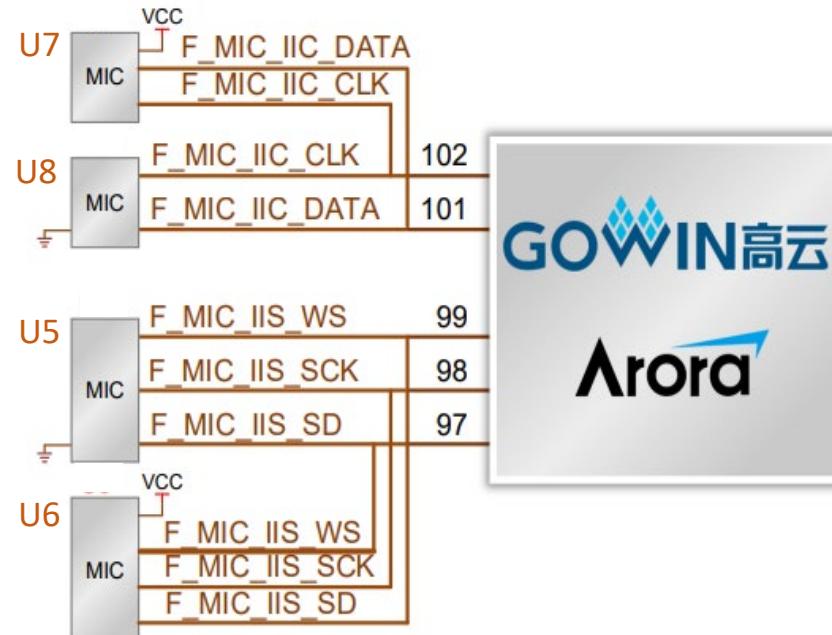
#### Audio Output Amplifier PCM digital audio Class-D MAX98357AETE+T Limitations

- 32-bits, 32KHz to 176.4KHz sample rates

Note GOWIN can provide evaluation hardware that supports other sampling frequencies and bit resolutions if required.

## Microphone Audio Inputs Left & Right Channels [two formats]

- MSM261S4030H0R I<sup>2</sup>S (IIS) inputs
- MSM261D4030H1CPM Inter-IC Sound (IIC) PWM inputs



Ref Design UAC\_GW1N\_REF\_V2.1\_11Apr2023

Supports I<sup>2</sup>S MEMs Microphone input

- MSM261S4030H0R L&R
- U5 & U6 -> I<sup>2</sup>S (IIS)

Does not yet support

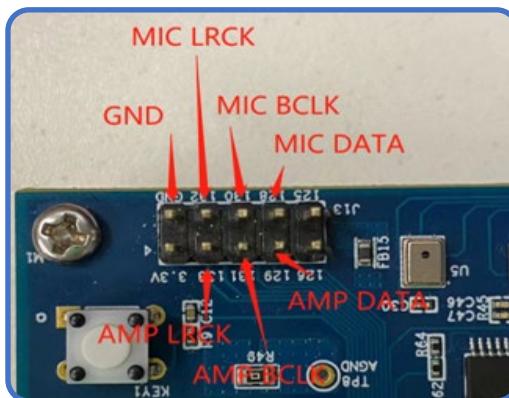
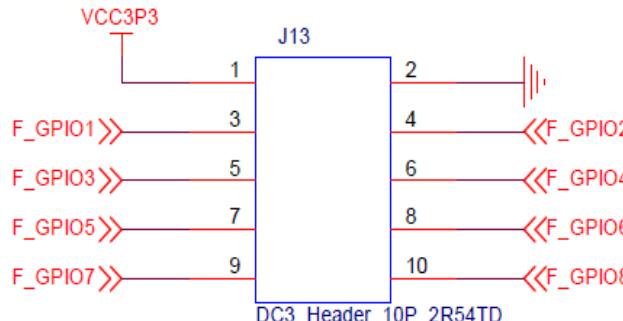
- MSM261D4030H1CPM L&R
- U7 & U8 -> Inter-IC Sound (IIC) PWM inputs

Input Format	Output Format	Data Widths	Sample Rates	Supported
Latest UAC_GW1N_REF_V2R1_27Jun2023 Reference Design				
MIC IIS (I <sup>2</sup> S) (L/R)	USB2.0	16/24/32-bits	32KHz to 96KHz	YES
Future Reference Design (coming soon)				
MIC IIC (L/R)	USB2.0	16-bit, 32-bit	32KHz to 96KHz	Next Release
MIC IIC (L/R)	SPDIF L/R	16-bit	32KHz to 96KHz	Next Release
MIC IIS (L/R)	SPDIF L/R	16-bit	32KHz to 96KHz	Next Release

## GPIO Audio Input / Output

Ref Design UAC\_GW1N\_REF\_V2.1\_11Apr2023

- GPIO I<sup>2</sup>S (IIS) Microphone to USB Input
- USB to GPIO I<sup>2</sup>S (IIS) Amplifier Output



Input Format	Output Format	Data Widths	Sample Rates	Supported
Latest UAC_GW1N_REF_V2R1_27Jun2023 Reference Design				
GPIO IIS (I2S)	USB2.0	16/24/32-bits	32KHz to 768KHz	YES
USB	GPIO IIS (I2S)	16/24/32-bits	32KHz to 768KHz	YES

Header J13	PCB Net	GW1N-9-LQ144	Ref Design HDL Port	Function
USB to GPIO Output Amplifier IIS (L/R)				
Pin-3	F_GPIO1	Pin-133	APM_IIS_LRCK_O	AMP I2S (IIS) Word Select Output -> 0 Left CH, 1 Right CH
Pin-5	F_GPIO3	Pin-131	APM_IIS_BCLK_O	AMP I2S (IIS) Bit Clock Output
Pin-7	F_GPIO5	Pin-129	APM_IIS_DATA_O	AMP I2S (IIS) Data Output
Pin-9	F_GPIO7	Pin-126		
Microphone IIS (L/R) GPIO Input to USB				
Pin-4	F_GPIO2	Pin-132	MIC_IIS_2_IO_LRCK_O	MIC I2S (IIS) Word Select Output -> 0 Left CH, 1 Right CH
Pin-6	F_GPIO4	Pin-130	MIC_IIS_2_IO_BCLK_O	MIC I2S (IIS) Bit Clock Output
Pin-8	F_GPIO6	Pin-128	MIC_IIS_2_IO_DATA_I	MIC I2S (IIS) Data Input
Pin-10	F_GPIO8	Pin-125		

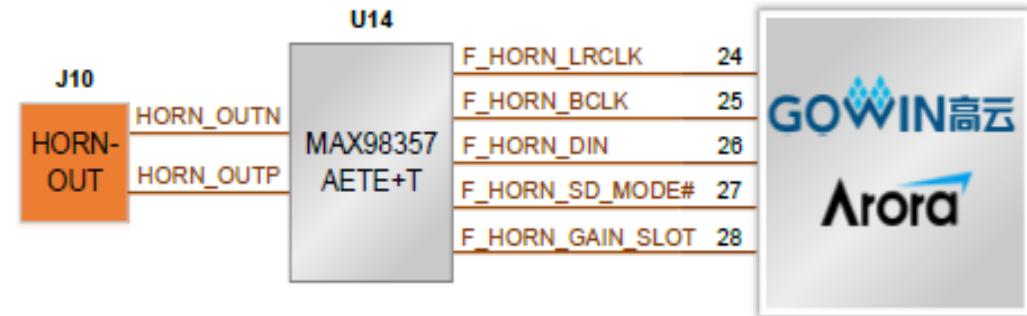
## Audio Amplifier Output

Ref Design UAC\_GW1N\_REF\_V2.1\_11Apr2023

- MAX98357AETE+T to Speaker 4W 4 Ohm or Headphones

The DVK includes a digital audio amplifier output path.

The GOWIN GW1N-LV9LQ144 can output processed PCM audio data to connector J10 via the MAX98357AETE+T Class D amplifier.



Input Format	Output Format	Data Widths	Sample Rates	Supported
Latest UAC_GW1N_REF_V2.1_11Apr2023 Reference Design				
USB	IIS (I2S) to Audio Amplifier to Speaker or Headset output path.	32-bits	32KHz to 176.4KHz	YES

The GOWIN USB2.0 I2S solution is implemented using a GW1N-LV9LQ144 FPGA which incorporates an USB 2.0 Soft-PHY, USB device controller and a UAC link layer.

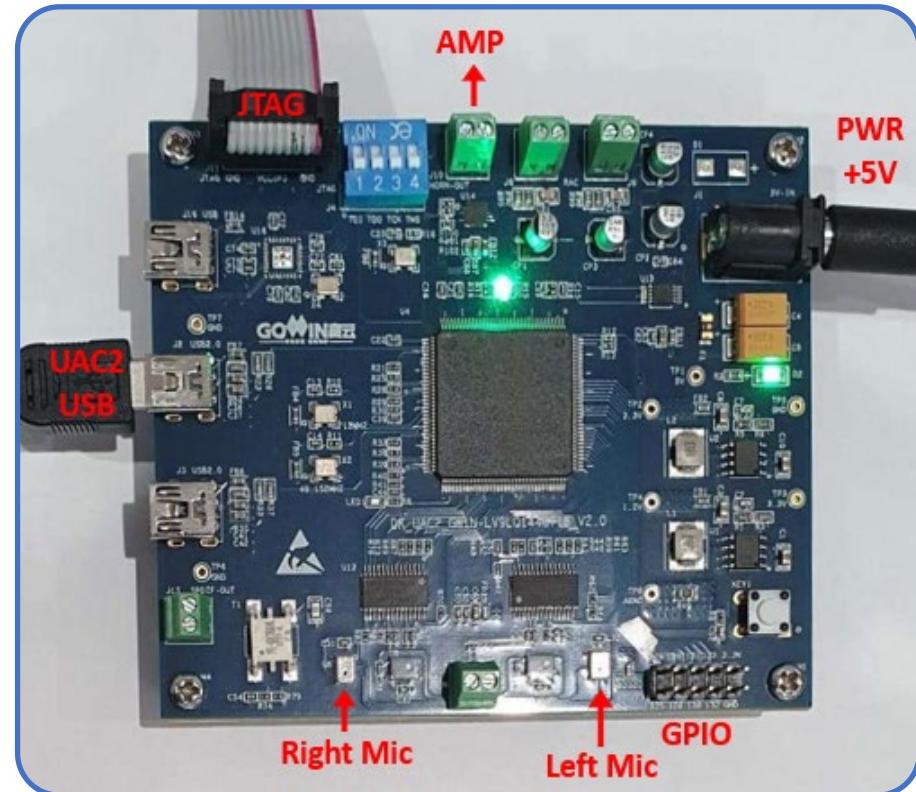
The DK\_UAC2\_GW1N-LV9LQ144C7I6\_V2.0 development board connects to the host (PC) using a standard Type-A 2.0 to Mini-B USB cable.

The development board is powered using an external 5V power supply (provided).

The example (right) shows a small 4-Ohm speaker (not provided) connected to the audio amplifier output J10.

We recommend using Windows 10 for the USB host as most of our testing targeted this OS. However, we have also demonstrated the basic functionality on MacOS & Linux Ubuntu.

You will need to download the appropriate bitstream configuration file to the GOWIN FPGA using the GOWIN USB to JTAG programming cable (provided).



The Programmer software is included in the EDA software version [Gowin V1.9.9Beta win.zip](#)

This FPGA EDA design tool requires a free license [GOWIN License Application Form](#)

The Programmer software can also be downloaded and used standalone [GOWIN EDA Download](#)

Recommended GOWIN EDA Version (Window or Linux) [\*\*Gowin V1.9.9Beta \(Windows\) Standard Edition\*\*](#)

Recommended Programmer (Window or Linux) [\*\*GOWIN Programmer V1.9.9Beta or newer\*\*](#)

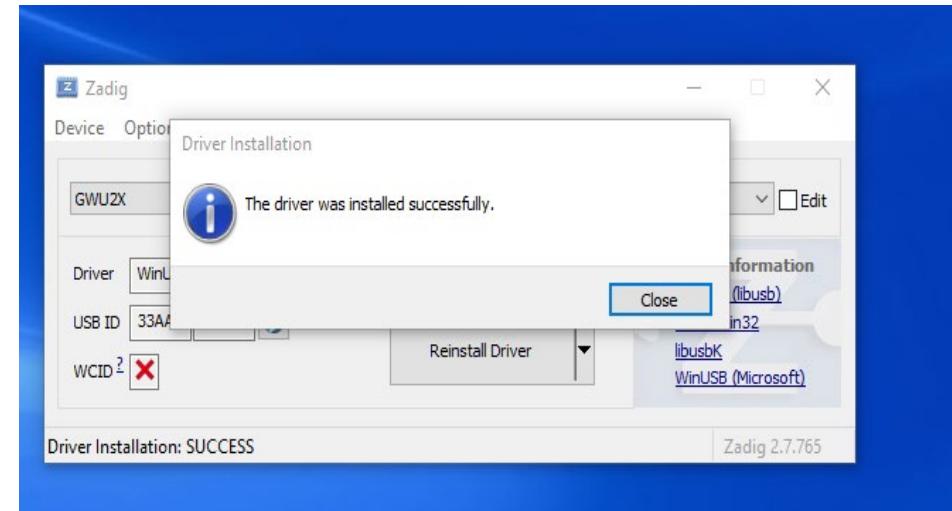
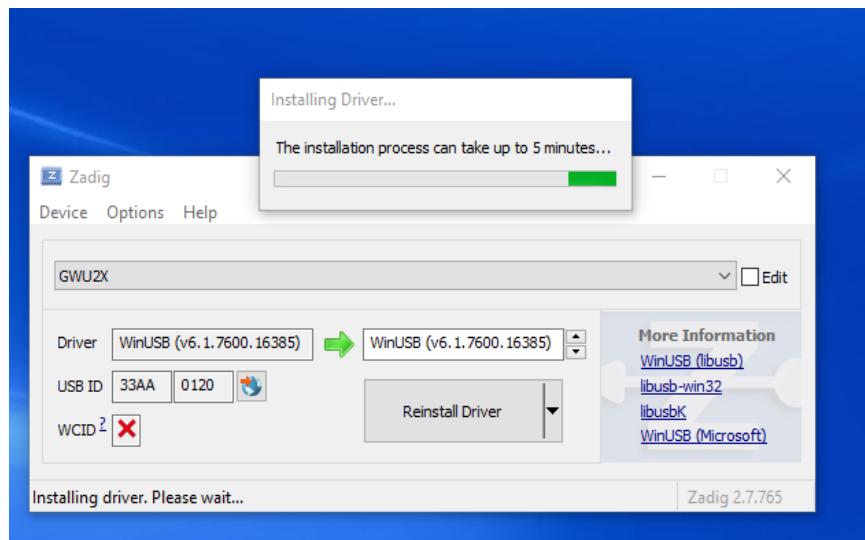
# UAC-2 DVK Demo Setup [3] JTAG Programming Cable

## Ref 3.2 PL-U2X-Cable Driver

Gowin USB Programming Download Cable User Guide UG112-1.1.1E

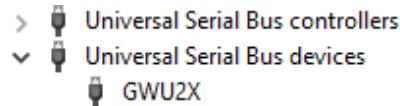
[https://www.gowinsemi.com/upload/database\\_doc/206/document/62da0bfe6d467.pdf](https://www.gowinsemi.com/upload/database_doc/206/document/62da0bfe6d467.pdf)

- 1) Connect the GOWIN GWU2X Programming Cable to your PC via USB.
- 2) Cable drivers (both GWU2X and FTDI) are included in the full GOWIN EDA Tool install.
- 3) The GWU2X driver can also be installed stand-alone as described below.
  - a) Download and save Zadig driver installer:  
<https://github.com/pbatard/libwdi/releases/download/v1.4.1/zadig-2.7.exe>
  - b) Select the GWU2X device, then select the driver to be installed as WinUSB



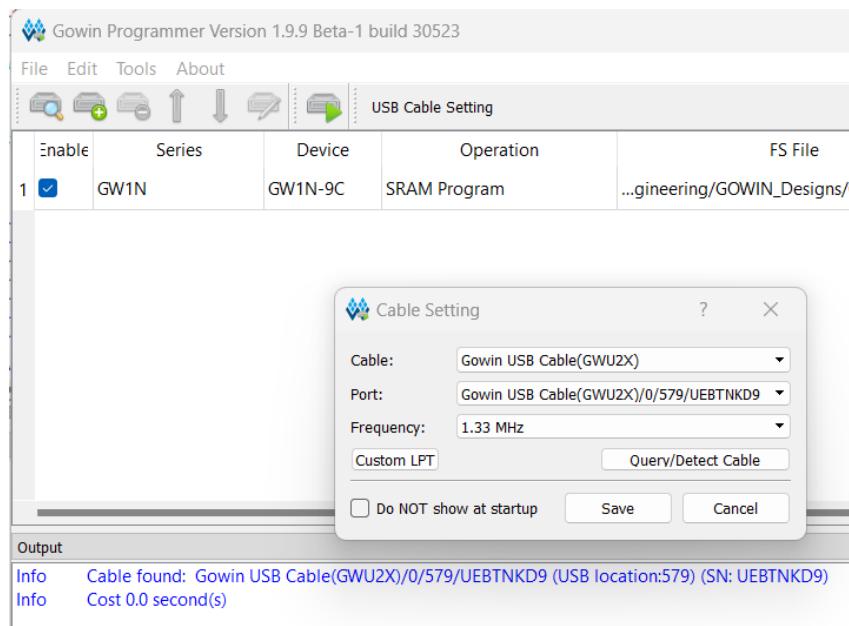
- ① Download Cable
- ② Flat Cable
- ③ Connection Cable

Once the drive is successfully installed,  
confirm the GWU2X hardware is detected in the Windows Device Manager.



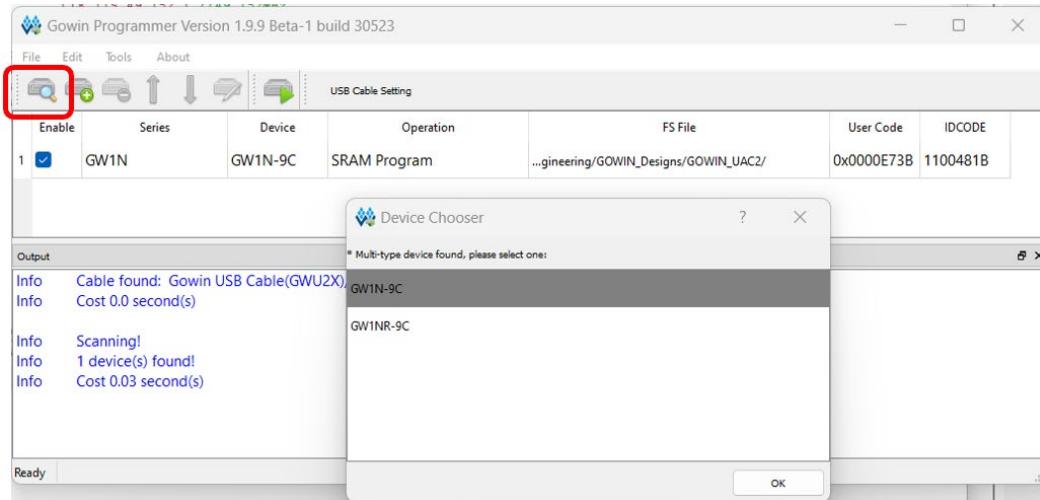
Next launch the GOWIN Programmer and the cable should be automatically detected.  
This should happen with just the USB connected to the PC,  
I.e. without needing to connecting the USB Programmer JTAG connector to the FPGA.

Note the download frequency is fixed at 1.33MHz for now.



Connect the JTAG programmer to the target device, then use the magnifying glass icon to automatically detect the FPGA device.

When prompted select device type **GW1N-9C**.



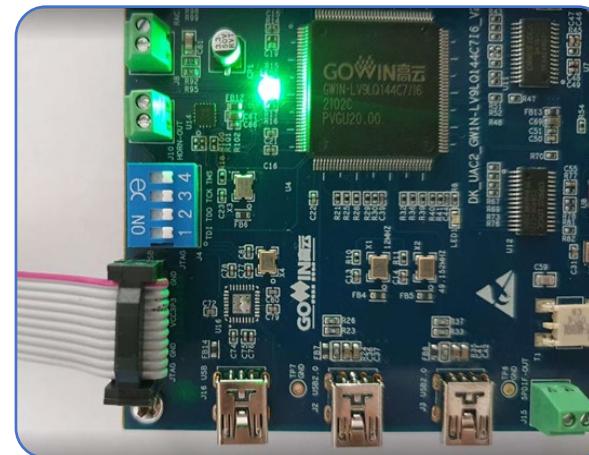
The programming cable is installed correctly, and the FPGA is ready to be programmed. To confirm, select the “READ Device Codes” operation then press the green download icon. The expected “READ Device Codes” consul output is shown below.

```

Info Target Cable: Gowin USB Cable(GWU2X)/0/579/UEBTNKD9@1.33 MHz
Info Operation "Read Device Codes" is starting on device-1...
Info ID code is: 0x1100481B
Info User code is: 0x00000000
Info Status code is: 0x00039020
Info Cost 0.06 second(s)
  
```

## JTAG Connector J11

- DK\_UAC2\_GW1N-LV9LQ144C7I6\_V2.0
- NB The Red line indicates Pin-1 TCK



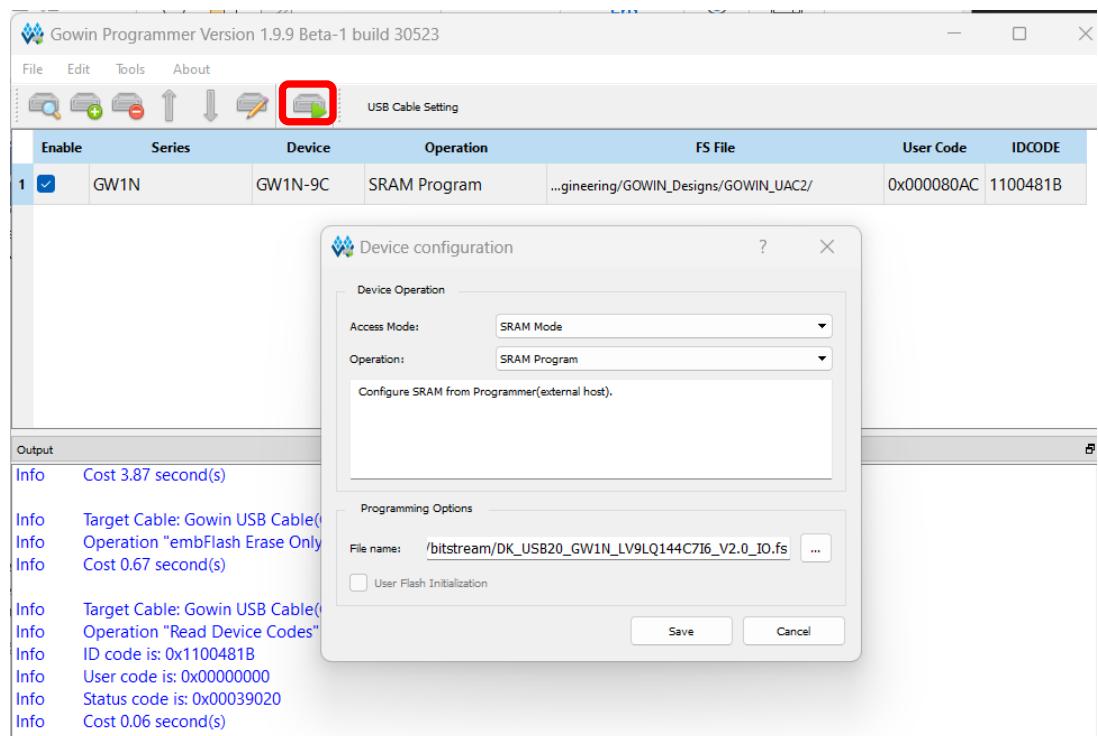
Using the GOWIN Programmer GUI to program the GW1N-9C FPGA device.

Set the Programming Mode as either

- SRAM Mode, SRAM Program (Volatile) or
- Embedded Flash Mode, embFlash, Erase, Program (Non-Volatile)

Then select the appropriate \*.fs bitstream file as shown in the example below.

The bitstream is then downloaded by clicking the Download Icon as highlighted.



## SRAM Mode, SRAM Program (Volatile)

Programming download expected return status values.

Info Target Cable: Gowin USB Cable(GWU2X)/0/579/UEBTNKD9@1.33 MHz  
 Info Operation "SRAM Program" is starting on device-1...  
 Info User Code: 0x000080AC  
 Info Status Code: 0x0003F020  
 Info Cost 3.82 second(s)

## Embedded Flash Mode, embFlash, Erase, Program (Non-Volatile)

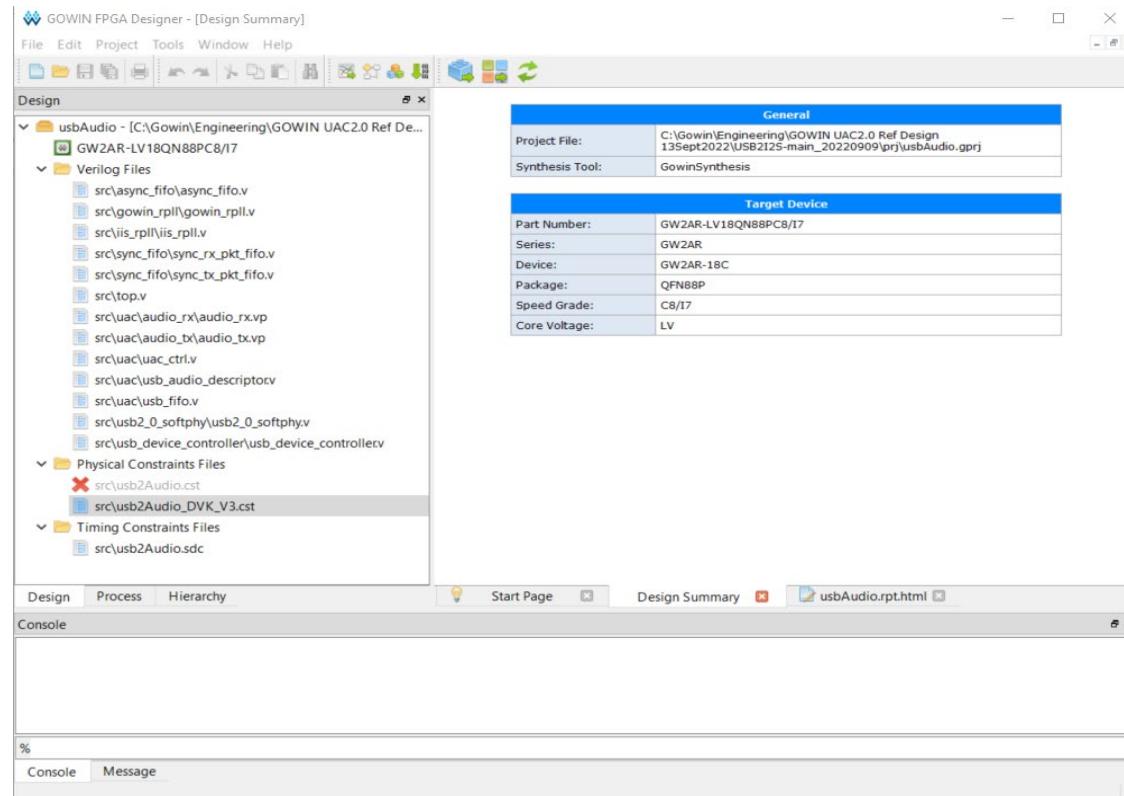
Programming download expected return status values.

Info Target Cable: Gowin USB Cable(GWU2X)/0/579/UEBTNKD9@1.33 MHz  
 Info Operation "embFlash Erase,Program" is starting on device-1...  
 Info Status Code: 0x0001F020  
 Info User Code: 0x000080AC  
 Info Cost 10.15 second(s)

The GOWIN FPGA project targets the GOWIN GW1N-LV9LQ144C7/I6 FPGA and the GOWIN DK\_UAC2\_GW1N-LV9LQ144C7I6\_V2.0 evaluation board.

This provides a considerable number of resources for design expansion and debug.

Please note that the GOWIN USB 2.0 Soft-PHY IP requires a C7/I6 speed grade GW1N FPGA.



## To Open the UAC FPGA Project

- 1) Ensure the latest version of GOWIN EDA is installed and an active license is setup.
- 2) Launch GOWIN EDA
- 3) File --> Open --> Navigate to 'usbAudio.gprj'

The UAC reference design is written in Verilog HDL.

- **usb2Audio.cst** pin constraints for the DK\_UAC2\_GW1N-LV9LQ144C7I6\_V2.0 DVK
- **usb2Audio.sdc** timing constraints for the various clock domains

There are two open Verilog source files that can be modified by the customer.

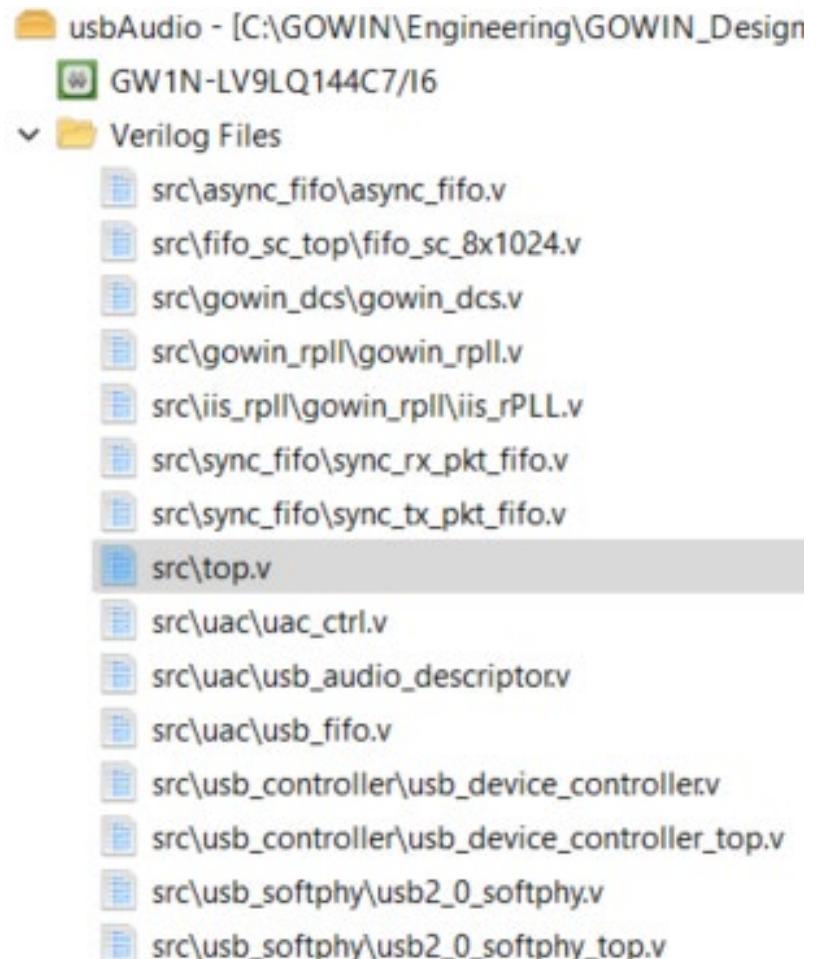
- **usb\_audio\_descriptor.v**
- **uac\_ctrl.v**

The remainder of the design including the USB Device Controller & Soft-PHY, I2S Audio Tx/Rx is encrypted and standard IP like FIFO, PLL etc. only expose their top-level wrappers.

The full list of design files are shown here on the right.

The top-level module file is named “**top.v**”

Constraints File	Description
usb2Audio.cst	Pin Constraint File
usb2Audio.sdc	Clock and Timing Constraint File



The UAC to I2S Reference Design is optimized for low density FPGAs and fits LittleBee and Aurora FPGA product families. The design is under 6K LUTs making it the ideal choice for developing a variety of low-cost USB audio products.

**Typical Resource utilization**

Resource Type	Resource Count
LUT	5714
REG	2363
PLL	2
BSRAM	9 SDPB 1 pROM

**Fabric Clocks FMAX – EDA V1.9.9Beta\_win**

Clock	Nominal Freq (MHz)	Max Freq (MHz)	Description
CLK_IN	12	83.3	USB Input
CLK_IIS_49_152_I	49.152		
CLK_IIS_45_158_I	45.158		
I2S_FCLK	98.304	99.114	Audio System
I2S_MCLK	49.150	~ 105	Audio System
USB_PCLK	60	~ 60	USB UTMI System
USB_CLKDIV	120	~ 121	USB PHY Internal

Top-Level Signal	Type	GW1N-LV9 Pin	DK_UAC2_GW1N-LV9LQ144C7I6_V2.0	Description
<b>Top-Level Parameters</b>				
P_LOOPBACK	Parameter	-	-	0 (default) = Mic Input, 1=I2S Loopback
GAIN_SLOT	Parameter	-	-	0 (default) = 12db, 1=6db
MIC_IIS_2_IO	Parameter	-	-	1 (default) = MIC IIS to I/O, 0= Mic IIS to MIC Chip
<b>USB2.0 Interface</b>				
USB_DXP_IO	Inout Port	Pin-48	J2 USB1-RC	USB IO Data
USB_DXN_IO	Inout Port	Pin-49	J2 USB1-RC	USB IO Data
USB_RXDP_I	Input Port LVDS25	Pin-42	J2 USB1-RC	USB IO Monitor
USB_RXDN_I	Input Port LVDS25	Pin-50	J2 USB1-RC	USB IO Monitor
USB_PULLUP_EN_O	Output Port LVCMOS33	Pin-40	J2 USB1-RC	USB Pull Up Control
USB_TERM_DP_IO	Inout Port LVCMOS33	Pin-46	J2 USB1-RC	USB Termination Control
USB_TERM_DN_IO	Inout Port LVCMOS33	Pin-47	J2 USB1-RC	USB Termination Control

Top-Level Signal	Type	GW1N-LV9 Pin	DK_UAC2_GW1N-LV9LQ144C7I6_V2.0	Description	
<b>Clocks</b>					
CLK_IN	Input Port	Pin-56	Net F_CLK_12M	USB Interface Clock Input 12MHz	
CLK_IIS_49_152_I	Input Port	Pin-58	Net F_CLK_49.152M	Audio Clock Input 49.152MHz	
CLK_IIS_45_158_I	Input Port	Pin-23	Net F_CLK_45.158M	Audio Clock Input 45.158MHz	
<b>I2S MEMs Microphone - MSM261S4030H0R – U5 &amp; U6</b>					
MIC_IIS_LRCK_O	Output Port	Pin-99	Net F_MIC_IIS_WS	FPGA I2S Audio Chip Select Output	
MIC_IIS_BCLK_O	Output Port	Pin-98	Net F_MIC_IIS_SCK	FPGA I2S Serial CLK Output	
MIC_IIS_DATA_I	Input Port	Pin-97	Net F_MIC_IIS_SD	FPGA I2S Left / Right Data Input	
<b>I2S Output to Amplifier - MAX98357AETE+T U14</b>					
IIS_LRCK_O	Output Ports	Pin-24	Net F_HORN_LRCLK	I2S Left Right Clock (LRCK) Output	
IIS_BCLK_O	Output Port	Pin-25	Net F_HORN_BCLK	I2S Continuous Serial BCLK Output	
IIS_DATA_O	Output Port	Pin-26	Net F_HORN_DIN	I2S Data Output	
HORN_SD_MODE_O	Output Port	Pin-27	Net F_HORN_SD_MODE	Shutdown Mode – TDM CH Select	
HORN_GAIN_SLOT_O	Output Port	Pin-28	Net F_HORN_GAIN_SLOT	Gain Slot – TDM CH Select	
<b>GPIO Header Signals J13</b>					
APM_IIS_LRCK_O	Output Port	Pin-133	Net F_GPIO1	J13 Pin-3	AMP Left Right Clock (LRCK) Output
APM_IIS_BCLK_O	Output Port	Pin-131	Net F_GPIO3	J13 Pin-5	AMP Serial BCLK Output
APM_IIS_DATA_O	Output Port	Pin-129	Net F_GPIO5	J13 Pin-7	AMP Data Output
MIC_IIS_2_IO_BCLK_O	Output Port	Pin-130	Net F_GPIO4	J13 Pin-6	Microphone Serial BCLK Output
MIC_IIS_2_IO_LRCK_O	Output Port	Pin-132	Net F_GPIO2	J13 Pin-4	Microphone Left Right Clock (LRCK) Output
MIC_IIS_2_IO_DATA_I	Input Port	Pin-128	Net F_GPIO6	J13 Pin-8	Microphone Data Input

### UAC HDL Top-Level Parameters

- **P\_LOOPBACK** 0: (disabled) Mic input | 1: = Received I2S from USB host is transmitted back to USB host
- **GAIN\_SLOT** 0: 12db | 1: 6db
- **MIC\_IIS\_2\_IO** 0: USB IIS to external Mic Amplifier | 1: USB IIS to GPIO Header Mic IO

Demo Ref	Bitstream Name	HDL Parameters	Demo Description
Test_01	DK_USB20_GW1N_LV9LQ144C7I6_V2.0.fs	P_LOOPBACK = 0 GAIN_SLOT = 0 MIC_IIS_2_IO = 0	Host PC audio stream output via FPGA to external amplifier
Test_02			MIC audio input via FPGA to Host PC -> Software Sound Recorder -> Host PC audio output via FPGA to external amplifier
Test_03			MIC audio input via FPGA to Host PC -> Host PC Output Speaker
Test_04	DK_USB20_GW1N_LV9LQ144C7I6_V2.0LOOPBACK.fs	P_LOOPBACK = 1 GAIN_SLOT = 0 MIC_IIS_2_IO = N/A	Host PC audio stream output via FPGA to external amplifier & Host PC Output Speaker
Test_05	DK_USB20_GW1N_LV9LQ144C7I6_V2.0_IO.fs	P_LOOPBACK = 0 GAIN_SLOT = N/A MIC_IIS_2_IO = 1	GPIO IIS MIC audio input via FPGA to Host PC Host PC audio stream output via FPGA to GPIO IIS Amplifier

## DK\_USB20\_GW1N\_LV9LQ144C7I6\_V2.0.fs

P\_LOOPBACK = 0 , // 0: (disabled) Mic input | 1: = Received I2S from USB host is transmitted back to USB host

GAIN\_SLOT = 0 , // Audio Amplifier gain : 0: 12db | 1: 6db

MIC\_IIS\_2\_IO = 0 // 0: USB IIS to external Mic Amplifier | 1: USB IIS to GPIO Header Mic IO

### **Max Frequency Summary:**

NO.	Clock Name	Constraint	Actual Fmax	Logic Level	Entity
1	USB_CLKDIV	120.005(MHz)	121.371(MHz)	8	TOP
2	PHY_CLKOUT	60.002(MHz)	60.058(MHz)	12	TOP
3	I2S_MCLK	49.152(MHz)	116.684(MHz)	8	TOP
4	I2S_FCLK	98.299(MHz)	99.114(MHz)	8	TOP

### **DK\_USB20\_GW1N\_LV9LQ144C7I6\_V2.0LOOPBACK.fs**

P\_LOOPBACK = 1 , // 0: (disabled) Mic input | 1: = Received I2S from USB host is transmitted back to USB host

GAIN\_SLOT = 0 , // Audio Amplifier gain : 0: 12db | 1: 6db

MIC\_IIS\_2\_IO = 0 // 0: USB IIS to external Mic Amplifier | 1: USB IIS to GPIO Header Mic IO

#### **Max Frequency Summary:**

NO.	Clock Name	Constraint	Actual Fmax	Logic Level	Entity
1	USB_CLKDIV	120.005(MHz)	119.072(MHz)	7	TOP
2	PHY_CLKOUT	60.002(MHz)	59.742(MHz)	18	TOP
3	I2S_MCLK	49.152(MHz)	107.535(MHz)	6	TOP
4	I2S_FCLK	98.299(MHz)	97.757(MHz)	9	TOP

The timing is marginal, due to recent EDA tool algorithm changes.

However, internal analysis show the design actually meets timing.

This issue will be fixed in the next EDA tool release 1.99-Beta-3.1 (scheduled for 8/18/2023)

## DK\_USB20\_GW1N\_LV9LQ144C7I6\_V2.0\_IO.fs

P\_LOOPBACK = 0 , // 0: (disabled) Mic input | 1: = Received I2S from USB host is transmitted back to USB host

GAIN\_SLOT = 0 , // Audio Amplifier gain : 0: 12db | 1: 6db

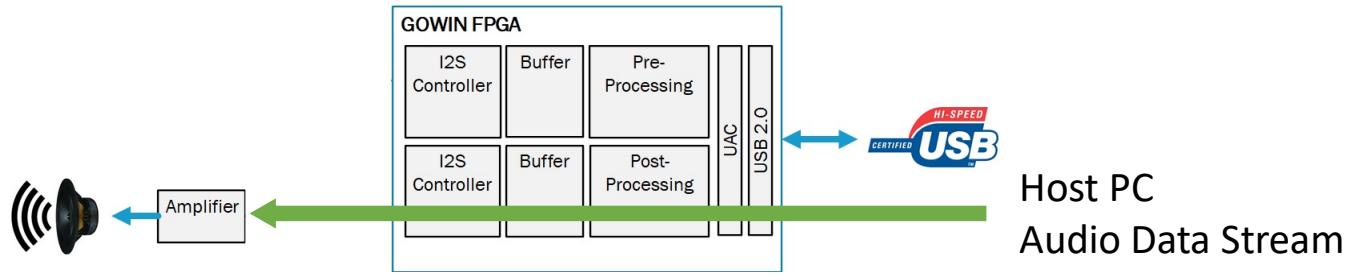
MIC\_IIS\_2\_IO = 1 // 0: USB IIS to external Mic Amplifier | 1: USB IIS to GPIO Header Mic IO

### **Max Frequency Summary:**

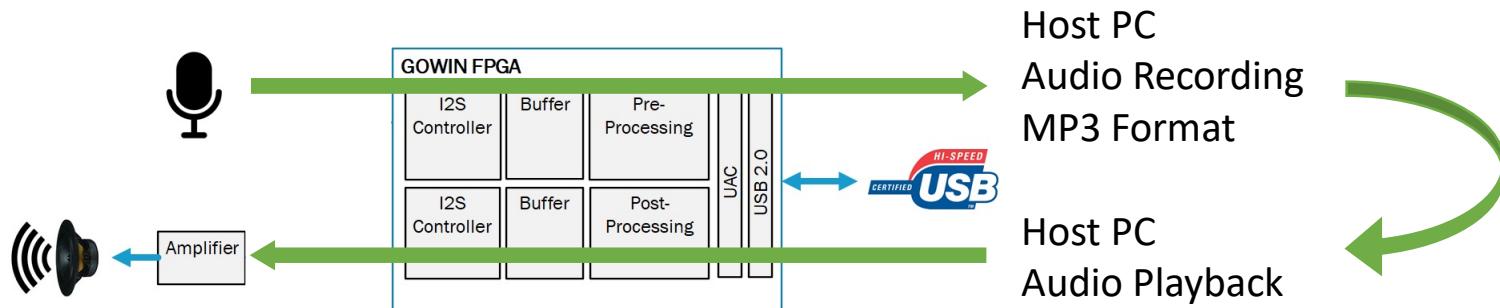
NO.	Clock Name	Constraint	Actual Fmax	Logic Level	Entity
1	USB_CLKDIV	120.005(MHz)	121.371(MHz)	8	TOP
2	PHY_CLKOUT	60.002(MHz)	60.058(MHz)	12	TOP
3	I2S_MCLK	49.152(MHz)	104.686(MHz)	4	TOP
4	I2S_FCLK	98.299(MHz)	99.114(MHz)	8	TOP

Please refer to *UAC2\_Demo\_SETUP.docx* for full details of the demo tests listed in the previous table.

## Test\_01 Host PC audio stream output via FPGA to external amplifier

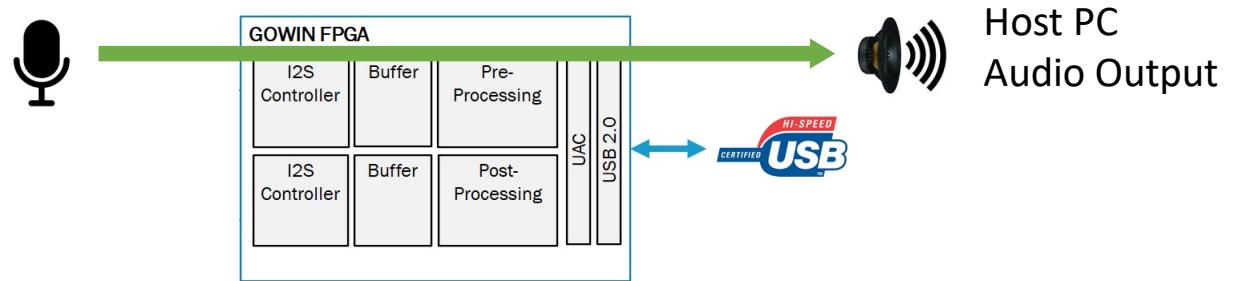


## Test\_02 MIC audio input via FPGA to Host PC -> Software Sound Recorder -> Host PC audio output via FPGA to external amplifier

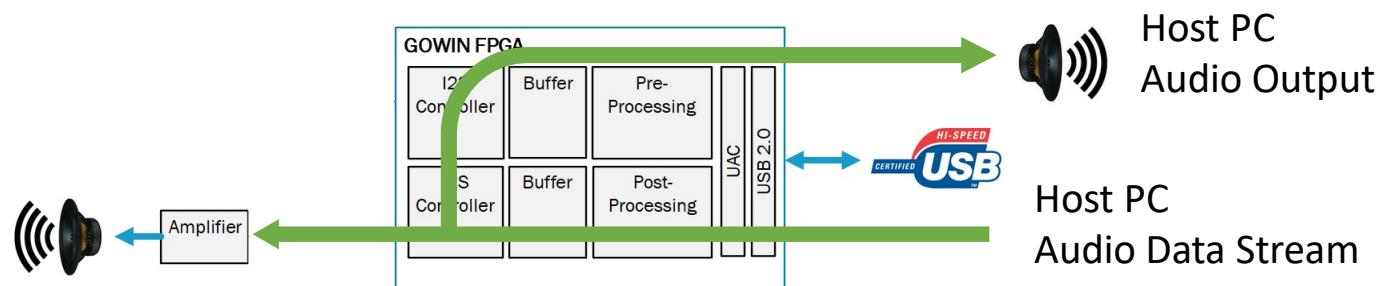


Please refer to *UAC2\_Demo\_SETUP.docx* for full details of the demo tests listed in the previous table.

## Test\_03 MIC audio input via FPGA to Host PC -> Host PC Output Speaker



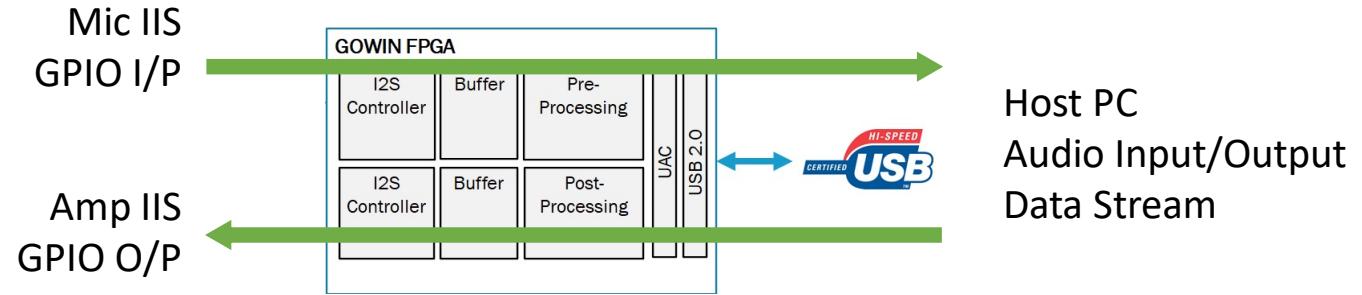
## Test\_04 Host PC audio stream output via FPGA to external amplifier & Host PC Output Speaker



Please refer to *UAC2\_Demo\_SETUP.docx* for full details of the demo tests listed in the previous table.

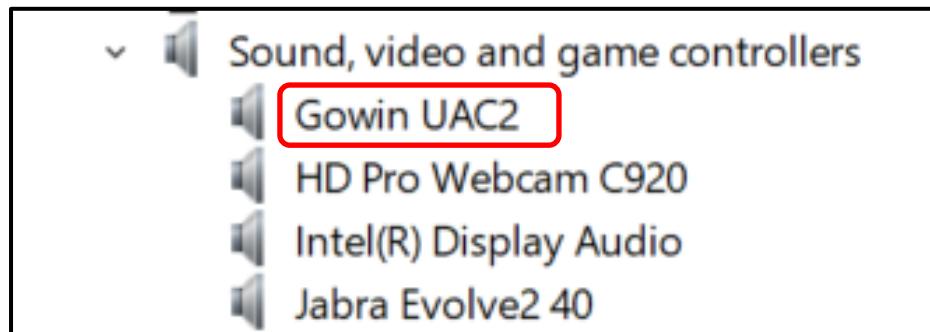
## Test\_05 GPIO IIS MIC audio input via FPGA to Host PC

Host PC audio output stream via FPGA to GPIO IIS Amplifier

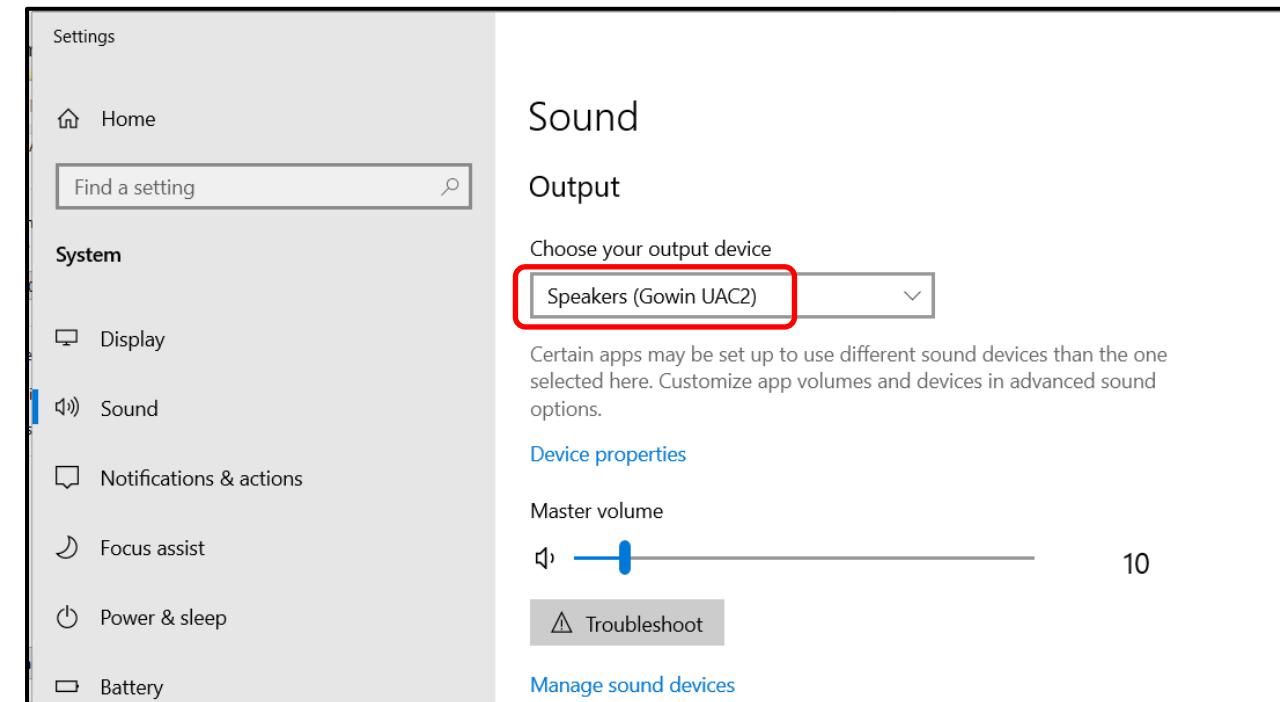


Windows10 “Device Manager” and “Sound Settings” will detect GOWIN UAC hardware as “Speakers (GOWIN UAC2)”

Windows10 OS Device Manager



Windows10 OS Sound Settings

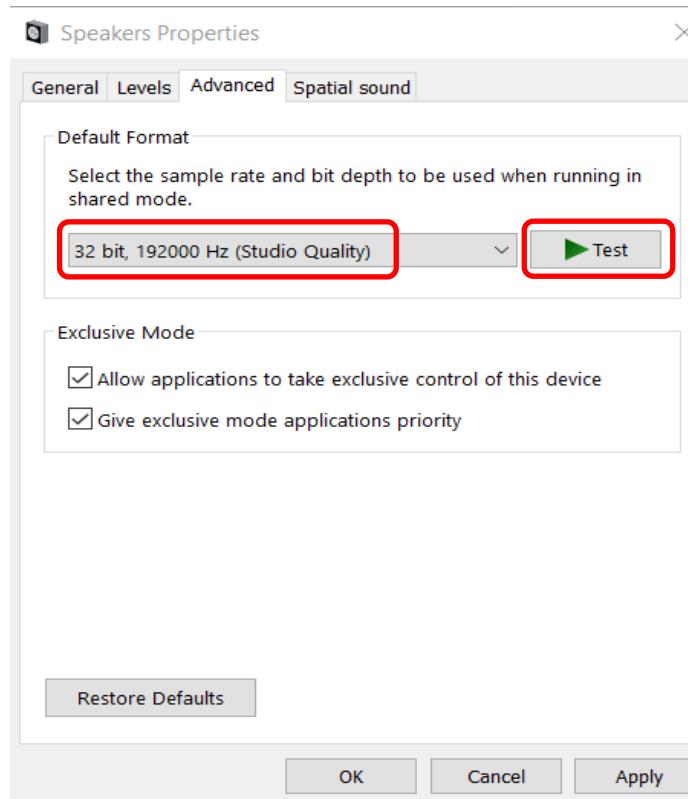


There's a simple but effective test feature built into Windows10

Windows10 -> Settings -> Sound

Select Output Device -> Speakers (GOWIN UAC2)

Select “Device Properties” -> “Additional Device Properties” -> Advanced



Select the Audio Bit Width and Sample Rate, and play a test tone to the USB2.0 UAC Speakers.

This will test both the left and right stereo channels.

### Supported Sample Rates

The UAC2 DVK includes 49.152MHz and 45.1584MHz crystal oscillators supporting sampling rates 32KHz, 44.1KHz, 48KHz, 64KHz, 88.2KHz, 96KHz, 128KHz, 176.4KHz, 192KHz, 352.8KHz, 384KHz, 705.6KHz & 768KHz at 16-bits, 24-bits and 32-bits.

If a sampling frequency isn't available, it's likely an OS driver issue because some drivers only support a limited range of sampling frequencies.

# Oscillator Frequencies & Audio Sample Rates

GOWIN Hardware	External OSC Freq	Supported Audio Sample Rates	Converted Audio Sample Rates	Comments
Audio_Eval_9K	49.152MHz	32KHz, 48KHz, 64KHz, 96KHz, 128KHz, 192KHz, 384KHz	N/A	GOWIN Internal Development Platform
Audio_Eval_9K	45.1584MHz	44.1KHz, 88.2KHz, 176.4KHz, 352.8KHz	N/A	GOWIN Internal Development Platform
DK_USB2.0_GW2AR18_V3.0 GW2AR-LV18QN88P C7/I6	8.192MHz	32KHz, 48KHz, 64KHz, 96KHz, 128KHz, 192KHz, 384KHz	44.1KHz -> 48KHz 88.2KHz -> 96KHz 176.4KHz -> 192KHz 352.8KHz -> 384KHz	GEN-1 UAC Demo Hardware
Gen2 UAC-2 DVK GW1N-LV9LQ144 C7/I6	49.152MHz 45.1584MHz	32KHz, 44.1KHz, 48KHz, 88.2KHz, 96KHz, 176.4KHz, 192KHz, 352.8KHz, 384KHz, 705.6KHz, 768KHz.		Gen-2 UAC Hardware

## New Product Incorporating GOWIN USB-To-I2S (UAC2)



Previous product [SHANLING UA3](#)  
Used a XMOS based UAC solution

Amazon [UA3 Portable Headphone Amplifier](#)

The image is a screenshot of the Amazon product page for the SHANLING UA3 Portable Headphone Amplifier. The page header shows "amazon" and "Deliver to United Kingdom". The search bar contains "shanning". The main product image shows two black UA3 units. The listing includes the price of \$1,599.00, a "High performance audio with iBasso" badge, and a "Currently unavailable" status. The product details section notes that it's a "SHANLING UA3 Portable Headphone Amplifier, Tiny Earphone Amps with Volume Control, USB DAC Balanced High Resolution, Sup 32bit/768kHz DSD512|3.5mm&4.4mm Jack, for Phone/Player/Nintendo Switch/PC (Black)". It has a 4.5-star rating from 14 reviews. The "About this item" section provides technical details: "25mm", "6.0mm", "Weight: 20.5g", and lists "Brand: SHANLING", "Model Name: SHANLING UA3", "Color: Black", "Form Factor: In Ear", and "Connectivity Technology: Wired". The "About this item" section also includes a bulleted list of features: "【Shanling UA2 upgrade】--Since the UA2 can only fine-tune the sound, we decided to let the Shanling UA3 Portable Headphone Amplifier achieve true free volume adjustment. We specially added a volume adjustment button, so you can adjust the volume and switch modes with one click.", "【Perfect Compatibility】--Portable headphone Amplifier compatible with various OS like Android/IOS/Windows/Mac/Nintendo Switch, you could use it connect most video device.", and "【High-Resolution Audio Amplifier】--Shanling UA3 headphones amp had improved on the basis of UA2, equipped with brand-new AKM AK4493SEQ DAC Chip & Dual RT8883 Amp Chip, supporting 32bit/768kHz and DSD512, AK4493SEQ has more powerful performance, the signal to noise ratio is as high as 120dB, and the excellent expressiveness makes the sound more realistic and natural!".

