DK_UAC2_GW1N-LV9LQ144C7I6_V2.0

User Guide

DBUG413-1.0E, 03/17/2023

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Revision History

Date	Version	Description
03/17/2023	1.0E	Initial version published.

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1 About This Guide

1.1 Purpose

The DK_UAC2_GW1N-LV9LQ144C7I6_V2.0 development board (hereinafter referred to as development board) user guide consists of following three parts:

- A brief introduction to the features of the development board
- An introduction to the development board system architecture and hardware resources
- An introduction to the hardware circuits, functions and pinout

1.2 Supported Products

The information presented in this guide applies to GW1N-LV9LQ144 device.

1.3 Related Documents

You can find the related documents at www.gowinsemi.com:

- DS100, GW1N series of FPGA Products Data Sheet
- UG114, GW1N-9 Pinout
- UG103, GW1N series of FPGA Products Package and Pinout User Guide
- UG290, Gowin FPGA Products Programming and Configuration Guide
- SUG100, Gowin Software User Guide

1.4 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
BSRAM	Block Static Random Access Memory
DDR	Double Data Rate
DSP	Digital Signal Processing
FLASH	Flash Memory
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
LDO	Low Dropout Regulator
LUT4	4-input Look-up Table
LVDS	Low-Voltage Differential Signaling
SPDIF	Sony/Philips Digital Interface Format
SSRAM	Shadow Static Random Access Memory

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

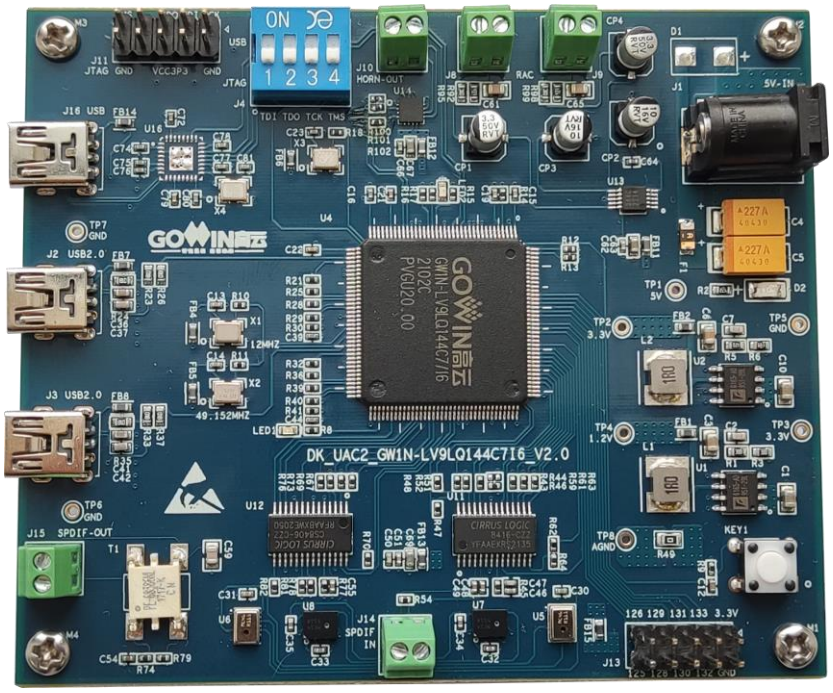
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_UAC2_GW1N-LV9LQ144C7I6_V2.0 Development Board



DK_UAC2_GW1N-LV9LQ144C7I6_V2.0 development board is embedded with GW1N-LV9LQ144 chip. It can be applied to USB 2.0 communication, microphone, SPDIF and other audio communications, 9X series of FPGA function evaluation, hardware reliability verification, and software learning and debugging, etc.

The GW1N series of FPGA products are the first generation of products in the LittleBee family. They offer abundant logic resources, multiple I/O standards, embedded BSRAM, DSP, PLL, and built-in Flash. They are non-volatile FPGA products with low power, instant-on, low-cost,

high-security, small size, various packages, and flexible usage.

The development board has the following features:

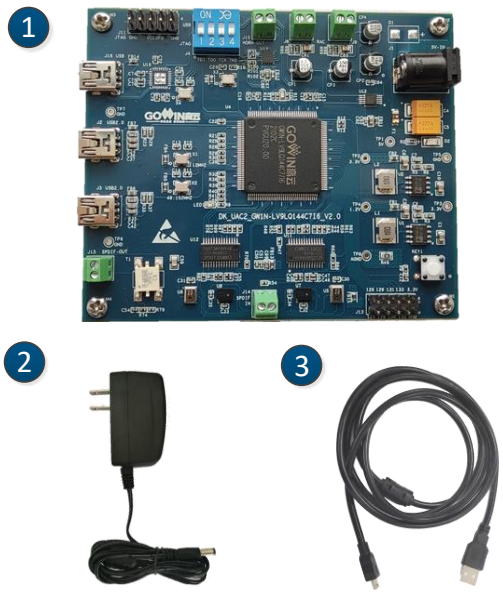
- Includes two USB 2.0 interfaces and supports USB 2.0 communication.
- Equipped with four microphone chips, and supports IIC and IIS microphone inputs.
- Equipped with CS8416-CZZR and CS8406-CZZR chips, and supports SPDIF digital audio communication.
- Equipped with CS4344-CZZR chip, and supports the communication of stereoscopic digital audio signal converting to analog audio signal.
- Equipped with MAX98357AETE+T chip, and can be connected to a 3.2W Output Power into 4Ω at 5V horn for audio signal output.
- Supports JTAG download.
- Reserves GPIO interfaces, LED, and keys to facilitate user test.

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_UAC2_GW1N-LV9LQ144C7I6_V2.0 development board
2. 5V power (Input: 100-240V~50/60Hz 0.5A, output: DC 5V 2A)
3. USB Mini B Data Cable

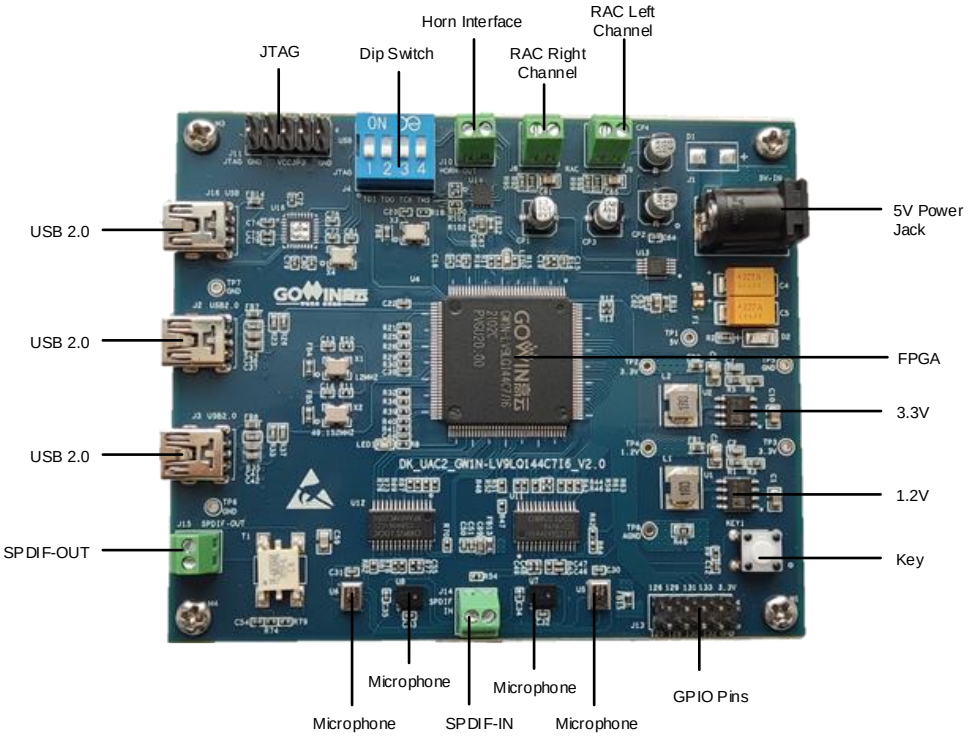
Figure 2-2 A Development Kit



① DK_UAC2_GW1N-LV9LQ144C7I6_V2.0 development board
② 5V Power Supply
③ USB Mini B Data Cable

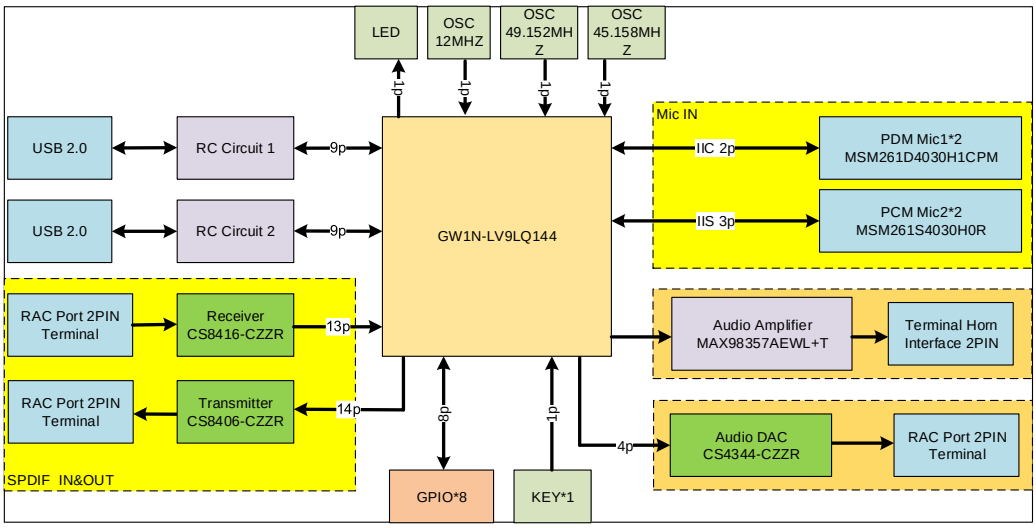
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The key features are as follows:

1. FPGA device
   - Gowin GW1N-LV9LQ144
   - Max. user I/O: 120
2. Download and Boot
   - Integrate a download module on the board, and download programs through JTAG downloader.
   - DONE light (LED2) will be on when programming or configuration is completed.
3. Power
   - External DC 5V 2A
   - LED is on after power on.
   - The development board provides 5.0V, 3.3V, and 1.2V power.
4. Clock system
   - 12MHz crystal oscillator: Provides 12MHz clock for GW1N-LV9LQ144.
   - 49.152MHz crystal oscillator: Provides 49.152MHz audio clock for GW1N-LV9LQ144.
   - 45.158MHz crystal oscillator: Provides 45.158MHz audio clock for GW1N-LV9LQ144.
5. USB 2.0 interface
   - Two USB 2.0 interfaces communicate with GW1N-LV9LQ144.
6. Microphone interface
   - Two IIS microphone array inputs: MSM261S4030H0R chip is used to provide microphone input of left and right channels.
   - Two IIC microphone array inputs: MSM261D4030H1CPM chip is used to provide microphone input of left and right channels.
7. SPDIF interface
   - One SPDIF digital audio input interface: CS8416-CZZR chip is used to decode and transmit the received stereoscopic digital audio data to the GW1N-LV9LQ144 chip.
   - One SPDIF digital audio output interface: CS8406-CZZR chip is used to encode and transmit the digital audio data sent by GW1N-LV9LQ144 chip.
8. Horn interface
   - One digital audio amplification output interface: MAX98357AETE+T chip is used to amplify the PCM signal sent by GW1N-LV9LQ144 chip for Class D to output.
9. RAC interface
   - One analog audio output interface: CS4344-CZZR chip is used to

convert the digital audio signal sent by GW1N-LV9LQ144 chip to analog signal to output.

10. GPIO interface
    - GPIO interface, enables communication with peripherals.
11. Debug module
    - 1 key
    - 1 LED (LED2)

3 Development Board Circuit

3.1 FPGA Module

Overview

For the resources of GW1N-LV9LQ144 FPGA products, please refer to *DS100, GW1N Series of FPGA Products*.

I/O BANK Introduction

For the I/O BANK, package, and pinout information, see *UG103, GW1N series of FPGA Products Package and Pinout User Guide*.

3.2 Download Module

3.2.1 Introduction

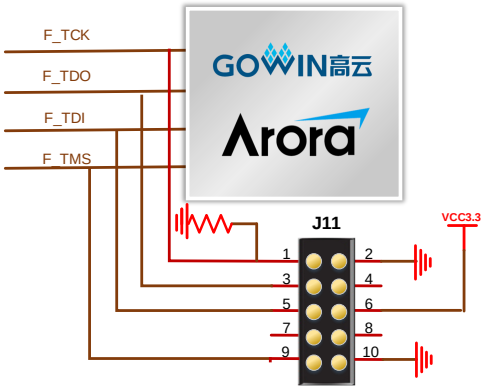
The development board offers a JTAG download interface. You can set the MODE value to download the programs to the on-chip SRAM or built-in Flash. When downloaded to the SRAM, the bitstream file will be lost if the device is powered down. When downloaded to the Flash, the bitstream file will not be lost if it is powered down.

The MODE value configuration is as follows:

1. In any mode, you can download the bitstream file to the on-chip SRAM and run it immediately.
2. Set MODE as "000" to download the bitstream file to the built-in Flash. When power on again, the device will read the FPGA configuration data from the built-in Flash automatically.

LED2 connected with DONE will be on after the program download is completed.

Figure 3-1 JTAG Download Connection Diagram



3.2.2 Pinout

Table 3-1 FPGA Download and Configuration Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_TCK	14	3	3.3V	JTAG Signal
F_TDO	18	3	3.3V	JTAG Signal
F_TDI	16	3	3.3V	JTAG Signal
F_TMS	13	3	3.3V	JTAG Signal

3.3 Power Supply

3.3.1 Introduction

The development board is powered via a power adapter. The input parameter is 100-240V~50/60MHz 0.5A, and the output is DC +5V 2A.

The input 5V power can generate 3.3V and 1.2V via the power conversion chip on the development board.

Convert DC+5V to DC+3.3V via FP6165ADXR-G1 chip and its peripheral circuit with a maximum output current of 3A.

Convert DC+3.3V to DC+1.2V via FP6165ADXR-G1 chip and its peripheral circuit with a maximum output current of 3A.

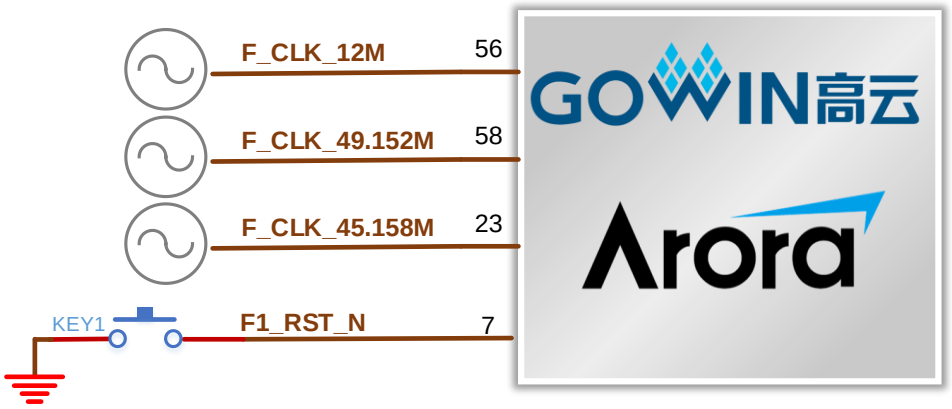
3.4 Clock and Reset

3.4.1 Introduction

The development board provides a 12MHz crystal oscillator connected to the global clock pins, and provides 49.152MHz and 45.158MHz crystal oscillators to generate the audio clocks for the board.

You can reset with the reset key (automatic reset when power on).

Figure 3-2 Connection Diagram of Clock and Reset



3.4.2 Pinout

Table 3-2 Clock and Reset Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_CLK_12M	56	2	3.3V	12MHz clock input
F_CLK_49.152M	58	2	3.3V	F_CLK_49.152MHz clock input
F_CLK_45.158M	23	3	3.3V	F_CLK_45.158MHz clock input
F1_RST_N	7	3	3.3V	Reset signal, active low.

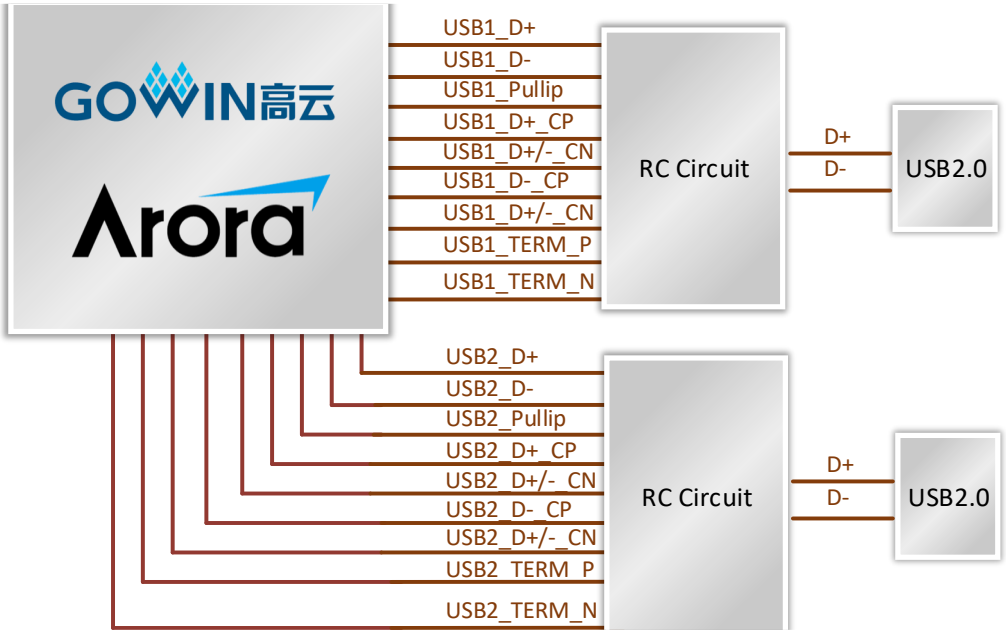
3.5 USB 2.0

3.5.1 Introduction

There are two USB 2.0 interfaces on the development board, which can be used for communication between the FPGA and the USB 2.0 interface.

The USB 2.0 interface is directly connected to the FPGA through configuration resistor.

Figure 3-3 USB Interface Connection Diagram



3.5.2 Pinout

Table 3-3 USB 2.0 Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
USB1_Pullip	40	2	3.3V	VBUS disconnect detection, used to reset USB
USB1_D+_CP	42	2	3.3V	USB+ signal
USB1_D+/-_CN	43	2	3.3V	USB+ reference signal
USB1_D-_CP	50	2	3.3V	USB- signal
USB1_D+/-_CN	51	2	3.3V	USB- reference signal
USB1_Term_p	46	2	3.3V	Terminal resistance control at high speed,

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
				USB data pin at full speed and low speed.
USB1_Term_n	47	2	3.3V	Terminal resistance control at high speed, USB data pin at full speed and low speed.
USB1_D+	48	2	3.3V	Data pin at USB high speed
USB1_D-	49	2	3.3V	Data pin at USB high speed
USB2_Pullip	62	2	3.3V	VBUS disconnect detection, used to reset USB
USB2_D+_CP	64	2	3.3V	USB+ signal
USB2_D+/-_CN	65	2	3.3V	USB+ reference signal
USB2_D-_CP	70	2	3.3V	USB- signal
USB_D+/-_CN	71	2	3.3V	USB- reference signal
USB2_Term_p	66	2	3.3V	Terminal resistance control at high speed, USB data pin at full speed and low speed.
USB2_Term_n	67	2	3.3V	Terminal resistance control at high speed, USB data pin at full speed and low speed.
USB2_D+	68	2	3.3V	Data pin at USB high speed
USB2_D-	69	2	3.3V	Data pin at USB high speed

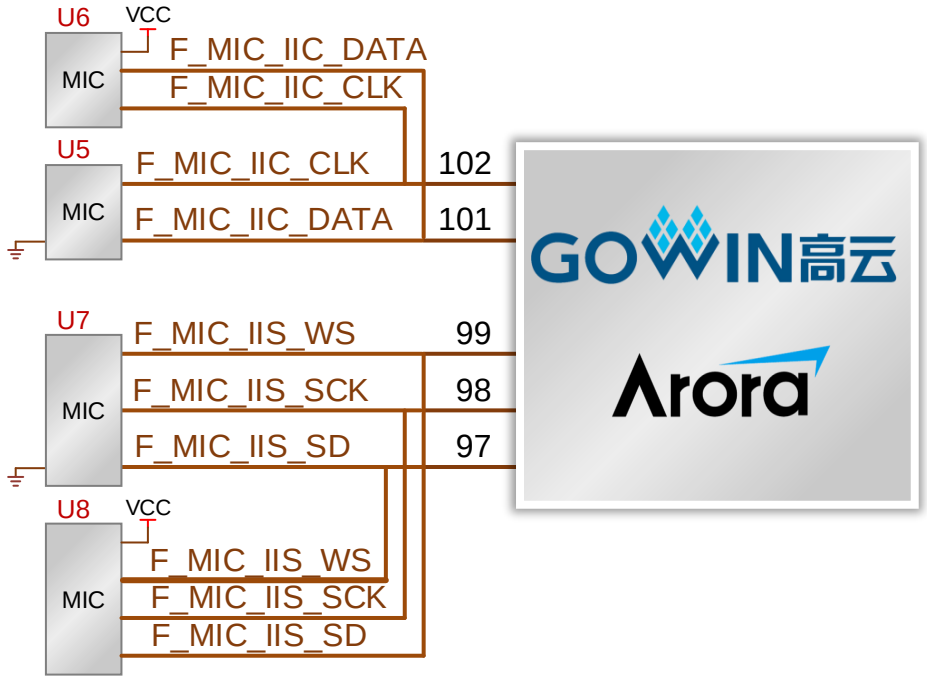
3.6 Microphone Input

3.6.1 Introduction

The development board is equipped with four microphones, two MSM261S4030H0R microphones of IIS input and two MSM261D4030H1CPM microphones of IIC input.

The 192KHz digital audio transmission is supported.

Figure 3-4 Microphone Connection Diagram



3.6.2 Pinout

Table 3-4 Microphone Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_MIC_IIC_CLK	102	1	3.3V	IIC audio clock signal
F_MIC_IIC_DATA	101	1	3.3V	IIC audio data signal
F_MIC_IIS_WS	99	1	3.3V	IIS audio chip selected signal
F_MIC_IIS_SCK	98	1	3.3V	IIS audio clock signal
F_MIC_IIS_SD	97	1	3.3V	IIS audio data signal

3.7 SPDIF Interface

3.7.1 Introduction

The development board is equipped with two SPDIF digital audio interfaces, one for SPDIF input and the other for SPDIF output.

The digital audio signal received by the SPDIF interface is decoded and transmitted via the CS8416-CZZR.

The CS8406-CZZR encodes the digital audio data sent by the GW1N-LV9LQ144 chip and transmits it to the SPDIF output interface.

Figure 3-5 SPDIF Interface Connection Diagram

3.7.2 Pinout

Table 3-5 SPDIF Input Interface Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SPDIFI_RST_N	124	0	3.3V	Reset signal, active low.
SPDIFI_OLRCK	123	0	3.3V	The word rate clock signal for audio data on the SDOUT pin
SPDIFI_OSCLK	122	0	3.3V	The serial bit clock signal for audio data on the SDOUT pin.
SPDIFI_AD0	121	0	3.3V	Address signal
SPDIFI_AD1	120	0	3.3V	Address signal
SPDIFI_SCL	119	0	3.3V	Serial control clock signal
SPDIFI_SDA	118	0	3.3V	Serial control data signal
PDIFI_GPO2	117	0	3.3V	General-purpose output signal
PDIFI_GPO1	116	1	3.3V	General-purpose output signal

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
PDIFI_GPO0	115	1	3.3V	General-purpose output signal
SPDIFI_RMCK	114	1	3.3V	Master clock output recovered from the phase-locked loop
SPDIFI_OMCK	113	1	3.3V	System clock input signal
PDIFI_SDOUT	112	1	3.3V	Audio serial data output

Table 3-6 SPDIF Output Interface Pinout

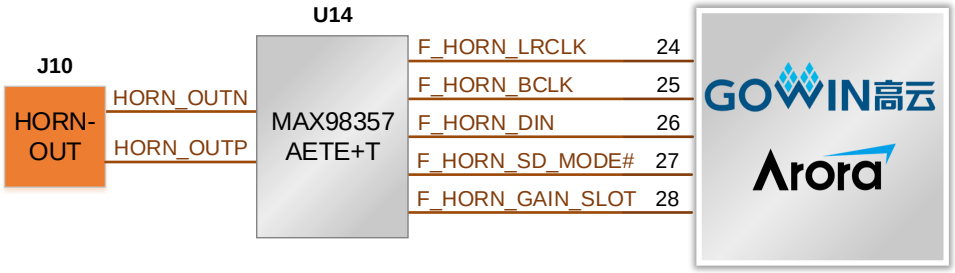
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SPDIFO_TCBL	96	1	3.3V	Transmit channel status block start
SPDIFO_INT	95	1	3.3V	Interrupt
SPDIFO_OMCK	94	1	3.3V	Master Clock
SPDIFO_AD1	93	1	3.3V	Address signal
SPDIFO_SCL	92	1	3.3V	Serial control clock signal
SPDIFO_SDA	90	1	3.3V	Serial control data signal
SPDIFO_AD0	88	1	3.3V	Address signal
SPDIFO_AD2	87	1	3.3V	Address signal
SPDIFO_RXP	86	1	3.3V	Auxiliary AES3 receiver port
SPDIFO_RST_N	85	1	3.3V	Reset signal, active low.
SPDIFO_ILRCK	84	1	3.3V	Serial audio input left/right clock
SPDIFO_ISCLK	83	1	3.3V	Serial audio clock signal
SPDIFO_U	81	1	3.3V	User data
SPDIFO_SDIN	78	2	3.3V	Serial audio data signal

3.8 Speaker Interface

3.8.1 Introduction

The development board is equipped with one digital audio amplification output interface. The GW1N-LV9LQ144 processed PCM audio signal is output to the horn interface via MAX98357AETE+T for Class D amplification.

Figure 3-6 Horn Interface Connection Diagram



3.8.2 Pinout

Table 3-7 Speaker Interface Pinout

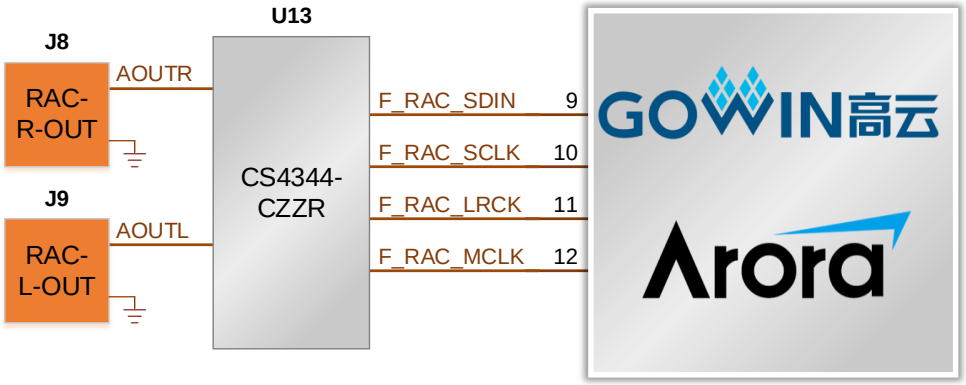
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_HORN_LRCLK	24	3	3.3V	Frame clock signal
F_HORN_BCLK	25	3	3.3V	Bit clock input signal
F_HORN_DIN	26	3	3.3V	Digital input signal
F_HORN_SD_MODE#	27	3	3.3V	Chip selected signal
F_HORN_GAIN_SLOT	28	3	3.3V	Gain and channel selected signal

3.9 RAC Interface

3.9.1 Introduction

The development board is equipped with one analog audio output interface, and the digital audio signal processed by GW1N-LV9LQ144 is converted digital-to-analog via CS4344-CZZR.

Figure 3-7 RAC Interface Connection Diagram



3.9.2 Pinout

Table 3-8 RAC Interface Pinout

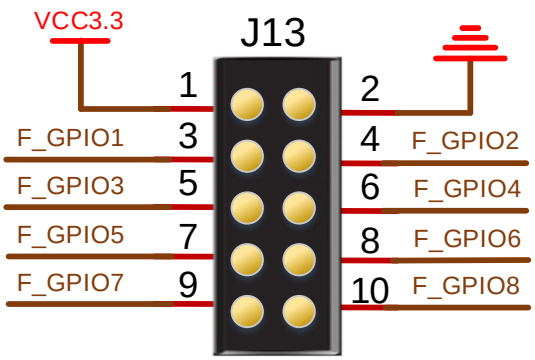
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_RAC_SDIN	9	3	3.3V	Serial audio data input
F_RAC_SCLK	10	3	3.3V	Serial clock input signal
F_RAC_LRCK	11	3	3.3V	Left/right channel clock input signal
F_RAC_MCLK	12	3	3.3V	Master clock input signal

3.10 GPIO

3.10.1 Introduction

To facilitate user testing, one double row pin header J13 with 2.54mm pitch is reserved on the development board, and there are a total of 8 GPIOs.

Figure 3-8 GPIO Connection Diagram



3.10.2 Pinout

Table 3-9 GPIO Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
GPIO1	133	0	3.3V	General-purpose input/output
GPIO2	132	0	3.3V	General-purpose input/output
GPIO3	131	0	3.3V	General-purpose input/output
GPIO4	130	0	3.3V	General-purpose input/output
GPIO5	129	0	3.3V	General-purpose input/output
GPIO6	128	0	3.3V	General-purpose input/output
GPIO7	126	0	3.3V	General-purpose input/output
GPIO8	125	0	3.3V	General-purpose input/output

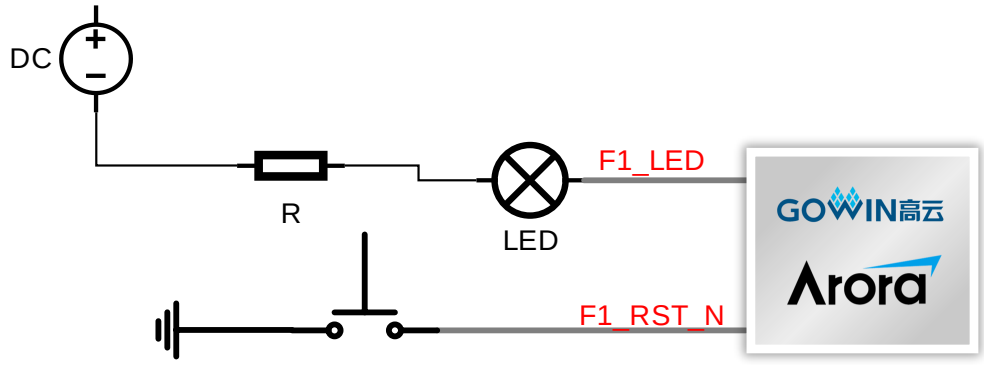
3.11 LED & Key

3.11.1 Introduction

The development board reserves one LED connected to the FPGA. When the FPGA outputs logic low, the LED is lit; when it outputs logic high, the LED goes out.

The development board is equipped with a key (hardware de-jitter) connected to the FPGA, which can be used flexibly by users.

Figure 3-9 LED & Key Connection Diagram



3.11.2 Pinout

Table 3-10 LED & Key Module Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F1_RST_N	7	3	3.3V	Key IO
F1_LED	75	2	3.3V	LED_IO

4 Gowin Software

Please refer to *SUG100, Gowin Software User Guide* for details.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