DK_GoAI_GW2AR-LV18QN88PC8I7_V1.1

User Guide

DBUG396-1.0E, 08/02/2021

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Revision History

Date	Version	Description
08/02/2021	1.0E	Initial version published.

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1 About This Guide

1.1 Purpose

DK_GoAI_GW2AR-LV18QN88PC8I7_V1.1 user guide consists of the following four parts:

1. A brief introduction to the features and hardware resources of the development board;
2. An introduction to the functions, circuits, and pinouts of each module;
3. Considerations for the use of development board;
4. An introduction to the usage of the FPGA development software.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. DS226, GW2AR series of FPGA Products Data Sheet
2. UG229, GW2AR series of FPGA Products Package and Pinout User Guide
3. UG115, GW2AR-18 Pinout
4. UG290, Gowin FPGA Products Programming and Configuration Guide
5. SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
SIP	System in Package

Terminology and Abbreviations	Meaning
SDRAM	Synchronous Dynamic RAM
CFU	Configurable Function Unit
CLS	Configurable Logic Slice
CRU	Configurable Routing Unit
LUT4	4-input Look-up Tables
LUT5	5-input Look-up Tables
LUT6	6-input Look-up Tables
LUT7	7-input Look-up Tables
LUT8	8-input Look-up Tables
REG	Register
ALU	Arithmetic Logic Unit
IOB	Input/Output Block
SSRAM	Shadow Static Random Access Memory
BSRAM	Block Static Random Access Memory
SP	Single Port
SDP	Semi Dual Port
DP	Dual Port
DSP	Digital Signal Processing
TDM	Time Division Multiplexing
DQCE	Dynamic Quadrant Clock Enable
DCS	Dynamic Clock Selector
PLL	Phase-locked Loop
DLL	Delay-locked Loop
QN88	QFN48 Package

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

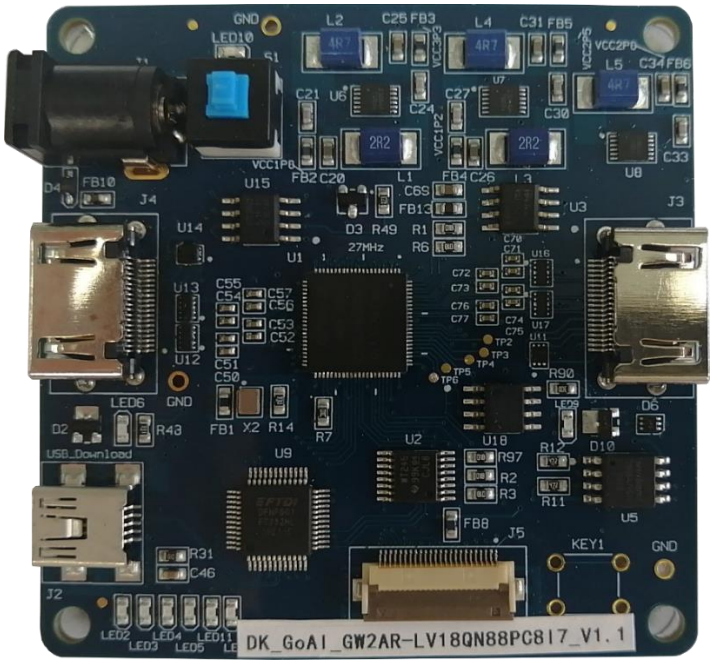
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_GoAI_GW2AR-LV18QN88PC8I7_V1.1 Development Board



The development board uses Gowin GW2AR-18 FPGA devices embedded with 64 Mbit PSRAM, The GW2AR series of FPGA products are the first generation products of Gowin Arora family. As a kind of SIP chips, the GW2AR series of FPGA products offer a range of features and rich resources like high-performance DSP, high-speed LVDS interface and BSRAM. These embedded resources combine a streamlined FPGA architecture with a 55nm process to make the GW2A series of FPGA products ideal for high-speed and low-cost applications.

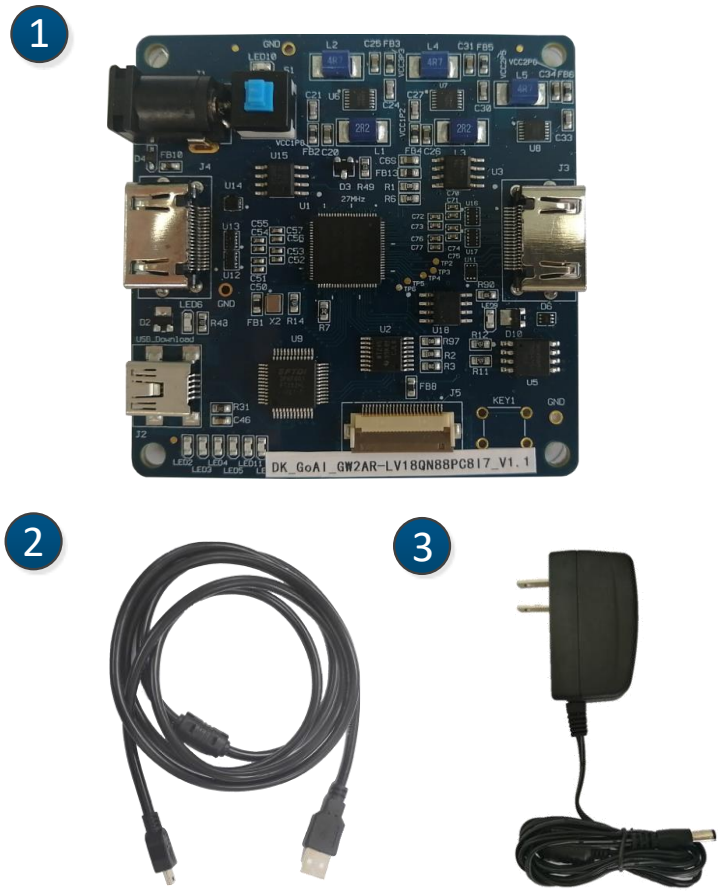
The development board offers abundant external interfaces, including Camera interfaces, HDMI interfaces, etc. There are also LED, Reset, Clock and other resources for developers or fans to learn to use.

2.2 A Development Board Suite

A development board suite includes the following items:

- DK_GoAI_GW2AR-LV18QN88PC8I7_V1.1 development board
- USB Cable
- DC5V power supply

Figure 2-2 A Development Board Suite



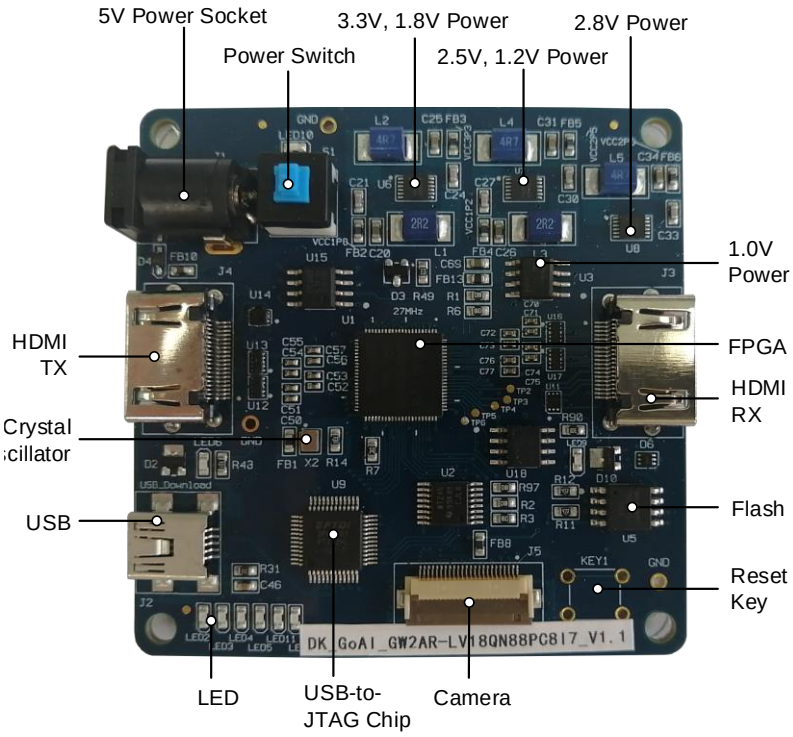
① DK_GoAI_GW2AR-LV18QN88PC8I7_V1.1 development board

② USB Cable

③ DC5V power supply

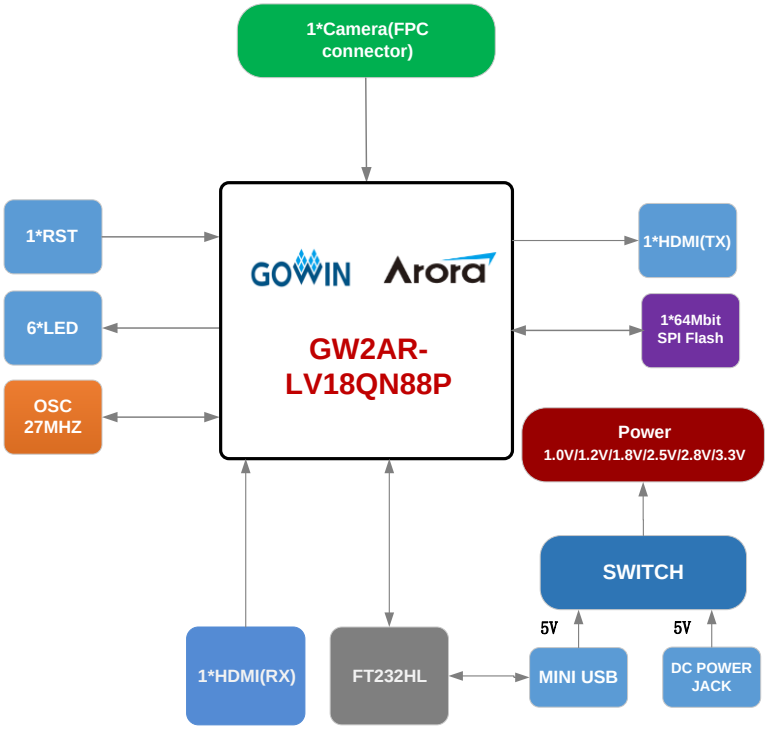
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The structure and features of the development board are as follows:

1. FPGA
   - Adopts QN48 package
   - Up to 66 user I/O
   - Abundant LUT4 resources
   - Multiple modes and capacities of B-SRAM
2. FPGA Configuration Modes
   - JTAG
   - MSPI
3. Clock resource
   27MHz Clock Crystal Oscillator
4. Key
   - 1 reset button
   - 1 key switch
5. LED
   - 1 power indicator (green)
   - 2 HDMI hot-plug indicators (green)
   - 6 LEDs (green)
6. Memory
   - 64Mbit embedded PSRAM
   - 64Mbit external SPI Flash
7. GPIO
   5 I/O expansion resources
8. HDMI
   - 1 HDMI TX Interface;
   - 1 HDMI RX Interface
9. DC-DC (LDO) power supply
   Supports 3.3V, 2.8V, 2.5V, 1.8 V, 1.2V and 1.0V power supply

2.6 Development Board Specification

Table 2-1 Development Board Specification

No.	Item	Functional Description	Technical Condition	Note
1	FPGA	Core chip	–	–
2	Download	Support USB interface; Support JTAG, MSPI	USB to JTAG chip integrated on board	–
3	Power Supply	3.3 V, 2.8V, 2.5V, 1.8V, and 1.2 V,1.0V output via LDO circuit (DC-DC).	● Input power: 5V ● Provide power for FPGA, download circuit and other circuits via 5V to 3.3V circuit; ● Provide power for camera via 5V to 2.8V circuit; ● Provide power for HDMI_RX and FPGA via 5V to 2.5V circuit; ● Provide power for FPGA PSRAM via 5V to 1.8 V circuit; ● Provide power for camera input via 5V to 1.2V circuit; ● Provide power for FPGA via 5 V to 1.0V circuit.	–
4	Push Switches	Power Switches for FPGA	1	–
5	Reset button	Reset for FPGA	1	–
6	LED	Test indicator, HDMI hot-plug indicator, Power indicator	● 6 test indicators, green; ● 2 hot-plug indicator, green; ● 1 power indicator, green.	–
7	Crystal Oscillator	Provide 27MHz clock for FPGA	Package 2520	–
8	Memory	Provide PSRAM and Flash	64Mbit embedded PSRAM 64Mbit external SPI Flash	–
9	GPIO	I/O for user to extend and test	5	–
10	HDMI	Used for design	1 HDMI TX Interface; 1 HDMI RX Interface	–

No.	Item	Functional Description	Technical Condition	Note
11	FPC connector	Used for camera	24PIN FPC	–
12	Protection	● USB interface: ESD protection; ● Power interface: Inverse current and over current protection; ● HDMI interface: ESD protection;	● USB interface ESD protection: ±15kV non-contact discharge, ± 8kV contact discharge; ● Schottky diode is connected between positive and negative anodes of power interface; ● 2A self-recovery fuses are connected at power inlet ● HDMI interface ESD protection: 1. ±17kV non-contact discharge, ± 12kV contact discharge; 2. ±15kV non-contact discharge, ± 8kV contact discharge;	–
13	Voltage	–	Input Voltage: 5V	–
14	Humidity	–	95%	–
15	Temperature	–	Operating range: -40°~85°	–

3 Development Board Circuit

3.1 FPGA Module

Overview

For the resources of GW2AR series of FPGA Products, see DS226, *GW2AR Series of FPGA Products Data Sheet*.

I/O BANK Introduction

For the I/O BANK, package, and pinout information, see UG229 *GW2AR Series of FPGA Products Package and Pinout User Guide*.

3.2 Download

3.2.1 Overview

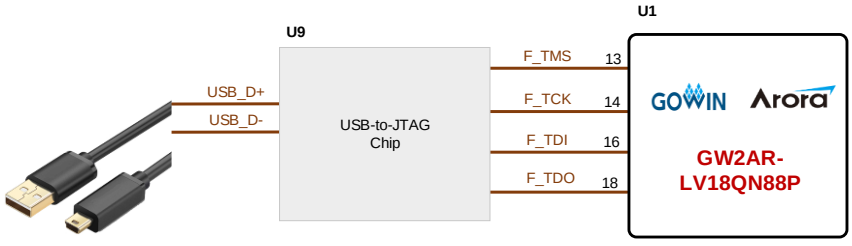
The development board provides a USB downloading interface. Download to on-chip SRAM or external SPI Flash as required.

Note!

- When downloaded to SRAM, the data stream file will be lost if the device is powered down, and it will need to be downloaded again after power-on.
- If downloaded to SPI flash, the data stream file will not be lost if the device is powered down.

3.2.2 USB Download Circuit

Figure 3-1 FPGA USB Download Connection Diagram



3.2.3 Download Flow

1. FPGA SRAM Download Mode:

   Plug the USB cable to the development board USB interface (J2). Then power on and open the Programmer tool, select SRAM mode and select the bitstream file to be downloaded.

2. FPGA MSPI Download Mode:
   Plug the USB cable into the USB port (J2) of the development board, then power on and open the Programmer tool, select External Flash mode, and select the bitstream file and FLASH device model to be downloaded. After a successful download, power off and then power on, the device will import the bitstream file from the external Flash into the SRAM.

3.2.4 Pinout

Table 3-1 FPGA Download Pinout

Signal Name	Pin No.	BANK	Description	I/O Level
TMS	5	2	JTAG Signal	1.8V
TCK	6	2	JTAG Signal	1.8V
TDI	7	2	JTAG Signal	1.8V
TDO	8	2	JTAG Signal	1.8V
MODE0	88	3	Mode selection pin	3.3V
MODE1	87	3	Mode selection pin	3.3V

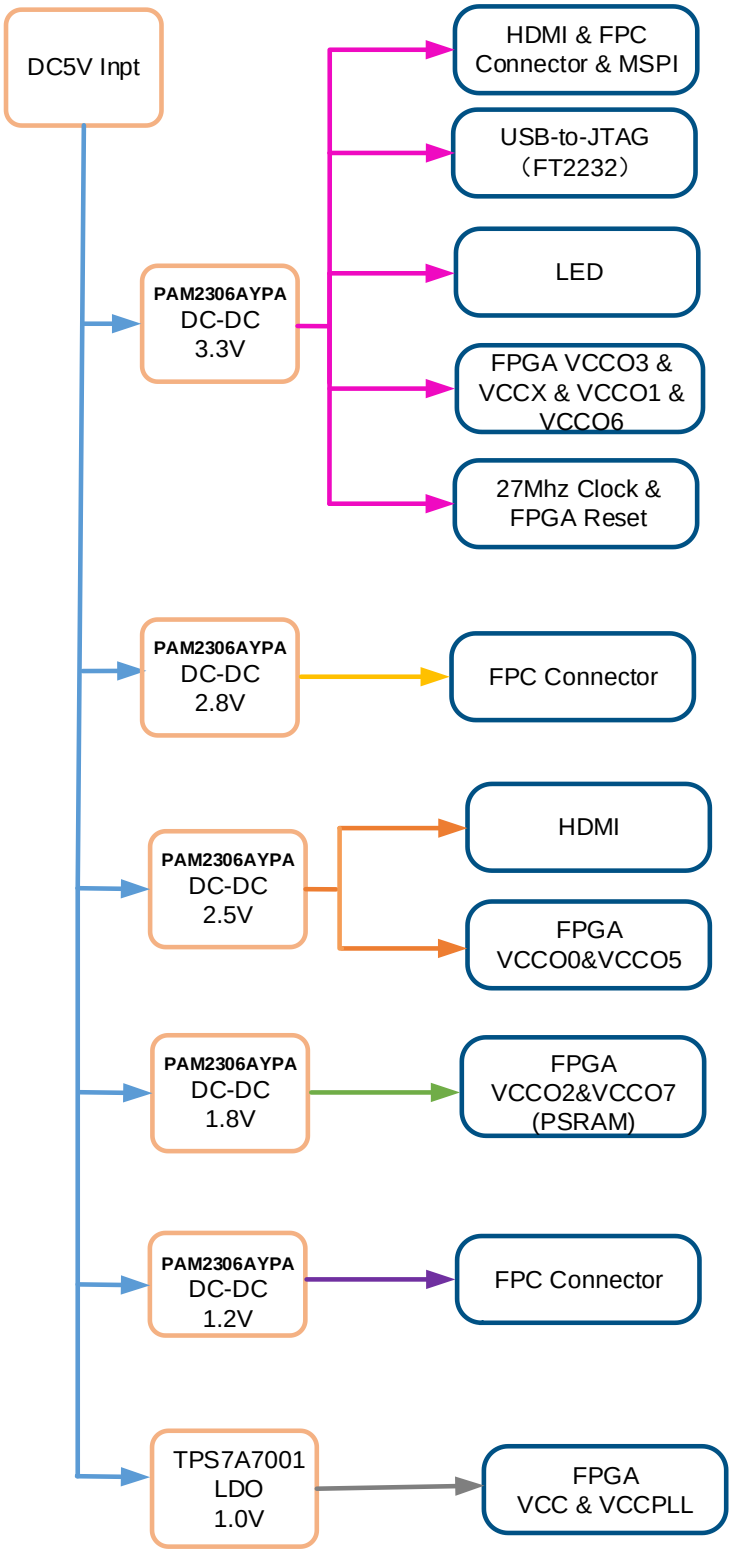
3.3 Power Supply

3.3.1 Overview

DC5V is input by USB interface. The TI LDO power supply chip and ONSEMI DC-DC power supply chip are used to step down voltage from 5V to 3.3V, 2.8V, 2.5V, 1.8V,1.2V, and 1.0V, which can meet the power demand of the development board.

3.3.2 Power System Distribution

Figure 3-2 Power Supply System Distribution



3.3.3 FPGA Power Supply Pinout

Table 3-2 FPGA Power Supply Pinout

Signal Name	Pin No.	BANK	Description	I/O Level
VCCO0	78	0	I/O Bank Voltage	2.5V
VCCO1	12, 67	1	I/O Bank Voltage	3.3V
VCCO2	3, 64	2	I/O Bank Voltage	1.8V
VCCO3	58	3	I/O Bank Voltage	3.3V
VCCO4	44	4	I/O Bank Voltage	3.3V
VCCO5	23	5	I/O Bank Voltage	2.5V
VCCO6	12, 67	6	I/O Bank Voltage	3.3V
VCCO7	3, 64	7	I/O Bank Voltage	1.8V
VCCPLLL1	14	-	PLLL1 power supply	1.0V
VCCPLLR1	50	-	PLLL1 power supply	1.0V
VCCX	12, 67	-	Auxiliary voltage are internally connected to VCCO1, VCCO6	3.3V
VCC	1, 22, 45, 66	-	Core voltage	1.0V
VSS	2, 21, 24, 43, 46, 65, 68	-	GND	-

3.4 Clock, Reset

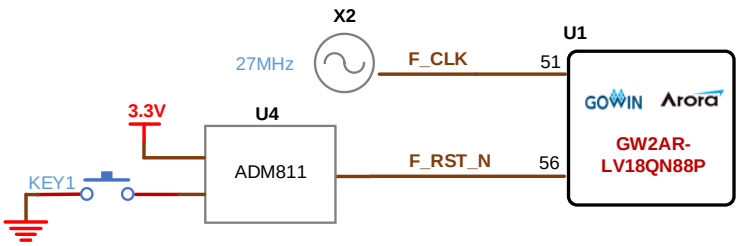
3.4.1 Overview

The development board provides a 27MHz crystal oscillator connected to the PLL input pin. This can be employed as the input clock for the PLL in FPGA. Frequency division and multiplication of PLL can output the clock required by the user.

At the same time, in order to facilitate debugging design, the development board adds a reset signal, active low.

3.4.2 Clock, Reset Circuit

Figure 3-3 Clock, Reset Circuit



3.4.3 Pinout

Table 3-3 FPGA Clock and Reset Pinout

Signal Name	Pin No.	BANK	Description	I/O Level
F_CLK	51	3	27MHz crystal oscillator Input	3.3V
F_RST_N	56	3	Reset Signal, Active Low	3.3V

3.5 LED

3.5.1 Overview

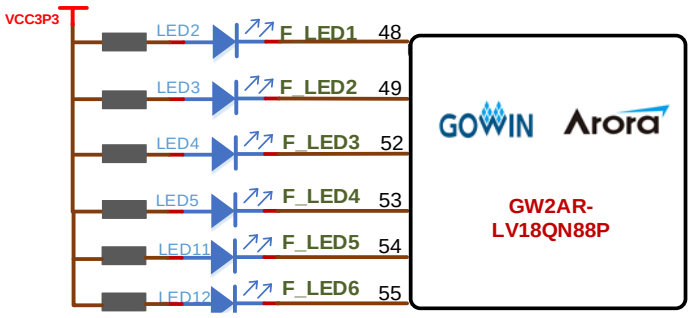
There is one green LED in the development board and users can display the required status through the LED. There is one or two LEDs left to facilitate the observation of power supply and HDMI hot-plug status.

You can test the LEDs in the following ways:

- When the FPGA corresponding pin output signal is logic low, the LED is lit;
- If the signal is high, LED is off.

3.5.2 LED Circuit

Figure 3-4 LED Circuit



3.5.3 Pinout

Table 3-4 LED Pinout

Signal Name	Pin No.	BANK	Description	I/O Level
F_LED1	48	3	LED2	3.3V
F_LED2	49	3	LED3	3.3V
F_LED3	52	3	LED4	3.3V
F_LED4	53	3	LED5	3.3V
F_LED5	54	3	LED11	3.3V
F_LED6	55	3	LED12	3.3V

3.6 GPIO

3.6.1 Overview

To facilitate the extension and testing for user functions, 5 GPIO test points are reserved on the development board.

3.6.2 Pinout

Table 3-5 GPIO Pinout

Signal Name	Pin No.	BANK	I/O Level
TP2	75	1	3.3V
TP3	74	1	3.3V
TP4	73	1	3.3V
TP5	71	1	3.3V
TP6	69	1	3.3V

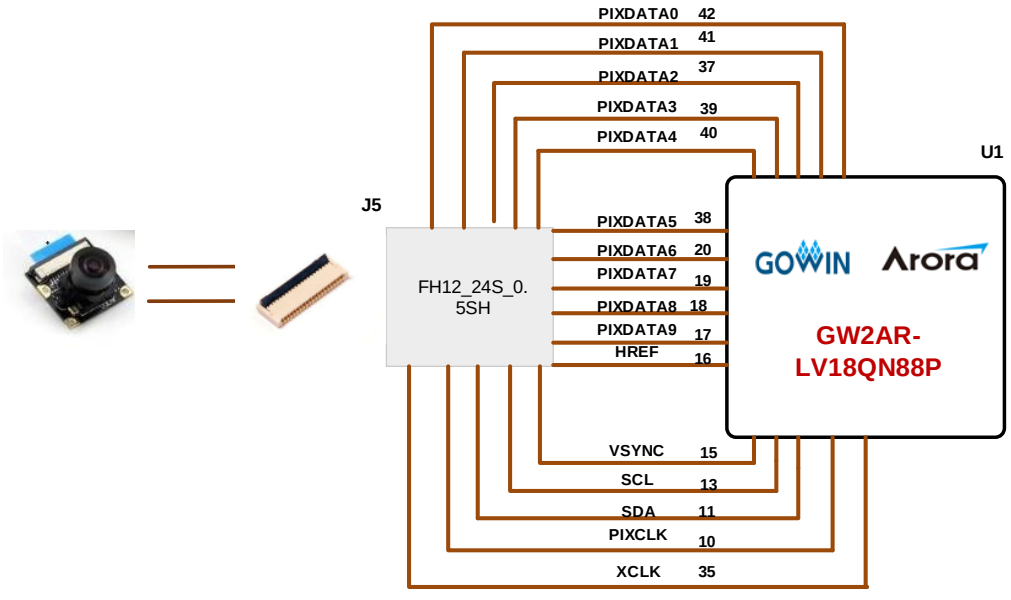
3.7 FPC connector

3.7.1 Overview

To facilitate users to input camera signal to FPGA, 24PIN FPC connector (FH12-24S-0.5SH) is reserved on the development board.

3.7.2 FPC Circuit

Figure 3-5 FPC Circuit



3.7.3 Pinout

Table 3-6 FPC Pinout

Socket Pin No.	Signal Name	Pin No.	BANK	Description	I/O Level
1	STROBE	-	-	Flash control signal	-
2	GND	-	-	GND	-
3	SDA	11	6	SCCB serial interface data	3.3V
4	AVDD	-	-	Analog signal power supply	2.8V
5	SCL	13	6	SCCB serial interface clock	3.3V
6	RST_N	-	-	Reset signal	-
7	VSYNC	15	6	Vertical Sync output	3.3V
8	PWDN	-	-	Power-down mode enable signal	-
9	HREF	16	6	Horizontal reference output	3.3V
10	SVDD	-	-	Sensor array power supply	1.2V
11	DOVDD	-	-	Digital image signal power supply	3.3V
12	PIXDATA9	17	6	Video output channel 9	3.3V
13	XCLK	35	4	System clock input	3.3V
14	PIXDATA8	18	6	Video output channel 8	3.3V
15	GND	-	-	GND	-
16	PIXDATA7	19	6	Video output channel 7	3.3V
17	PIXCLK	10	6	Pixel clock output	3.3V
18	PIXDATA6	20	6	Video output channel 6	3.3V
19	PIXDATA2	37	4	Video output channel 2	3.3V
20	PIXDATA5	38	4	Video output channel 5	3.3V
21	PIXDATA3	39	4	Video output channel 3	3.3V
22	PIXDATA4	40	4	Video output channel 4	3.3V
23	PIXDATA1	41	4	Video output channel 1	3.3V
24	PIXDATA0	42	4	Video output channel 0	3.3V

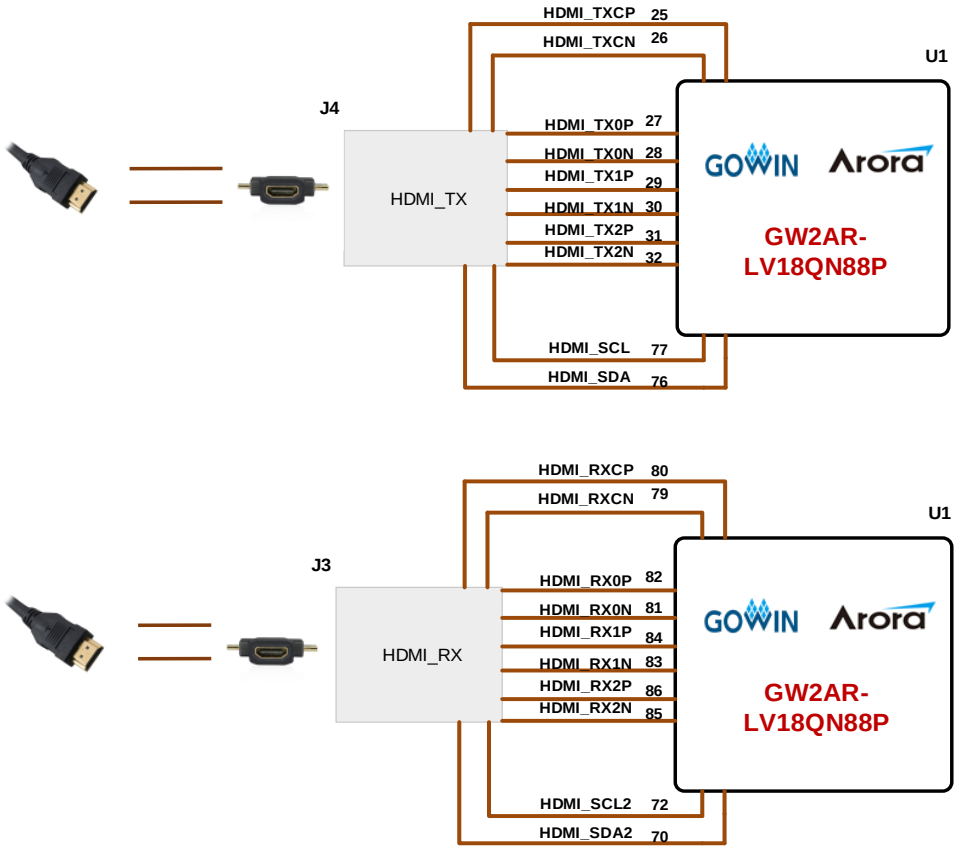
3.8 HDMI

3.8.1 Overview

To facilitate users to input image to FPGA and output after FPGA image processing, one HDMI RX interface and one HDMI TX interface are reserved.

3.8.2 HDMI Circuit

Figure 3-6 HDMI Connection Diagram



3.8.3 Pinout

Table 3-7 HDMI_TX Pinout

Signal Name	Pin No.	BANK	Description	I/O Level
HDMI_TXCP	25	5	TMDS Clock signal +	2.5V
HDMI_TXCN	26	5	TMDS clock signal -	2.5V
HDMI_TX0P	27	5	TMDS data 0 +	2.5V
HDMI_TX0N	28	5	TMDS data 0 -	2.5V
HDMI_TX1P	29	5	TMDS data 1 +	2.5V
HDMI_TX1N	30	5	TMDS data 1 -	2.5V
HDMI_TX2P	31	5	TMDS data 2 +	2.5V
HDMI_TX2N	32	5	TMDS data 2 -	2.5V
HDMI_SCL	77	1	DDC clock line	3.3V
HDMI_SDA	76	1	DDC Cable	3.3V

Table 3-8 HDMI_RX Pinout

Signal Name	Pin No.	BANK	Description	I/O Level
HDMI_RXCP	80	0	TMDS Clock signal +	2.5V
HDMI_RXCN	79	0	TMDS clock signal -	2.5V
HDMI_RX0P	82	0	TMDS data 0 +	2.5V
HDMI_RX0N	81	0	TMDS data 0 -	2.5V
HDMI_RX1P	84	0	TMDS data 1 +	2.5V
HDMI_RX1N	83	0	TMDS data 1 -	2.5V
HDMI_RX2P	86	0	TMDS data 2 +	2.5V
HDMI_RX2N	85	0	TMDS data 2 -	2.5V
HDMI_SCL2	72	1	DDC clock line	3.3V
HDMI_SDA2	70	1	DDC Cable	3.3V

4 Considerations

Considerations for the use of development board:

1. Handle with care and pay attention to electrostatic protection.
2. The PWDN interface of the camera is not connected to the GW2AR-18 device.
3. For the device of GW2AR-18, PSRAM power supply is provided via VCCO2/7 Bank voltage.
4. Since the development board MODE port is grounded, the MODE is fixed and cannot be changed.
5. The 27MHZ clock of the development board is provided to the GW2AR-18 device and the 12MHZ clock is provided to the USB to JTAG chip (FT232HL).

5 Gowin Software

See SUG100, *Gowin Software User Guide* for details.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