MJB_V1.2

User Guide

MDBUG1051-1.0.1E, 02/22/2024

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Revision History

Date	Version	Description
12/02/2022	1.0E	Initial version published.
02/22/2024	1.0.1E	The description of Chapter 4 optimized.

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1 About This Guide

1.1 Purpose

The MJB_V1.2 development board (hereinafter referred to development board) user guide consists of following three parts:

- A brief introduction to the features of the development board.
- An introduction to the development board system architecture and hardware resources
- An introduction to the hardware circuits, functions and pinout

1.2 Supported Products

The information presented in this guide applies to GW2AR-LV18QN88P device.

1.3 Related Documents

You can find related documents at magicjellybeanfpga.github.

1.4 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
BSRAM	Block Static Random Access Memory
DDR	Double Data Rate
DSP	Digital Signal Processing
FLASH	Flash Memory

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
LDO	Low Dropout Regulator
LUT4	Four-input Look-up Table
LVDS	Low-Voltage Differential Signaling
MJB	Magic Jelly Bean
SSRAM	Shadow Static Random Access Memory

1.5 Support and Feedback

Magic Jelly Bean Organization provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

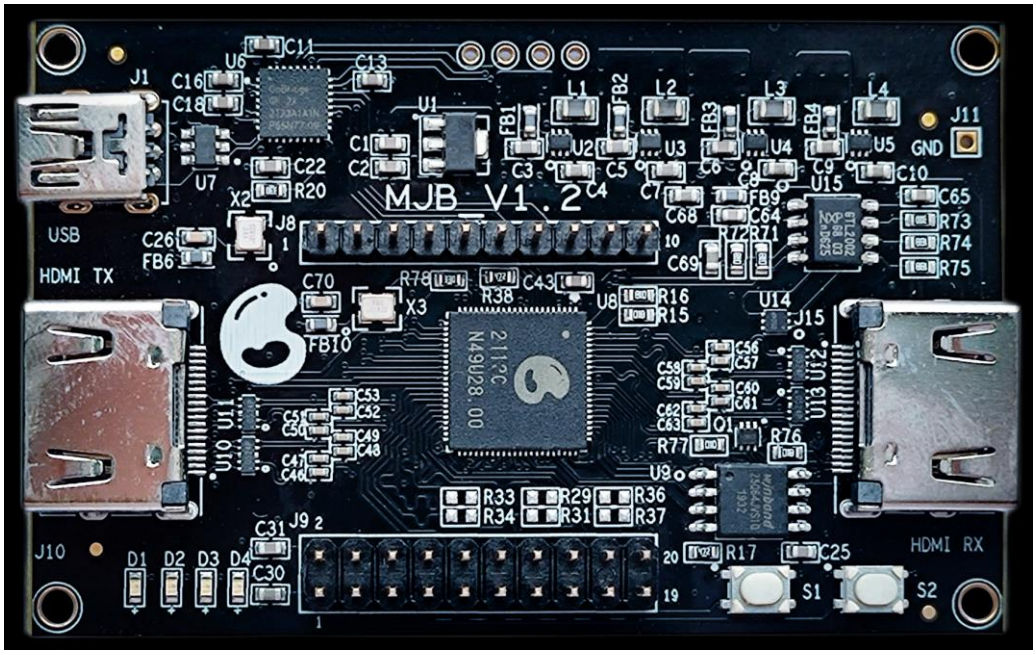
Website: magicjellybeanfpga.github

E-mail: admin@magicjellybean.org

2 Development Board Introduction

2.1 Overview

Figure 2-1 MJB_V1.2 Development Board



MJB_V1.2 development board uses Gowin GW2AR-18 FPGA devices embedded with 64 Mbit PSRAM, The GW2AR series of FPGA products are the first generation products of the Arora® family. They offer a SIP chip. The main difference between the GW2A series and the GW2AR series is that the GW2AR series integrates abundant memories. The GW2AR series also provides high-performance DSP resources, high-speed LVDS interfaces, and abundant BSRAM resources. These embedded resources in combination with a streamlined FPGA architecture with 55nm process make the GW2AR series of FPGA products suitable for high-speed and low-cost applications.

MJB_V1.2 development board adopts Micro USB interface for easy and reliable connection, which facilitates applying to various IoT hardware terminal occasions. MJB_V1.2 development board can work independently as the smallest system, or can be used together with MJB Mic daughter card, MJB Accelerometer daughter card or MJB Camera daughter card. MJB_V1.2 development board provides 2 HDMIs as receive and transmit interface, which can input/output 720P images at maximum. The development board provides one 10Pin single-row pin with 2.54mm pitch and one 20Pin double-row pin with 2.54mm pitch as the input interface for MJB daughter card or other devices.

2.2 MJB Daughter Card

2.2.1 MJB_Mic

MJB_Mic daughter card provides the sound capture function for the MJB_V1.2 development board.

The MJB_Mic daughter card is connected to the MJB_V1.2 development board through a pin header, which can be connected according to the pin socket and pin header.

The daughter card provides 2 MEMS microphones with I2S interface and 8 LEDs.

2.2.2 MJB_Camera_V2.1

MJB_Camera_V2.1 daughter card provides the camera function for the MJB_V1.2 development board.

The MJB_Camera_V2.1 daughter card is connected to the MJB_V1.2 development board through a pin header, which can be connected according to the pin socket and pin header.

The daughter card provides 1 DC/DC converter (3.3V to 2.8V) and 5 LEDs.

2.2.3 MJB_Accelerometer

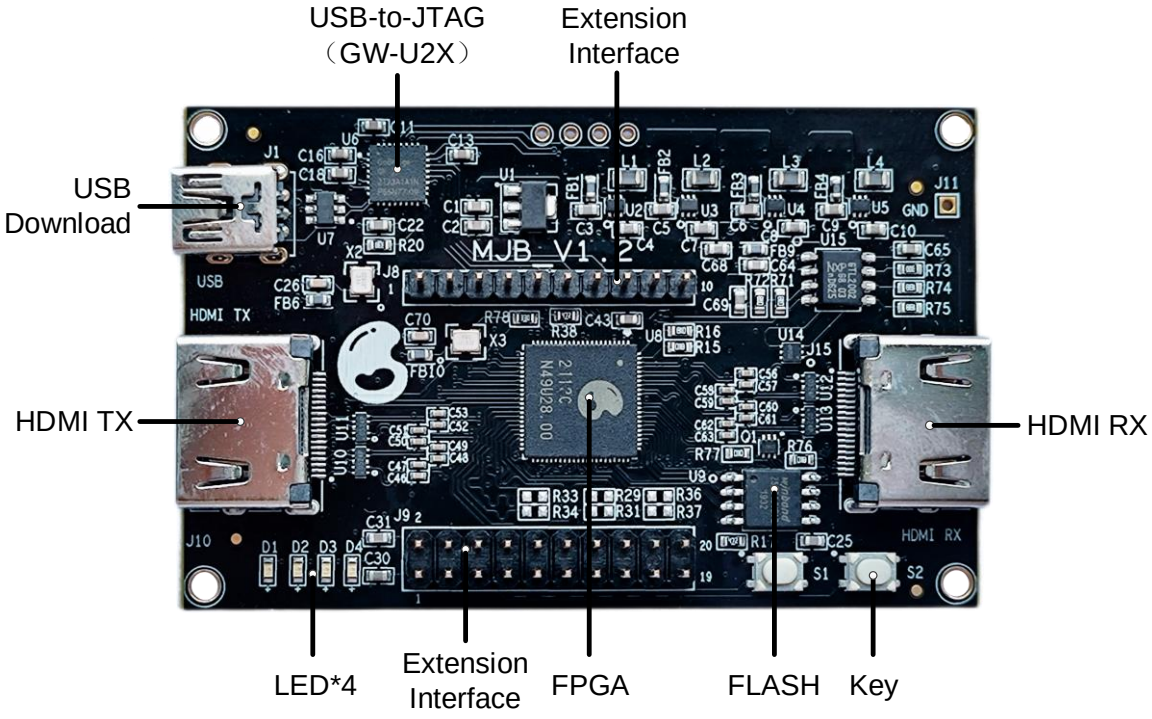
MJB_Accelerometer daughter card provides the speed detection function for the MJB_V1.2 development board.

The MJB_Accelerometer daughter card is connected to the MJB_V1.2 development board through a pin header, which can be connected according to the pin socket and pin header.

The daughter card provides 1 accelerometer with I2S interface and 8 LEDs.

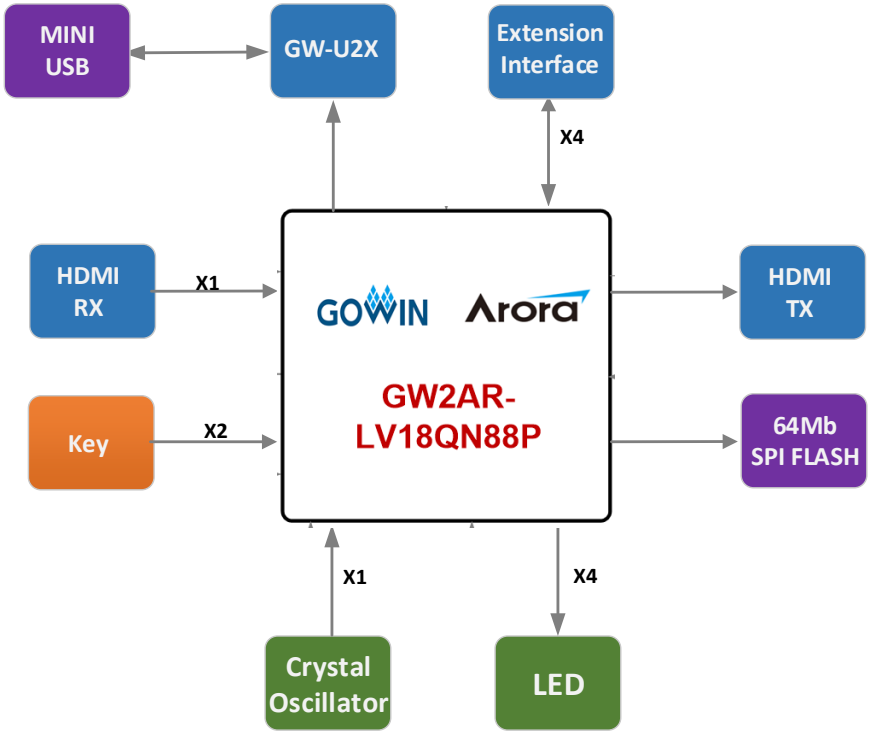
2.3 PCB Components

Figure 2-2 PCB Components



2.4 System Block Diagram

Figure 2-3 System Block Diagram



2.5 Features

The structure and features of the development board are as follows:

1. FPGA
   - QN88 package
   - Up to 66 user I/Os
   - Abundant LUT4 resources
   - Multiple modes and capacities of B-SRAM
2. FPGA configuration modes
   - JTAG
   - MSPI
3. Clock resource

   12MHz Clock Crystal Oscillator
4. Key

   2 keys
5. LED

   4 LEDs
6. Memory
   - 64Mbit embedded PSRAM
   - 64Mbit external SPI flash
7. GPIO

   16 I/O expansion resources
8. MIPI

   1 MIPI interface (1clk+2data)
9. HDMI
   - 1 HDMI TX Interface
   - 1 HDMI RX Interface
10. Extension Interface of Core Board

    It can connect to Gowin core boards (microphone core board, camera core board, etc.)
11. DC-DC (LDO) Power

    Provides 3.3 V, 2.8V, 2.5V, 1.8V,1.2V and 1.0V power supply

3 Development Board Circuit

3.1 FPGA Module

Overview

For the resources of GW2AR series of FPGA Products, see *DS226, GW2AR Series of FPGA Products Data Sheet*.

I/O BANK Introduction

For the I/O BANK, package, and pinout information, see *UG229 GW2AR Series of FPGA Products Package and Pinout User Guide*.

3.2 Download Module

3.2.1 Overview

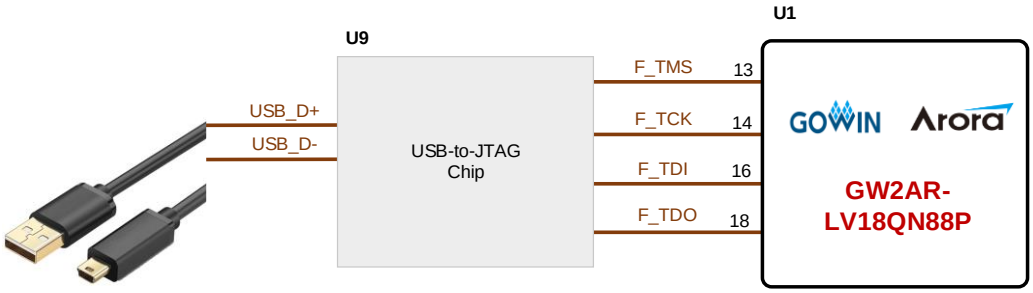
The development board provides a USB download interface. The bitstream file can be downloaded to the internal SRAM or the external SPI flash as needed.

Note!

- When downloaded to SRAM, the data stream file will be lost if the device is powered down, and it will need to be downloaded again after power-on.
- If downloaded to SPI flash, the data stream file will not be lost if the device is powered down.

3.2.2 USB Download Circuit

Figure 3-1 FPGA USB Download Connection Diagram



3.2.3 Download Process

1. FPGA SRAM Download Mode:

   Plug the USB cable to the USB interface (J1) on the development board. Power on. Open the Programmer, select SRAM mode, and then select the bitstream file you required.

2. FPGA MSPI Download Mode:

   Plug the USB cable to the USB interface (J1) on the development board, then power on. Open the Programmer, select External Flash mode, and then select the bitstream file and FLASH you required. Turn off the power after downloading. Power on, and then the device will import the bitstream file to SRAM from the external Flash.

3.2.4 Pinout

Table 3-1 FPGA Download and Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
TCK	6	2	1.8V	JTAG Signal
TDO	8	2	1.8V	JTAG Signal
TDI	7	2	1.8V	JTAG Signal
TMS	5	2	1.8V	JTAG Signal

3.3 Power Supply

3.3.1 Overview

DC5V is input by USB interface. The TI LDO and ONSEMI DC-DC power supply chip are used to step down voltage from 5V to 3.3V, 2.8V, 2.5V, 1.8V, 1.2V and 1.0V, which can meet the power demands of the development board.

3.3.2 FPGA Power Supply Pinout

Table 3-2 FPGA Power Supply Pinout

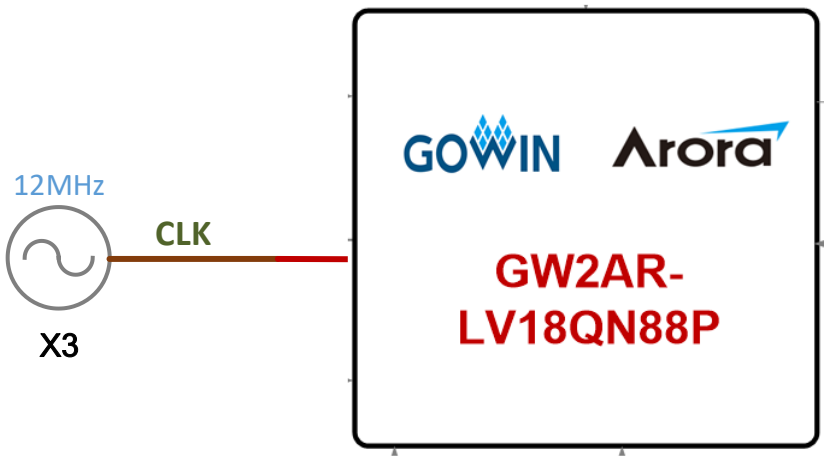
Signal Name	Pin No.	BANK	Description	I/O Level
VCCIO0	78	0	I/O Bank Voltage	2.5V
VCCIO1	12, 67	1	I/O Bank Voltage	2.5V
VCCIO2	3, 64	2	I/O Bank Voltage	1.8V
VCCIO3	58	3	I/O Bank Voltage	2.5V
VCCIO4	44	4	I/O Bank Voltage	1.2V
VCCIO5	23	5	I/O Bank Voltage	2.5V
VCCIO6	12, 67	6	I/O Bank Voltage	2.5V
VCCIO7	3, 64	7	I/O Bank Voltage	1.8V
VCCPLLL1	14	-	PLLL1 power	1.0V
VCCPLLR1	50	-	PLLL1 power supply	1.0V
VCCX	12, 67	-	Auxiliary voltage are internally connected to VCCO1 and VCCO6	2.5V
VCC	1, 22, 45, 66	-	Core voltage	1.0V
VSS	2, 21, 24, 43, 46, 65, 68	-	GND	

3.4 Clock and Reset

3.4.1 Overview

The development board provides a 12MHz crystal oscillator connected to the PLL input pin. This can be employed as the input clock for the PLL in FPGA. Frequency division and multiplication of PLL can output the clock required by the user.

Figure 3-2 Clock and Reset Connection Diagram



3.4.2 Pinout

Table 3-3 Clock and Reset Pinout

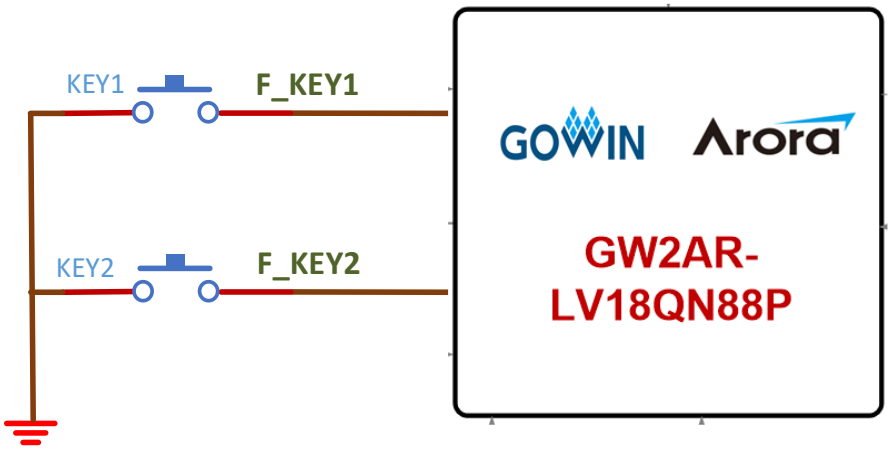
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
FPGA_18KCLK_12M	13	6	2.5V	27MHz active crystal oscillator input

3.5 Key

3.5.1 Overview

To facilitate the extension and testing for user functions, two keys are reserved on the development board.

Figure 3-3 Key Circuit Diagram



3.5.2 Pinout

Table 3-4 Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_KEY1	36	2	1.2V	KEY1
F_KEY2	35	2	1.2V	KEY2

3.6 LED

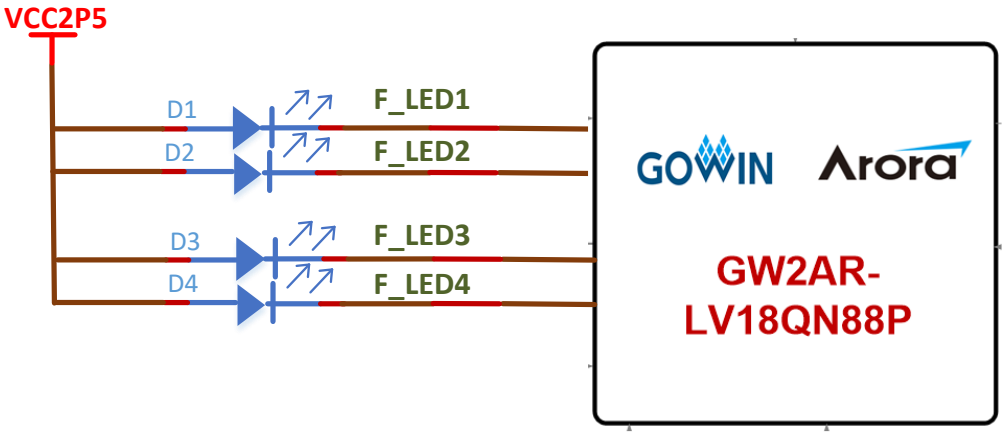
3.6.1 Overview

There are four LEDs in the development board and users can display the required status through the LEDs.

You can test the LEDs in the following ways:

- When the FPGA corresponding pin output signal is logic low, the LED is lit.
- If the signal is high, LED is off.

Figure 3-4 LED Circuit



3.6.2 Pinout

Table 3-5 Ethernet Pinout

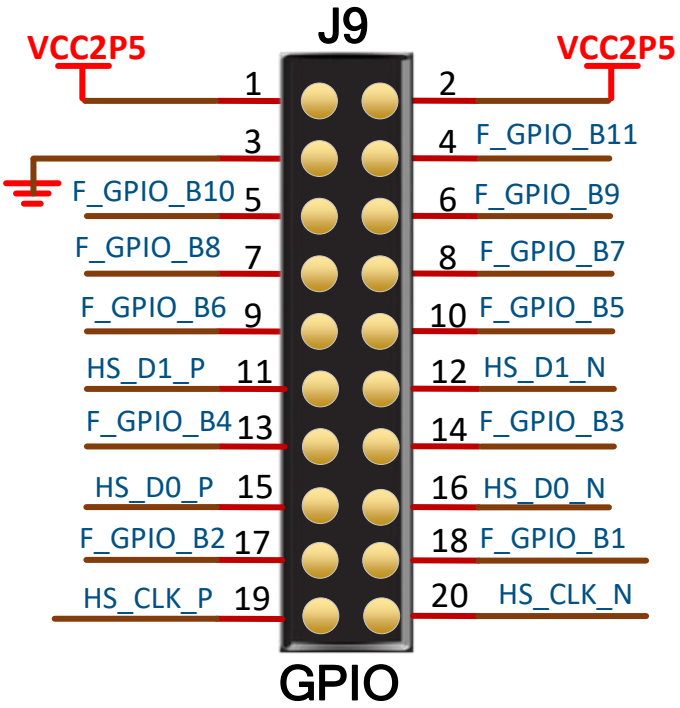
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_LED1	4	7	1.8V	LED1
F_LED2	20	6	2.5V	LED2
F_LED3	33	5	2.5V	LED3
F_LED4	34	5	2.5V	LED4

3.7 MIPI Interface

3.7.1 Introduction

To facilitate the extension and testing for user functions, 1 MIPI interface is reserved on the development board. The MIPI interface is one clk channel and two data channels (Share a set of pins with GPIO).

Figure 3-5 MIPI Interface Connection Diagram



3.7.2 Pinout

Table 3-6 MIPI Interface Pinout

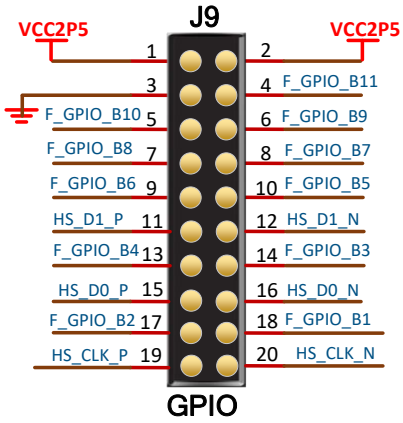
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
HS_CLK_P	77	1	2.5V	CLK signal line+
HS_CLK_N	76	1	2.5V	CLK signal line-
HS_D0_P	75	1	2.5V	DATA0 signal line+
HS_D0_N	74	1	2.5V	DATA0 signal line-
HS_D1_P	73	1	2.5V	DATA1 signal line+
HS_D1_N	72	1	2.5V	DATA1 signal line-

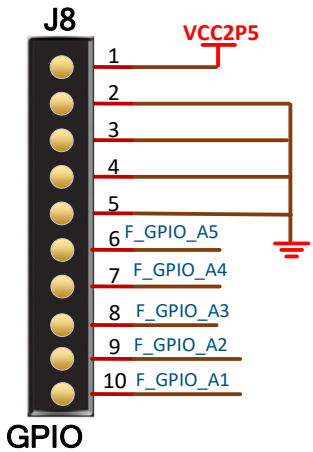
3.8 GPIO

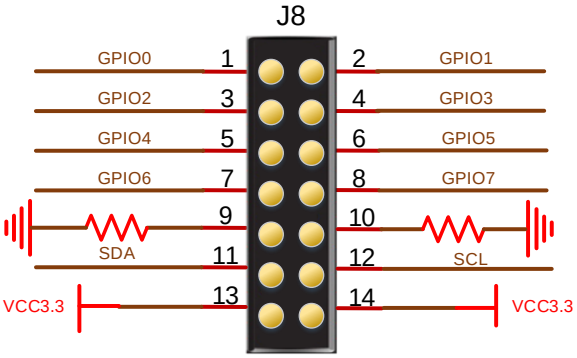
3.8.1 Introduction

The development board leads to two sets of pins (J8, J9), a set of 20Pin pins (J9), a total of 11 common GPIOs, a set of 1CLK+2DATA MIPI interface, a set of 10Pin pins (J8), a total of 5 common GPIOs. You can choose according to your needs.

Figure 3-6 GPIO Pin Header Connection Diagram







3.8.2 Pinout

Table 3-7 J5 Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_GPIO_A1	15	6	2.5V	General-purpose input/output
F_GPIO_A2	16	6	2.5V	General-purpose input/output
F_GPIO_A3	17	6	2.5V	General-purpose input/output
F_GPIO_A4	18	6	2.5V	General-purpose input/output
F_GPIO_A5	19	6	2.5V	General-purpose input/output
F_GPIO_B1	70	1	2.5V	General-purpose input/output
F_GPIO_B2	69	1	2.5V	General-purpose input/output
F_GPIO_B3	55	3	2.5V	General-purpose input/output
F_GPIO_B4	71	1	2.5V	General-purpose input/output
F_GPIO_B5	54	3	2.5V	General-purpose input/output
F_GPIO_B6	56	3	2.5V	General-purpose input/output
F_GPIO_B7	52	3	2.5V	General-purpose input/output
F_GPIO_B8	53	3	2.5V	General-purpose input/output
F_GPIO_B9	49	3	2.5V	General-purpose input/output
F_GPIO_B10	51	3	2.5V	General-purpose input/output
F_GPIO_B11	48	3	2.5V	General-purpose input/output

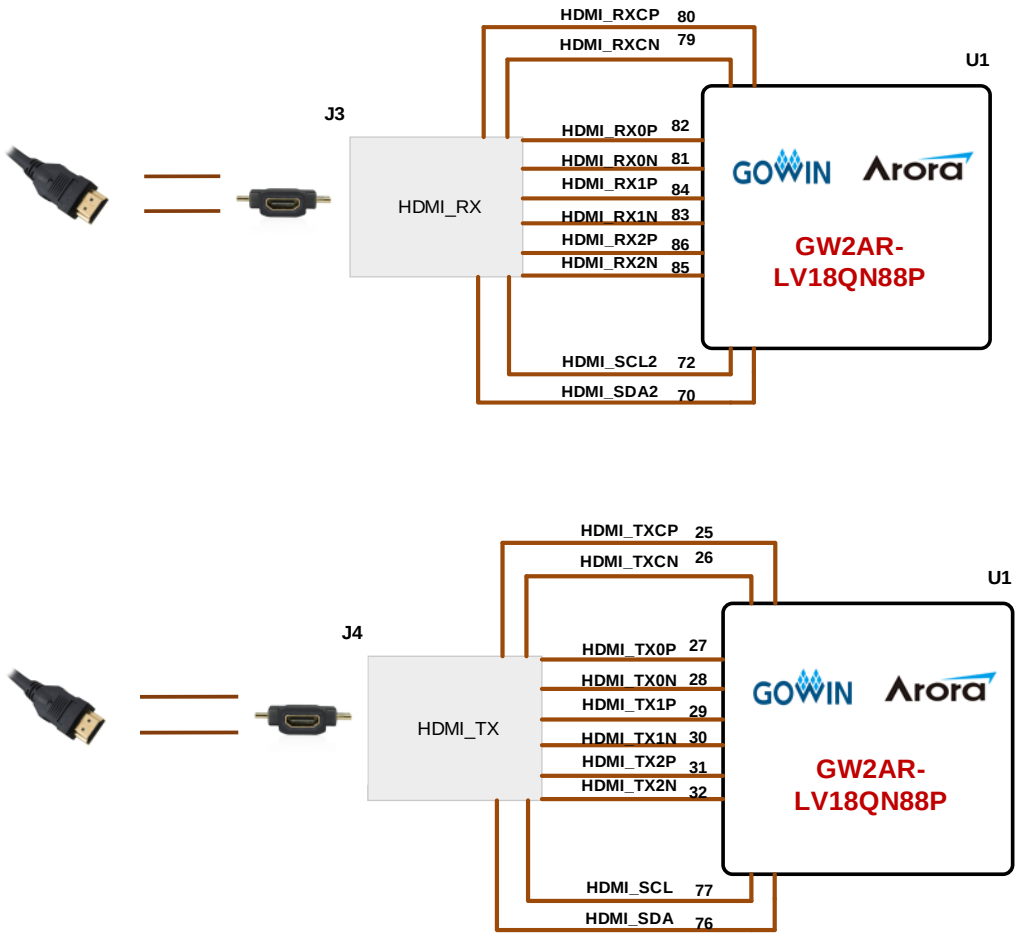
3.9 HDMI

3.9.1 Overview

To facilitate you to input image to FPGA and output after FPGA image processing, one HDMI RX interface and one HDMI TX interface are reserved.

3.9.2 HDMI Circuit

Figure 3-7 HDMI Connection Diagram



3.9.3 Pinout

Table 3-8 HDMI_TX Pinout

Signal Name	Pin No.	BANK	Description	I/O Level
HDMI_TXCP	25	5	TMDS clock signal+	2.5V
HDMI_TXCN	26	5	TMDS clock signal-	2.5V
HDMI_TX0P	27	5	TMDS data 0+	2.5V
HDMI_TX0N	28	5	TMDS data 0-	2.5V
HDMI_TX1P	29	5	TMDS data 1+	2.5V
HDMI_TX1N	30	5	TMDS data 1-	2.5V
HDMI_TX2P	31	5	TMDS data 2+	2.5V
HDMI_TX2N	32	5	TMDS data 2-	2.5V

Table 3-9 HDMI_RX Pinout

Signal Name	Pin No.	BANK	Description	I/O Level
HDMI_RXCP	80	0	TMDS clock signal+	2.5V
HDMI_RXCN	79	0	TMDS clock signal-	2.5V
HDMI_RX0P	82	0	TMDS data 0+	2.5V
HDMI_RX0N	81	0	TMDS data 0-	2.5V
HDMI_RX1P	84	0	TMDS data 1+	2.5V
HDMI_RX1N	83	0	TMDS data 1-	2.5V
HDMI_RX2P	86	0	TMDS data 2+	2.5V
HDMI_RX2N	85	0	TMDS data 2-	2.5V
HDMI_SCL2	10	6	DDC clock line	2.5V
HDMI_SDA2	11	6	DDC data line	2.5V

4 MJB Software

Please refer to *MUG100, MJB Software User Guide* for details.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