# MiniStar nano Experiment Kit

# User Guide

**DBUG409-1.1E, 04/24/2022**

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## Revision History

| Date | Version | Description |
|---|---|---|
| 04/24/2022 | 1.1E | Initial version published |

# Contents

# List of Figures

# List of Tables

# 1 About This Guide

## 1.1 Purpose

MiniStar nano Experiment Kit user guide consists of the following three parts:

1. A brief introduction to the features and hardware resources of the development board.
2. An introduction to the functions, circuits, and pinout of each module.
3. Notes for the use of development board.

## 1.2 Supported Products

The information in the guide applies to GW1NSR series of FPGA product: GW1NSR-LV4CQN48P.

## 1.3 Related Documents

The latest user guides are available on the Gowin Website. You can find the related documents at www.gowinsemi.com:

- DS861, GWINSR series of FPGA Products Data Sheet
- UG863, GWINSR series of FPGA Products Package and Pinout Manual
- UG864, GW1NSR-4 Pinout
- UG290, Gowin FPGA Products Programming and Configuration Guide
- SUG100, Gowin Software User Guide

## 1.4 Terminology and Abbreviations

The abbreviations and terminology used in this manual are as shown in Table 1- 1 below.

**Table 1-1 Terminology and Abbreviations**

| Terminology and Abbreviations | Meaning |
|---|---|
| FPGA | Field Programmable Gate Array |
| LED | Light Emitting Diode |
| LDO | Low Dropout Regulator |
| GPIO | General Purpose Input Output |
| LUT4 | Four-input Look-up Table |
| SSRAM | Shadow Static Random Access Memory |
| BSRAM | Block Static Random Access Memory |
| PLL | Phase-locked Loop |
| DLL | Delay-locked Loop |
| DSP | Digital Signal Processing |
| QN48P | QN48P |

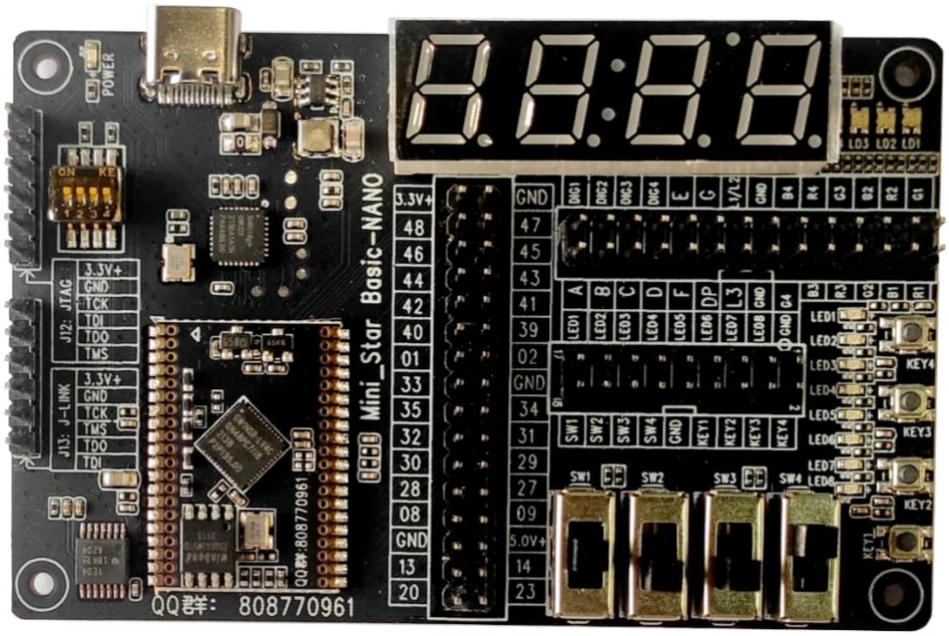
## 1.5 Technical Support

1. For the latest FPGA technical information, please pay attention to WeChat official account: MYMNIEYE.
2. Instruction video link: https://space.bilibili.com/507416742.
3. Taobao shop: MYMNIEYE.
4. Technical support QQ group: 808770961.

# 2 Development Board Introduction

## 2.1 Overview

**Figure 2-1 MiniStar nano Experiment Kit**




The MiniStar nano Experiment Kit is based on Gowin GW1NSR series of FPGA product GW1NSR-LV4CQN48P.

GW1NSR series of FPGA products are the first-generation products of LittleBee® family and represent one form of SIP chips, which integrates GW1NS series of FPGA product and PSRAM. GW1NSR series of FPGA products include GW1NSR-2C, GW1NSR-4C, GW1NSR-2, and GW1NSR-4 devices. GW1NSR-2C and GW1NSR-4C devices are embedded with ARM Cortex-M3 hardcore processor. In addition, the GW1NSR series of FPGA products are also embedded with USB2.0 PHY, User Flash, and ADC.

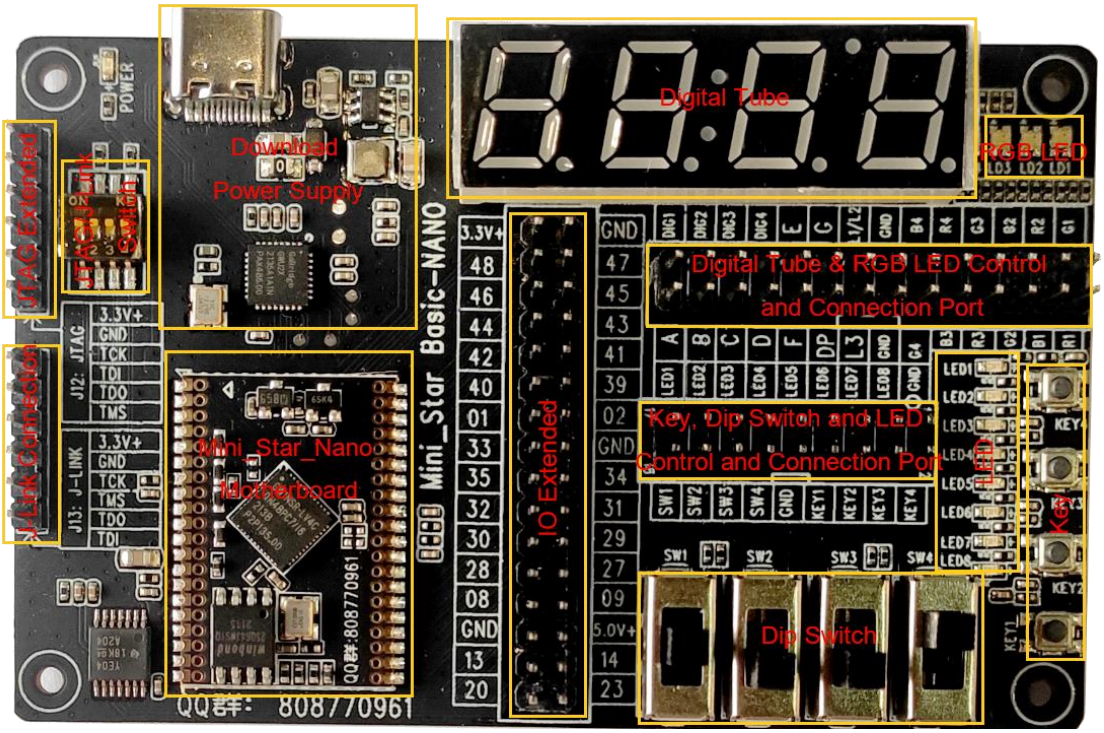
ARM Cortex-M3 hardcore processor is employed as the core of GW1NSR-2C and GW1NSR-4C devices, and the needs of the minimum memory can be met. FPGA logic resources and other embedded resources can flexibly facilitate the peripheral control functions, which provide excellent calculation functions and exceptional system response interrupts. They also offer high performance, low power, flexible use, instant start-on, low cost, nonvolatile, high security, and abundant package types, etc.. GW1NSR-2C can achieve seamless connection between programmable logic devices and embedded processors. They are compatible with multiple peripheral device standards, which can reduce costs and can be widely deployed in industrial control, communication, Internet of Things, servo drive, consumption fields, etc.

## 2.2 Development Kit

A development board kit includes the following items:

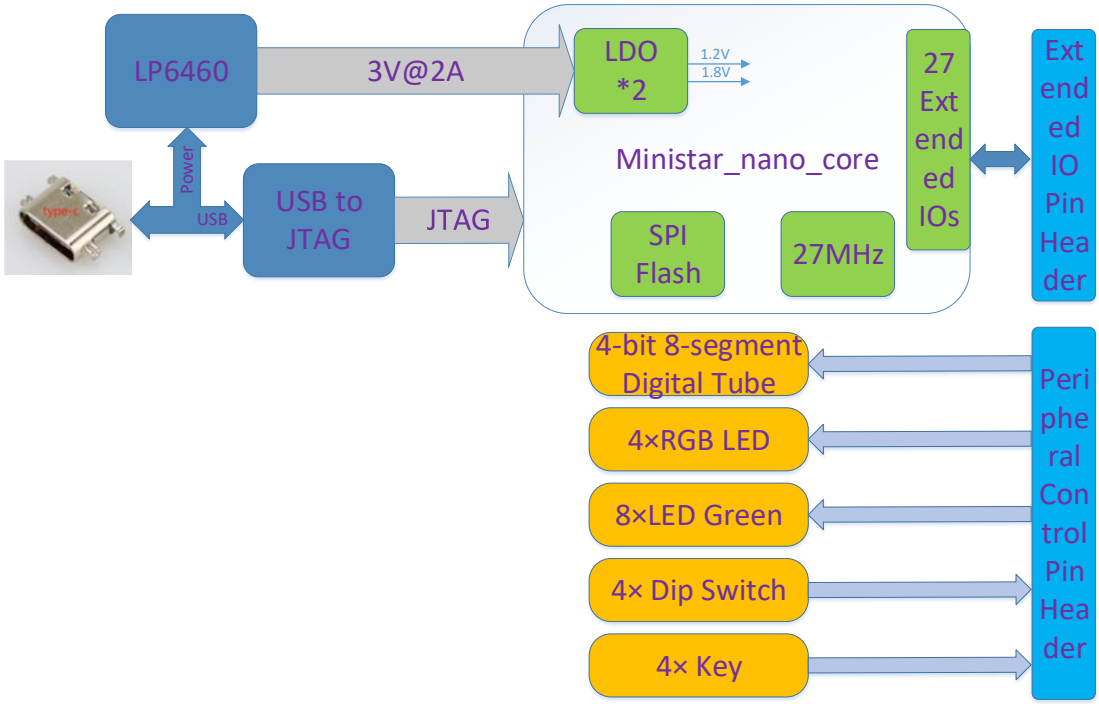
- Development Board
- Development Board User Guide

**Figure 2-2 MiniStar nano Experiment Kit Function Interfaces**



## 2.3 System Block Diagram

**Figure 2-3 MiniStar nano Experiment Kit System Block Diagram**




## 2.4 Features

The structure and features of the development board are as follows:

1. FPGA
   - QN48P package
   - Embedded ARM Cortex-M3 hardcore processor
2. FPGA configuration mode
   - JTAG
   - Internal Flash
3. Clock resource
   - 27MHz clock crystal oscillator
4. Memory
   - External 64 Mbit SPI Flash
   - Embedded 256 Kbit User Flash
5. Key
   - Four keys
6. LED

- One power indicator (green)
- Eight user indicators (green)

7. Digital tube
   - One 4-bit 8-segment digital tube
8. RGB LED
   - Four RGB LEDs
9. Dip switch
   - Four dip switches
10. JTAG extended
    - 6-pin header
11. J-Link input
    - 6-pin header
12. Power Supply
    - Inverse voltage protection
    - 5V supported

## 2.5 Development Board Specification

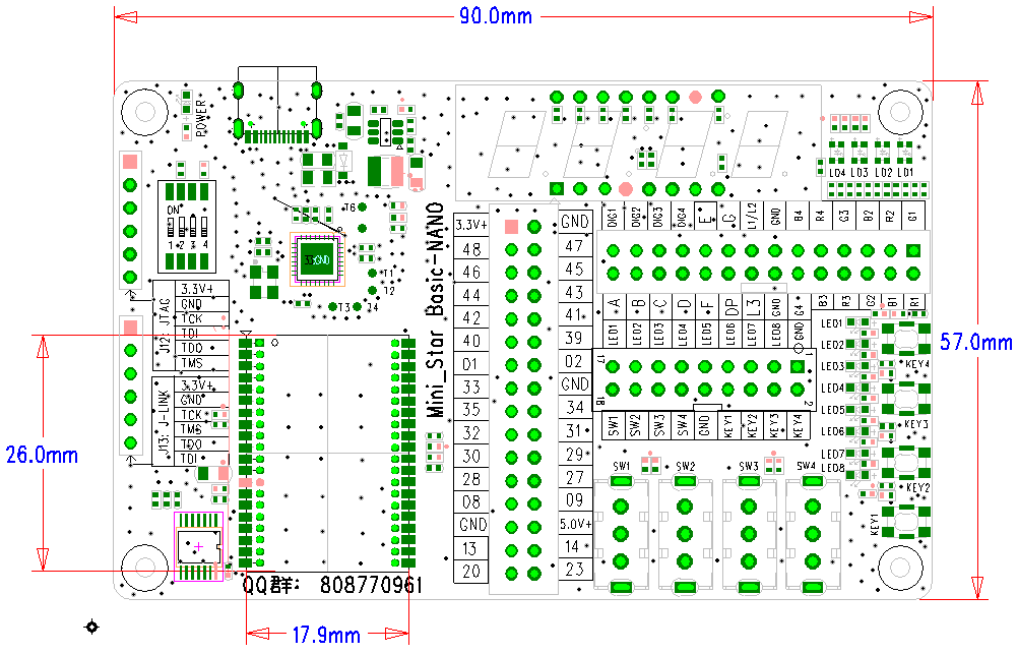
**Table 2-1 MiniStar nano Experiment Kit Specification**

| No. | Item | Parameter | Functional Description |
|---|---|---|---|
| 1 | 5V power supply and download | 5V DC-DC<br>Type-C USB | 5V power supply; USB to JTAG interface |
| 2 | External Flash | 64 Mbit Flash | SPI Flash |
| 3 | Clock | One 27MHz clock | Provides 27MHz clock for FPGA |
| 4 | Extended IO | 2.54 pitch pin header | 27 extended IOs can be connected to on-board peripherals or external interfaces. |
| 5 | Key | Four keys | After connecting the key control port with the FPGA extended IO, it can be used as a test control input. When the key is pressed, it is low. |
| 6 | Indicator | 8 LED indicators | After connecting the LED control port to the FPGA extended IO, the LED will be lit when the FPGA outputs the corresponding pin signal in low level. |
| 7 | RGB LED | Four RGB LEDs | After connecting the RGB port with the FPGA extended IO, the FPGA will control |

| No. | Item | Parameter | Functional Description |
|---|---|---|---|
| | | | the corresponding pins to change the display RGB status. |
| 8 | Dip switches | Four dip switches | After connecting the dip switch control port with the FPGA extended IO, it can be used as a test control input. When the key is pressed, it is low. |
| 9 | Digital tube | 4-bit 8-segment digital tube | After connecting the digital tube port with the FPGA extended IO, the FPGA will control the corresponding pins to change the digital tube display. |
| 7 | Operating Temperature | Commercial 0~+ 70℃ | - |
| 8 | Ambient Temperature | 20%~90%, non-condensing. | - |
| 9 | Size | 90mm×57mm | - |
| 10 | PCB specification | White letters on black ground | - |
| 11 | Power supply | 5V/1A, powered by Type-C USB interface. | - |
| 12 | System power | - | - |

## 2.6 Size

**Figure 2-4 MiniStar nano Experiment Kit Size**



# 3 Development Board Circuit

## 3.1 MiniStar nano Motherboard

### 3.1.1 Overview

The resources of GW1NSR-LV4CQN48P FPGA are shown in Table 3-1.

**Table 3-1 GW1NSR-LV4CQN48P Product Resources**

| Device | GW1NSR-4C |
|---|---|
| LUT4 | 4608 |
| Flip-Flop (FF) | 3456 |
| Block Static Random Access Memory<br>BSRAM (bits) | 180% |
| Number of BSRAM<br>BSRAM | 10 |
| User Flash (bits) | 256K |
| HyperRAM(bit) | 64M |
| 18 x 18 Multiplier | 16 |
| Phase-locked Loop (PLLs) | 2 |
| OSC | 1, ±5% accuracy. |
| Hard core processor | Cortex-M3 |
| Number of I/O banks | 4 |
| Max. User I/O | 39 |
| Core voltage | 1.2V |

## 3.1.2 I/O BANK Introduction

There are four I/O Banks in the GW1NSR series of FPGA products. The I/O BANK distribution is as shown in Figure 3-1, and QN48P pin distribution view is as shown in Figure 3-2.

**Figure 3-1 GW1NSR-LV4CQN48P I/O BANK Distribution**

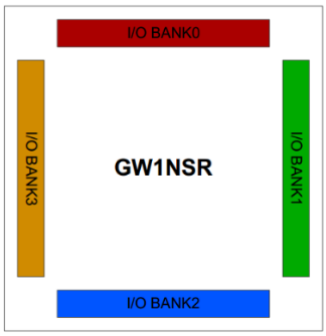
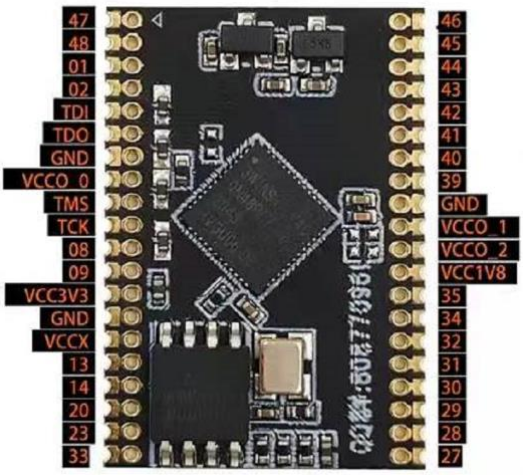



**Figure 3-2 View of GW1NSR-LV4CQN48P Pin Distribution (Top View)**


**Table 3-2 FPGA I/O BANK Voltage and Functions**

| BANK | Voltage | Function | I/O Used | Voltage |
|---|---|---|---|---|
| 0 | 3.3V | JTAG | Four GPIOs | VCCO_0 3.3V |
| | | IO Extended | One differential pair and two GPIOs | |
| 1 | 3.3V | IO Extended | Five differential pairs | VCCO_1 3.3V |
| 2 | 3.3V | IO Extended | Four differential pair and one GPIO | VCCO_2 3.3V |
| 3 | 1.8V | 27MHz clock | One GPIO | VCC3V3 1.8V generated by LDO |
| | | IO Extended | Four GPIOs | |
| | | SPI Flash | Five GPIOs | |

Figure 3-3 MiniStar nano Motherboard Pinout



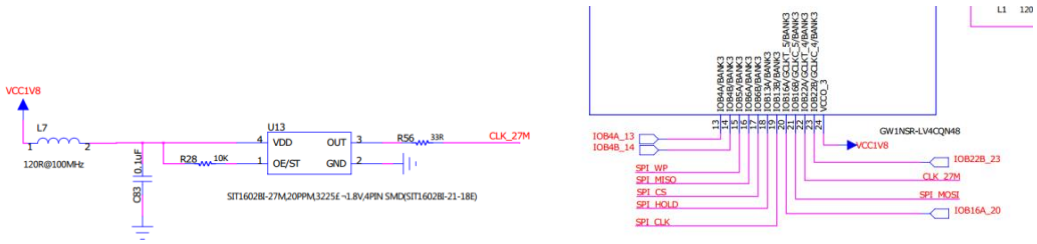

## 3.1.3 Clock

### Overview

The development board provides 27MHz crystal oscillator connecting to the global clock pins.

### Clock Circuit

Figure 3-4 Clock Schematic




### Pinout

Table 3-3 FPGA Clock and Reset Pinout

| Signal Name | Pin No. | BANK | Description | I/O Level |
|---|---|---|---|---|
| CLK_27MHZ_IN | 22 | 3 | 27MHz crystal oscillator Input | 1.8V |

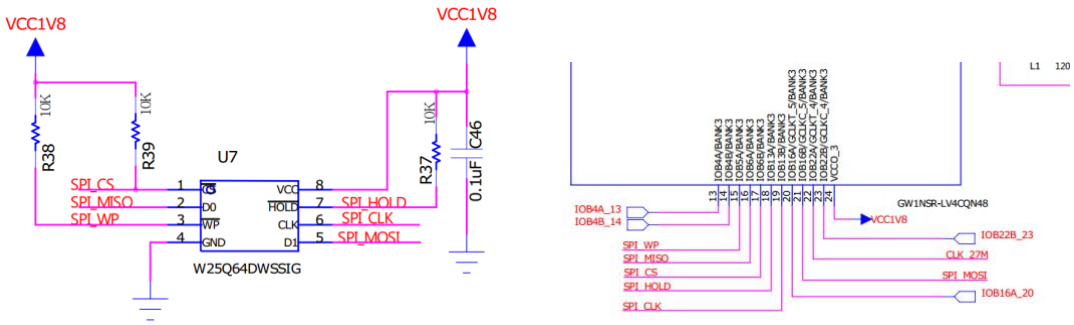
## 3.1.4 Flash

### Overview

The development board provides an external SPI memory (64Mbit and W2564DWSSIG model) for the FPGA.

### Flash Circuit

**Figure 3-5 Flash Connection Schematic**




### Pinout

**Table 3-4 FPGA SPI Flash Pinout**

| Signal Name | Pin No. | BANK | Description | I/O Level |
|---|---|---|---|---|
| SPI_CS | 17 | 3 | SPI chip selection signal | 1.8V |
| SPI_MISO | 16 | 3 | SPI master input slave output signal | 1.8V |
| SPI_WP | 15 | 3 | SPI write protect signal | 1.8V |
| SPI_MOSI | 21 | 3 | SPI master output slave input signal | 1.8V |
| SPI_CLK | 19 | 3 | SPI clock signal | 1.8V |
| SPI_HOLD | 18 | 3 | SPI hold signal | 1.8V |

## 3.1.5 Extended IO

### Overview

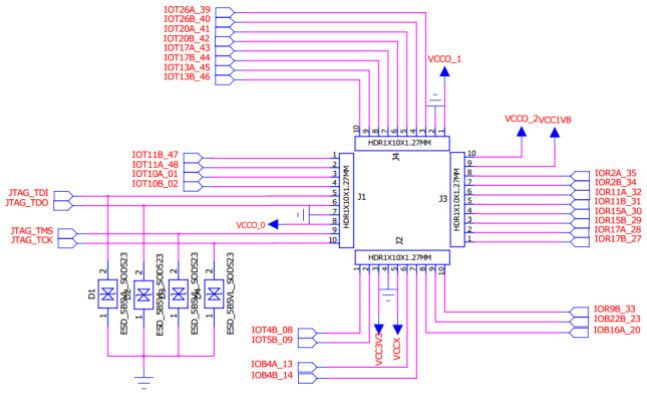
The development board includes four groups of extended IO, which are connected to the outside by four 1.25mm-10P pin headers/stamp holes. The first group includes: Bank0 power input, two pairs of differential pair GPIO, and JTAG interface. The second group includes: DC3.3V power input, two pairs of differential pair GPIO, 3 single-ended GPIOs, auxiliary power VCCX input (recommended to use the highest voltage of bank power supply, and MiniStar nano Experiment Kit provides 3.3V).

The third group includes: Bank2 power input, DC1.8V power output, four pairs of differential pair GPIO of Bank2.

The fourth group includes: Bank1 power input, four pairs of differential pair GPIOs of Bank1.

## Extended IO Schematic

**Figure 3-6 Extended IO Schematic**




## Pinout

**Table 3-5 Extended IO Pinout-5**

| Signal Name | Pin No. | BANK | Description | I/O Level |
|---|---|---|---|---|
| IOT10A_01 | 1 | 0 | Differential Pair | VCCO_0 |
| IOT10B_02 | 2 | 0 | | |
| IOT4B_08 | 8 | 0 | GPIO | |
| IOT5B_09 | 9 | 0 | GPIO | |
| IOR17B_27 | 27 | 2 | Differential Pair | VCCO_2 |
| IOR17A_28 | 28 | 2 | | |
| IOR15B_29 | 29 | 2 | Differential Pair | |
| IOR15A_30 | 30 | 2 | | |
| IOR11B_31 | 31 | 2 | Differential Pair | |
| IOR11A_32 | 32 | 2 | | |
| IOR9B_33 | 33 | 2 | GPIO | |
| IOR2B_34 | 34 | 2 | Differential Pair | |
| IOR2A_35 | 35 | 2 | | |
| T26A_39 | 39 | 1 | Differential Pair | VCCO_1 |
| IOT26B_40 | 40 | 1 | | |
| IOT20A_41 | 41 | 1 | Differential Pair | |
| IOT20B_42 | 42 | 1 | | |
| IOT17A_43 | 43 | 1 | Differential Pair | |
| IOT17B_44 | 44 | 1 | | |
| IOT13A_45 | 45 | 1 | Differential | |

| Signal Name | Pin No. | BANK | Description | I/O Level |
|---|---|---|---|---|
| IOT13B_46 | 46 | 1 | Pair | |
| IOT11B_47 | 47 | 1 | Differential Pair | |
| IOT11A_48 | 48 | 1 | | |
| IOB22B_23 | 23 | 3 | GPIO | 1.8V |
| IOB16A_20 | 20 | 3 | GPIO | |
| IOB4A_13 | 13 | 3 | Differential Pair | |
| IOB4B_14 | 14 | 3 | | |

# 3.2 MiniStar nano Daughterboard

## 3.2.1 Download

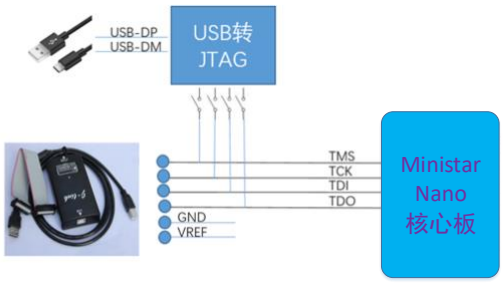
### Overview

The development board provides USB download interface, which is realized by the USB conversion chip. The internal ARM Cortex-M3 hardcore processor is also downloaded through the same IO group. When you need to debug and download the ARM core, you need to keep the USB power supply, and at the same time, toggle the dip switch to disconnect the USB to JTAG module.

The download connection is as show in Figure 3-5.

### USB Download Circuit

**Figure 3-7 FPGA Download Circuit Schematic**




### Pinout

**Table 3-6 Download Circuit Pinout**

| Signal Name | Pin No. | BANK | Description | I/O Level |
|---|---|---|---|---|
| FPGA_ TMS | 6 | 0 | TMS | 3.3V |
| FPGA_ TCK | 7 | 0 | TCK | 3.3V |
| FPGA_ TDI | 3 | 0 | TDI | 3.3V |
| FPGA_ TDO | 4 | 0 | TDO | 3.3V |

## 3.2.2 Power Supply

### Overview

The development board provides DC5V input through the Type-C USB interface, and is equipped with 1.5A overcurrent protection and anti-reverse connection protection.

### Power System Distribution

**Figure 3-8 Power Circuit**


## 3.2.3 LED

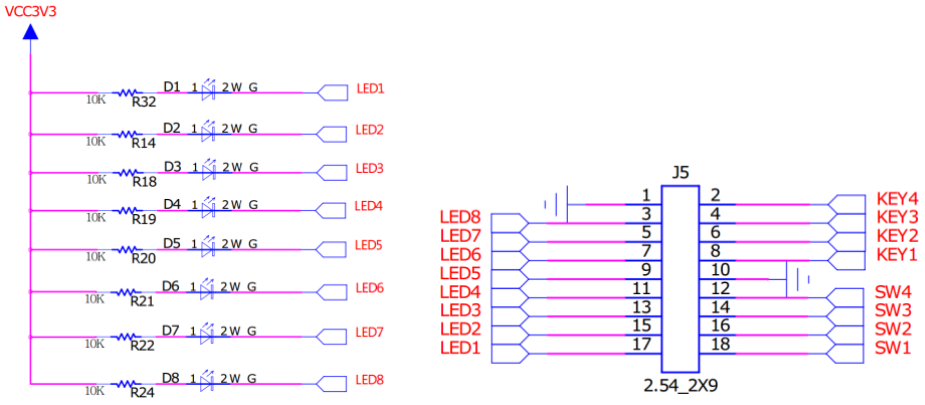
### Overview

There are eight LEDs in the development board and they can display the required status. After connecting the control connector of the LED with the extended IO connector, the LED can be tested in the following ways.

- When the output signal of the corresponding pin of the FPGA is in high level, the LED is off;
- If the output signal is low, LED is on.

### LED Circuit

**Figure 3-9 LED Circuit Schematic**




### Pinout

There are user-extended IOs on the development board that can be connected if needed. Connect the LED-related control ports on the J5 connector to the corresponding IOs on the extended IO connector J2 with

Dupont cables, the IOs are assigned to the LED.

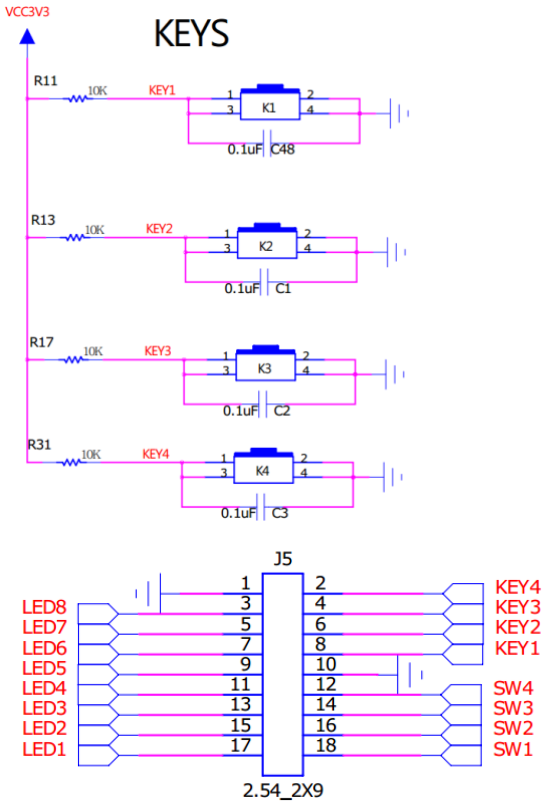
## 3.2.4 Key

### Overview

There are four keys in the development board. Users can manually input low level to the corresponding FPGA pins for testing purposes. When the key is pressed, it is set to low.

### Key Circuit

**Figure 3-10 Key Circuit Schematic**




### Pinout

There are user-extended IOs on the development board that can be connected if needed. Connect the key-related control ports on the J5 connector to the corresponding IOs on the extended IO connector J2 with Dupont cables, the IOs are assigned to the key.

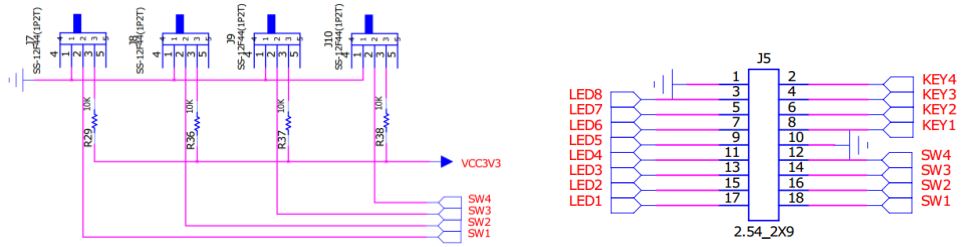
## 3.2.5 Dip Switch

### Overview

There are four dip switches in the development board. Users can manually input low level to the corresponding FPGA pins for testing purposes.

### Dip Switch Circuit

**Figure 3-11 Dip Switch Circuit Schematic**




### Pinout

There are user-extended IOs on the development board that can be connected if needed. Connect the dip switch-related control ports on the J5 connector to the corresponding IOs on the extended IO connector J2 with Dupont cables, the IOs are assigned to the dip switch.

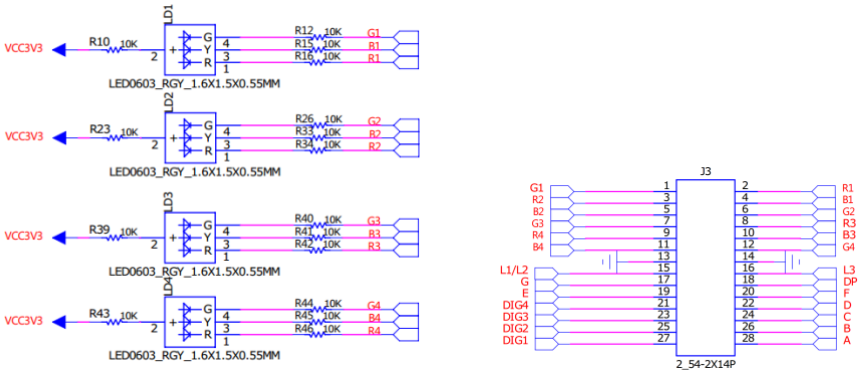
## 3.2.6 RGB LED

### Overview

The development board has four RGB LEDs. After connecting the RGB control connector to the extended IO connector, the FPGA can control the RGB LED to display different status.

### RGB LED Circuit

**Figure 3-12 RGB LED Circuit Schematic**




### Pinout

There are user-extended IOs on the development board that can be connected if needed. Connect the RGB LED-related control ports on the J3 connector to the corresponding IOs on the extended IO connector J2 with Dupont cables, the IOs are assigned to the RGB LED.

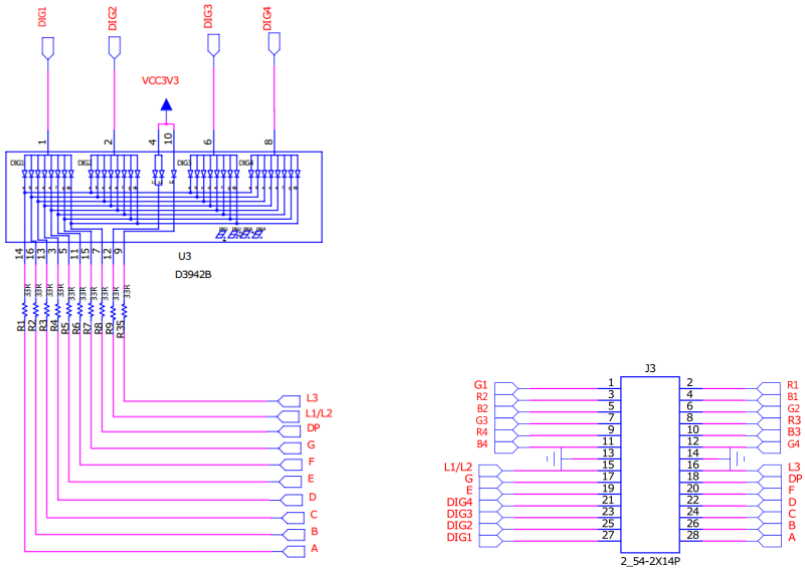
## 3.2.7 Digital Tube

### Overview

The development board has one 4-bit 8-segment digital tube with clock. After connecting the digital tube control connector to the extended IO connector, the FPGA can control the RGB LED to display different status.

### Digital Tube Circuit

**Figure 3-13 RGB LED Circuit Schematic**




### Pinout

There are user-extended IOs on the development board that can be connected if needed. Connect the digital tube-related control ports on the J3 connector to the corresponding IOs on the extended IO connector J2 with Dupont cables, the IOs are assigned to the digital tube.

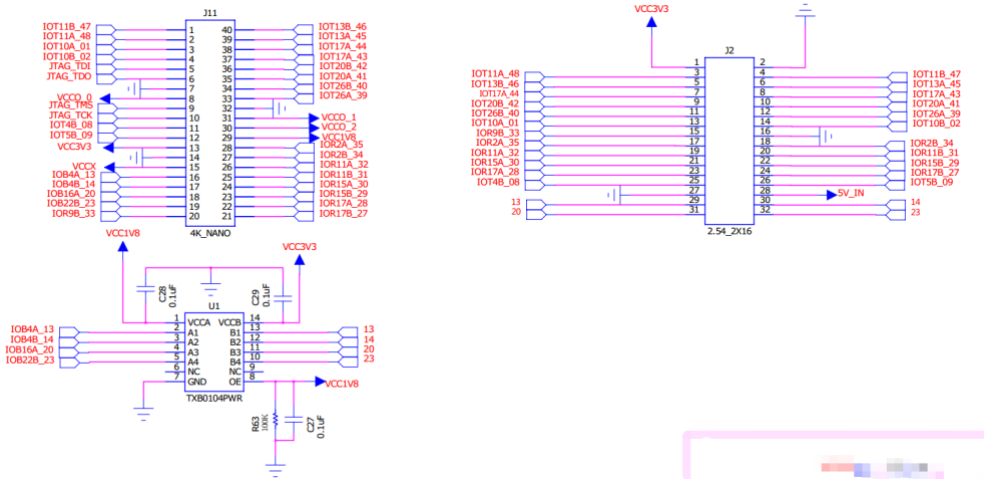
## 3.2.8 Motherboard Extended IO Connector

### Overview

The development board connects all extended IOs of motherboard to a double-row 2.54mm pin header J2, which is convenient for you to use.

## Extended IO Circuit

**Figure 3-14 Extended IO Circuit Schematic**




## Pinout

The extended IO in the development board can be connected if needed. Connect the control IO of the corresponding peripheral to the J2 connector to use the MiniStar nano motherboard to control or read the status of the peripheral; the J2 connector pinout is shown below.

**Table 3-7 J2 Connector Pinout**

| J2 Pin | Pin No. | Description | I/O Level |
|---|---|---|---|
| 1 | - | Power Supply 3.3V | - |
| 2 | - | GND | - |
| 3 | 48 | IO | 3.3V |
| 4 | 47 | IO | 3.3V |
| 5 | 46 | IO | 3.3V |
| 6 | 45 | IO | 3.3V |
| 7 | 44 | IO | 3.3V |
| 8 | 43 | IO | 3.3V |
| 9 | 42 | IO | 3.3V |
| 10 | 41 | IO | 3.3V |
| 11 | 40 | IO | 3.3V |
| 12 | 39 | IO | 3.3V |
| 13 | 01 | IO | 3.3V |
| 14 | 02 | IO | 3.3V |
| 15 | 33 | IO | 3.3V |

| J2 Pin | Pin No. | Description | I/O Level |
|---|---|---|---|
| 16 | - | GND | - |
| 17 | 35 | IO | 3.3V |
| 18 | 34 | IO | 3.3V |
| 19 | 32 | IO | 3.3V |
| 20 | 31 | IO | 3.3V |
| 21 | 30 | IO | 3.3V |
| 22 | 29 | IO | 3.3V |
| 23 | 28 | IO | 3.3V |
| 24 | 27 | IO | 3.3V |
| 25 | 08 | IO | 3.3V |
| 26 | 09 | IO | 3.3V |
| 27 | - | GND | - |
| 28 | - | Power Supply 5V | - |
| 29 | 13 | IO | 3.3V |
| 30 | 14 | IO | 3.3V |
| 31 | 20 | IO | 3.3V |
| 32 | 23 | IO | 3.3V |

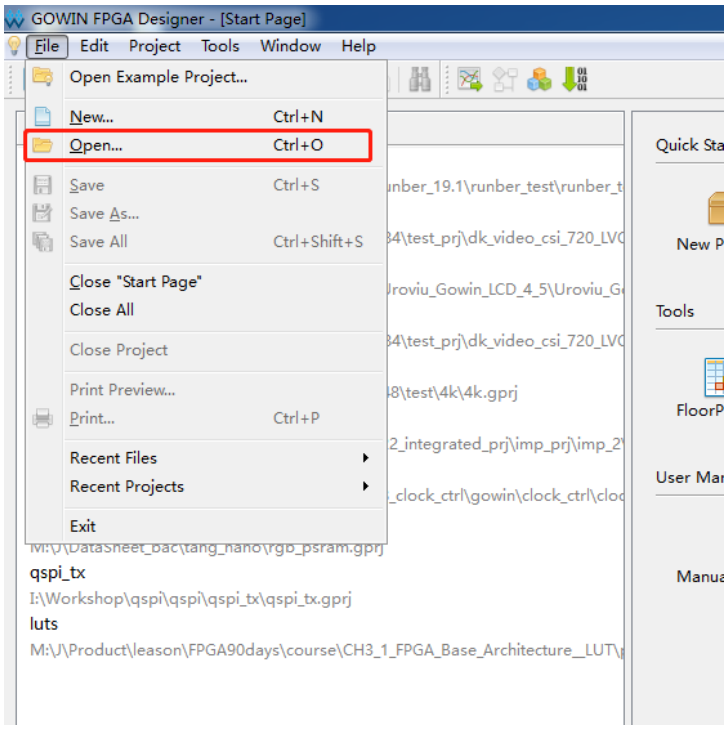
# 4 Use of Development Board

## 4.1 Import Project

For the details of software usage, you can see *SUG100, Gowin Software User Guide*.

1. Directly click .gprj file.
2. Click "File > Open" to choose .gprj file.

**Figure 4-1 Import Project**




## 4.2 Build and Download

1. After writing the program, save it and click "Process > Place & Route" to build. After the build is done, a green tick will appear in front of it.

**Figure 4-2 Click Place & Route**

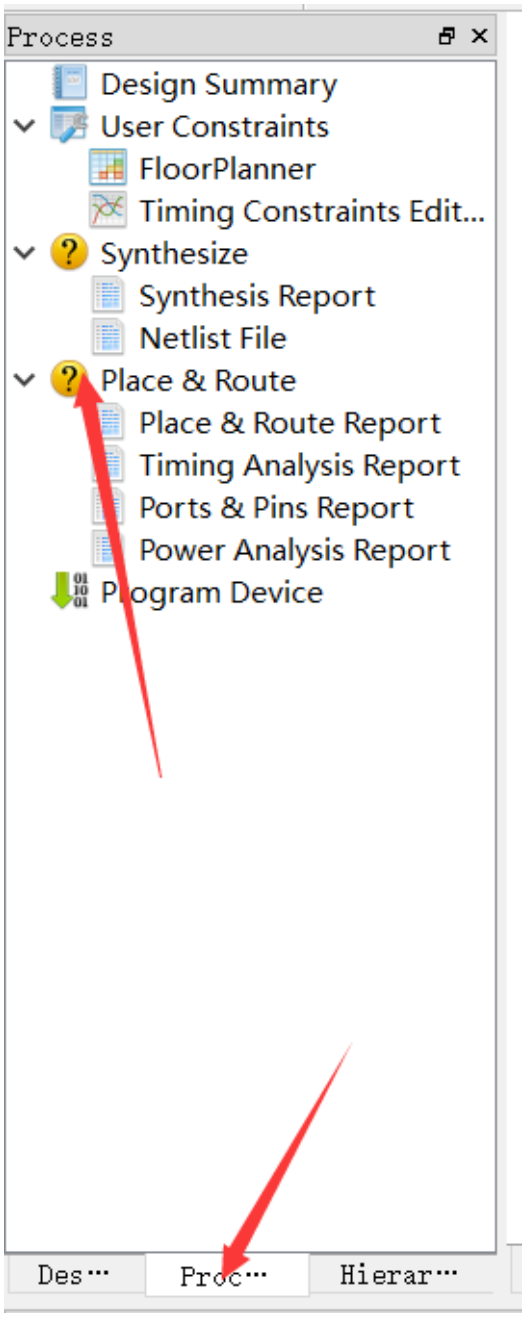
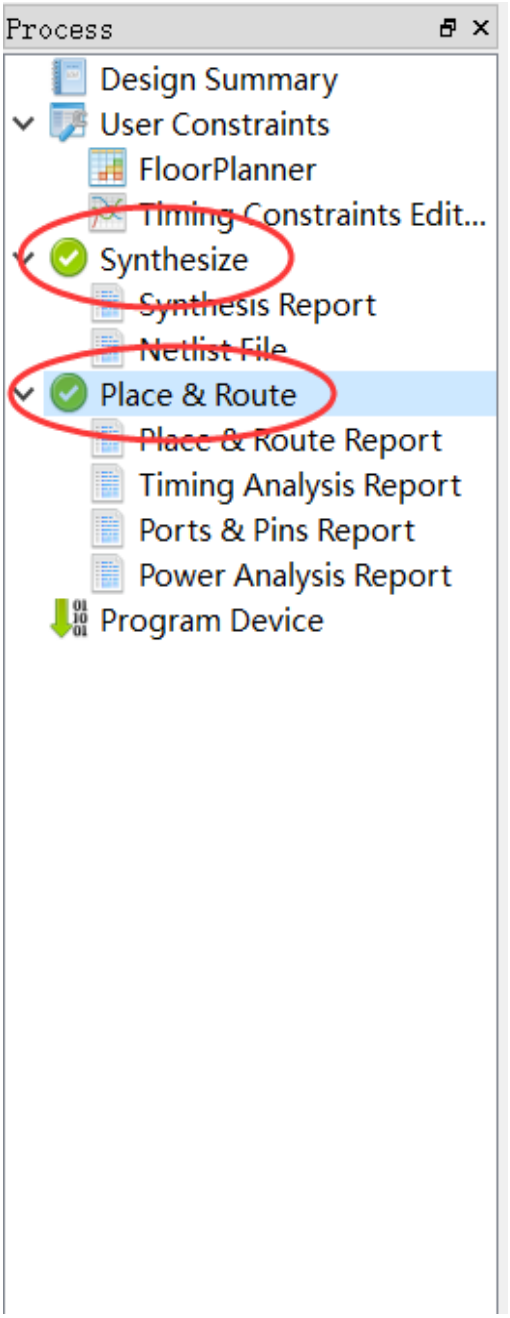


**Figure 4-3 Build Succeed**




2. After build, double-click "Program Device" to pop up the download view, and click to start the download.

**Figure 4-4 Double-click Program Device**

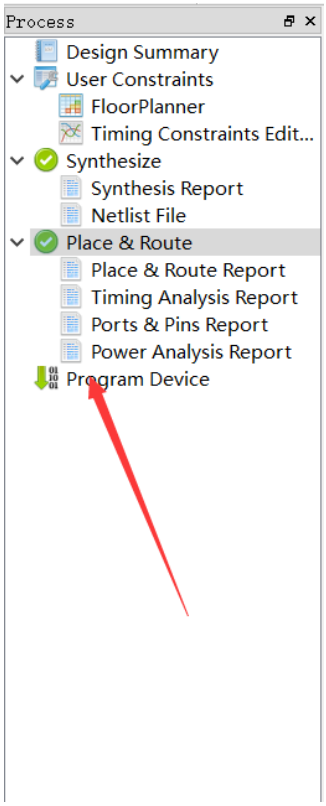
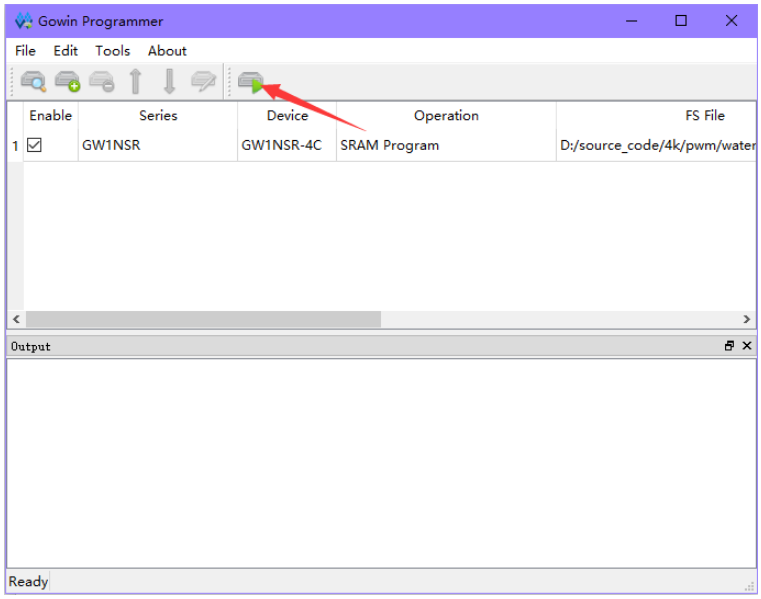



**Figure 4-5 Download View**



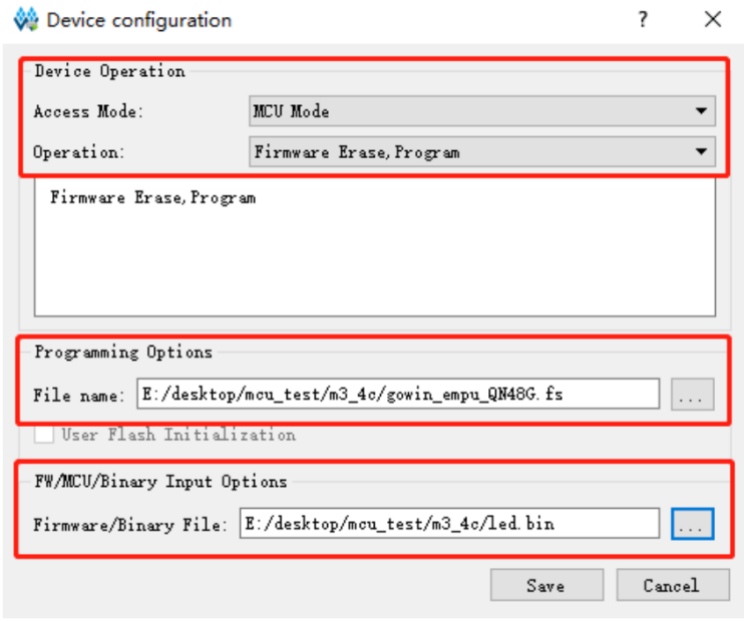
## 4.3 Routine Operation and Description

The supporting video of the development board will be released on Bilibili (website:https://space.bilibili.com/507416742 ) and other websites and related official accounts. You are welcome and encourage to follow the updates and information.

## 4.4 Hardware and Software Download

GW1NS-4C is embedded with ARM Cortex-M3 hardcore processor. If you want to use EMPU, you need to download Gowin_EMPU (GW1NS-4C) hardware bitstream file and software programming BIN file by Programmer of Gowin software. Double-click the device under Device list, and the GW1NS-4C/GW1NSR-4C download options are as shown in the figure below.

**Figure 46 Device configuration View**




For the details, you can see the reference design and manuals on the Gowin Website. You can refer to the following related manuals.

- IPUG930, Gowin_EMPU(GW1NS-4C) Quick Design Reference Manual
- IPUG931, Gowin_EMPU(GW1NS-4C) Software Programming Reference Manual
- IPUG932, Gowin_EMPU(GW1NS-4C) Hardware Design

Reference Manual

- IPUG928, Gowin_EMPU(GW1NS-4C) IDE Software Reference Manual
- IPUG929, Gowin_EMPU(GW1NS-4C) Serial Debugging Reference Manual
- RN933, Gowin_EMPU(GW1NS-4C) Software and Hardware Design Release Note

## 4.5 Notes for the Use of Development Board

1. Handle with care and pay attention to electrostatic protection;
2. When downloading bitstream files to internal flash or external flash, set the MODE pin state to the correct configuration value.
3. When connecting a module, it must be powered off first.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