Mini_Star_Nano Development Board User Manual

8/19/2021

Contents

1. About This Manual

1.1 Contents of the Manual

The User Manual of Mini_Star_Nano Development Board Kit consists of three parts:

1. A brief description of the functionality of the development board and the hardware resources;
2. An introduction of the functionality, circuits and pin planning of the hardware circuits of various parts of the development board;
3. Instructions on use of the development board.

1.2 Applicable Products

Information contained in this Manual is applicable to the following GW1NSR series of FPGA product:

- GW1NSR-LV4CQN48p

1.3 Related Documents

The documents below can be downloaded and viewed at Gowin Semiconductor Corp.'s website www.gowinsemi.com.cn :

1. Data Book of GW1NSR Series FPGA Product
2. Package and Pin Manual of GW1NSR Series FPGA Product
3. Pinout Manual of GW1NSR-4 Devices
4. Programming Configuration Manual of GW1NSR Series of FPGA Product
5. User Manual of Gowin Cloud Software

1.4 Technical Support

1. For latest information on FPGA technologies, please follow our official WeChat account MYMNIEYE;
2. Updated link to teaching videos: https://space.bilibili.com/507416742
3. Taobao store: Minieye Semiconductor
4. Official website: www.myminieye.com
5. QQ group for technical guidance: 808770961

1.5 Terms and Acronyms

Terms and acronyms used in this Manual and related interpretations are listed in Table 1-1.

Table 1-1 Terms and Acronyms

Terms and Acronyms	Full name	Meaning
FPGA	Field Programmable Gate Array	Field Programmable Gate Array
LED	Light Emitting Diode	Light Emitting Diode
LDO	Low Dropout Regulator	Low Dropout Regulator
GPIO	General Purpose Input Output	General Purpose Input Output
LUT4	4-input Look-up Table	4 -input Look-up Table
S-SRAM	Shadow SRAM	Shadow SRAM
B-SRAM	Block SRAM	Block SRAM
PLL	Phase-locked Loop	Phase-locked Loop
PLL	Delay-locked Loop	Delay-locked Loop
DSP	Digital Signal Processing	Digital Signal Processing
QN48p	QN48p	QN48 Package

2. About the Development Board

2.1 Overview

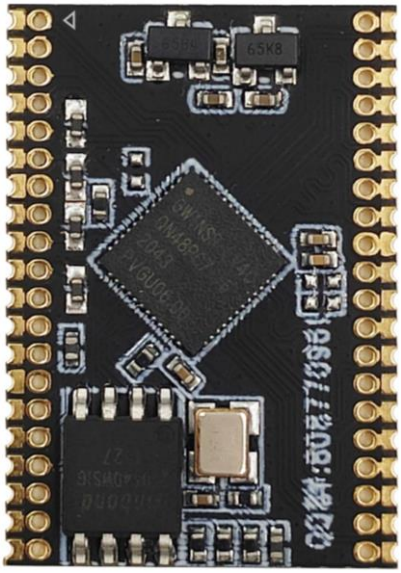


Figure 2-1 Mini_Star_4K Development Board

The MINI_STAR_NANO development board has the GW1NSR series of FPGA ： GW1NSR-LV4CQN48P of Gowin Semiconductor as its core.
The GW1NSR series of FPGA product of Gowin Semiconductor is the first generation FPGA product of its LittleBee® family, a system level packaged chip that integrates the GW1NS series of FPGA product and the PSRAM storage chip. It consists of the GW1NSR-2C device, GW1NSR-4C device, GW1NSR-2 device and GW1NSR-4 device. ARM Cortex-M3 hardcore processor is embedded in the GW1NSR-2C and GW1NSR-4C devices. In addition, USB2.0 PHY, user's flash memory and ADC converter are embedded in the GW1NSR series of FPGA product. The GW1NSR-2C / GW1NSR-4C device has ARM Cortex-M3 hardcore processor as its core, featuring the minimum memory needed for the system function; the embedded FPGA logic module is flexible and easy to use, which can realize various peripheral control functions and provide excellent computing and abnormal system response interruption, and features high-performance, low power consumption, small number of pins, flexible use, instant start, low cost, nonvolatility, high security, diverse types of packages, etc.

The GW1NSR-2C device realizes seamless connection of programmable logic devices and embedded processors, is compatible with various standards of peripheral devices, which can greatly reduce users' costs and be widely used in industrial control, communications, IoT, servo drive, consumption and many other sectors.

2.2 About the Development Board Kit

The development board kit consists of:

- The development board
- Instruction manual

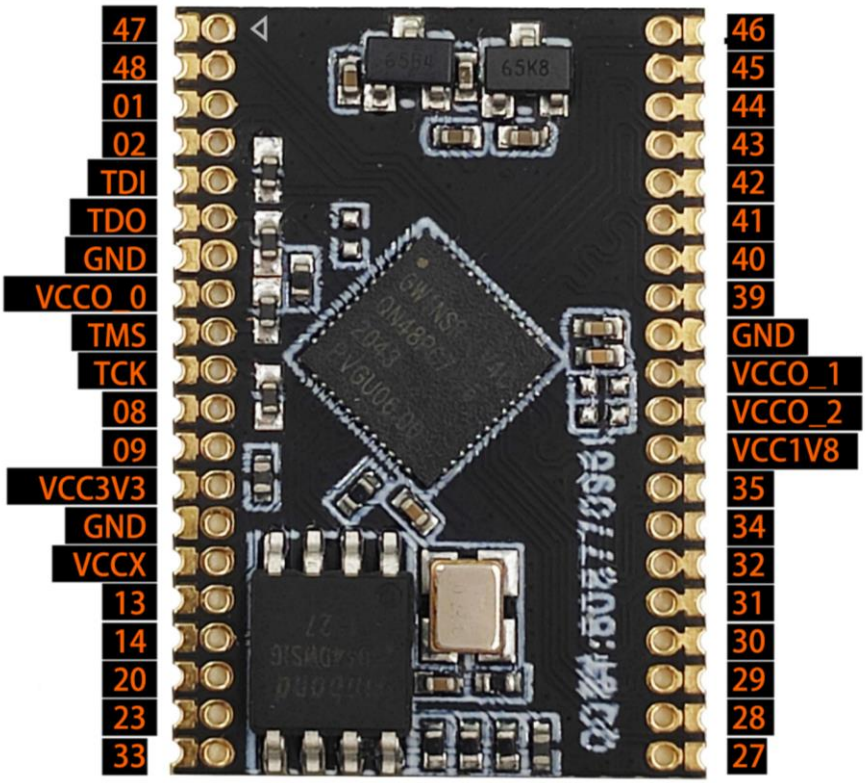


Figure 2-2 MINI_STAR_NANO Development Board's interface

2.3 Features

The structure and features of the development board:

1. FPGA
   - QN48 package
   - Embedded ARM Cortex-M3 hardcore processor
2. FPGA Configuration Modes
   - JTAG
3 Clock Resources
   - 27MHz crystal oscillator
4. Storage
   - 256Kbit internal flash
   - 64Mbit external flash
5. IO expansion interface
   - 2 sets of IO expansion interfaces
6. Power supply
   - Reverse voltage protection;
   - Voltage input of 3.3V.

2.4 Parameters

Table 2-1 List of Parameters of MiniStar_Nano Development Board

No.	Item	Parameter	Description of functionality
5	Clock	1 -way 27MHZ clock	27MHz clock for FPGA
6	Expansion interface	FPC socket expansion	Used to control output for cameras, HDMI, GPIO, etc.
7	Operating Temperature	0~+ 70℃, commercial grade	---
8	Ambient humidity	20%~90%, non-condensing	---
9	Mechanical dimensions	17.9mm×26.0mm	---
10	PCB specifications	2 layers, white characters on black background	---
11	Power supply	3.3V/1A	---
12	System power consumption	---	---

2.5 Diagram of Mechanical Dimensions

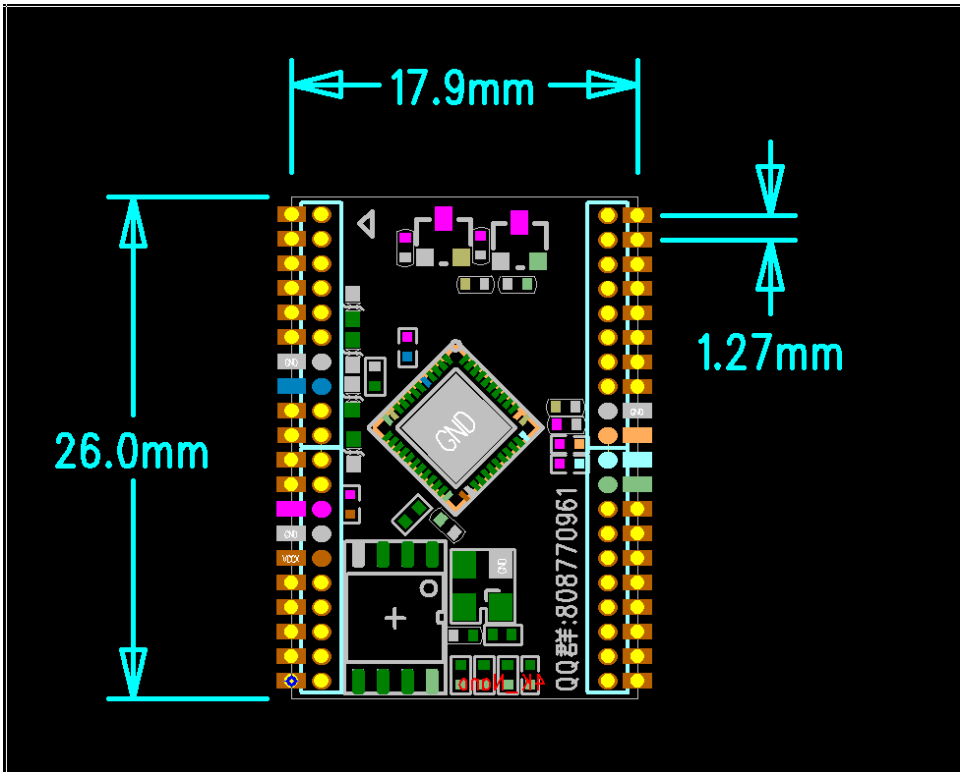


Figure 2-3 MINI_STAR_4K Development Board

3. Detailed Introduction of the Development Board

3.1 FPGA Modules

3.1.1 Overview

Resource information on the GW1NSR-LV4CQN48P FPGA product is shown below in Table 3-1.

Table 3-1 List of Information on GW1NSR Series of FPGA Product

Devices	GW1NSR-4C
Logic unit (LUT4)	4608
Register (FF)	3456
Block SRAM **B-SRAM (bits)**	180K
Number of Block SRAM **B-SRAM (PCS)**	10
User Flash Memory (bits)	256K
PSRAM (bits)	64M
HyperRAM (bit)	64M
NOR FLASH (bits)	32M
Multiplier (18x18Multiplier)	16
Phase-locked loop (PLLs)	2
OSC	1, accuracy of ±5%
Hardcore processor	Cortex-M3
Total number of I/O Banks	4
Maximum number of user I/O	39
Voltage of the core	1.2V

3.1.2 About I/O BANK

The GW1NSR series of FPGA product is divided into 4 I/O BANKs. Figure 3-1 is an overall diagram of the I/O BANKs of GW1NSR series of FPGA product. Figure 3-2 is the diagram of pin planning of QN48P package.

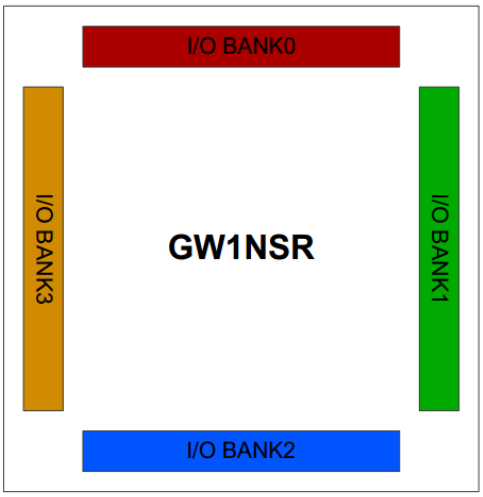


Figure 3-1 Overall diagram of the I/O BANKs of GW1NSR Series of FPGA Product

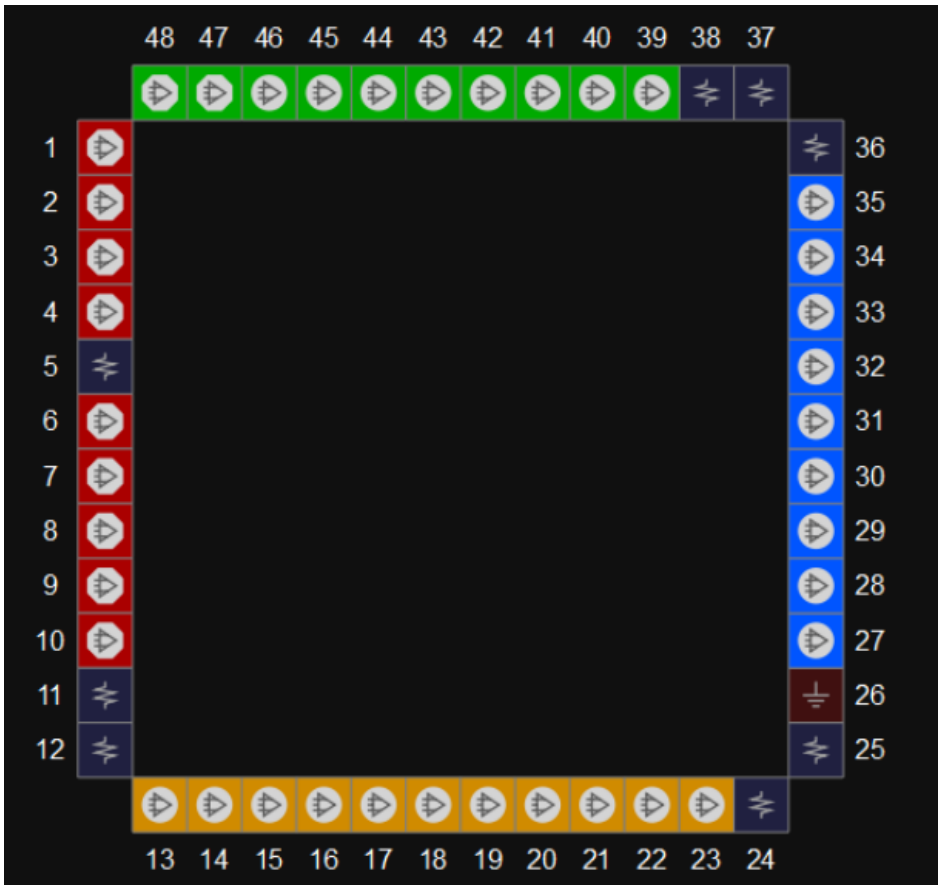


Figure 3-2 Diagram of Pin Planning of GW1NSR-LV4CQN48P FPGA Package (top view)

Table 3-2 FPGA I/O BANK Voltage and Functionality Distribution

BANK	Voltage	Functionality	I/O utilization
0	1.2V/1.8V	Jtag	4 GPIOs
		IO expansion	1 differential pair, 2 GPIOs
1	1.2V/1.8V	IO expansion	5 differential pairs
2	1.2V/1.8V	IO expansion	4 differential pairs, 1 GPIO
3	1.8V	27M clock	1 GPIO
		spi-flash	5 GPIOs
		IO expansion	1 differential pair, 2 GPIOs

3.2 Downloading

3.2.1 Overview

The development board provides a interface for downloading. The downloading of the internal ARM Cortex-M3 hardcore processor is via the same IO.

The diagram of connection for downloading is shown in Figure 3-5.

3.2.2 Downloading Circuit

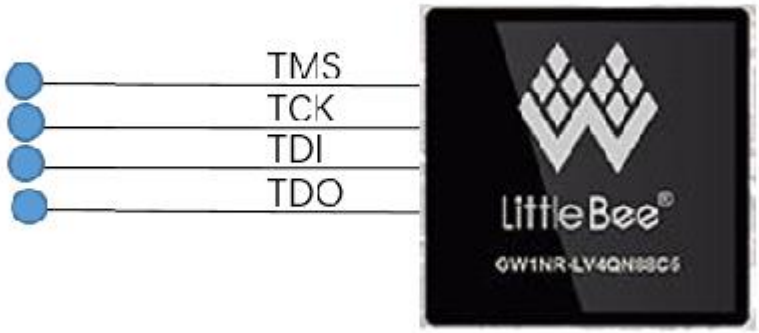


Figure 3-3 Schematic Circuit Diagram of FPGA Downloading

3.2.3 Pin Planning

Table 3-3 Pin Planning of Downloading Circuit

Signal name	No. of FPGA pin	BANK	Description	I/O level
FPGA_ TMS	**6**	0	TMS	3.3V
FPGA_ TCK	**7**	0	TCK	3.3V
FPGA_ TDI	**3**	0	TDI	3.3V
FPGA_ TDO	**4**	0	TDO	3.3V

3.3 Power supply

3.3.1 Overview

The development board provides DC3.3V input via typec-USB interface, and 1.5A overcurrent protection is set up for protection against reverse connection.

The input power supply of DC3.3V is converted to output of 1.8V and 1.2V via IC.

3.3.2 Distribution of Power Supply System

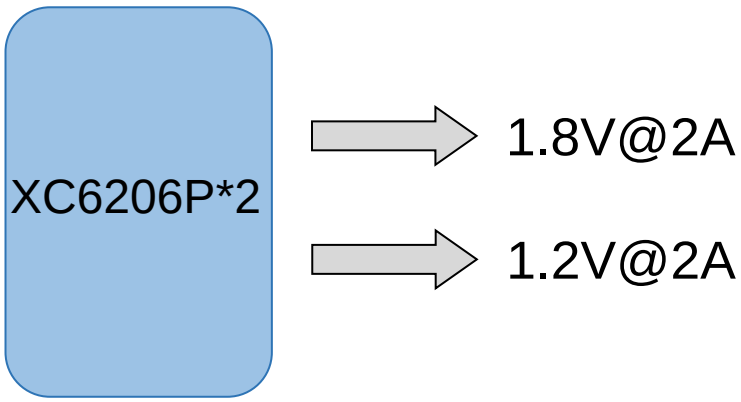


Figure 3-4 Power Supply Circuit

3.4 Clock

3.4.1 Overview

The development board provides 27MHz active crystal oscillator for FPGA, which is connected to the pin of the global clock.

3.4.2 Circuit Diagram of Clock

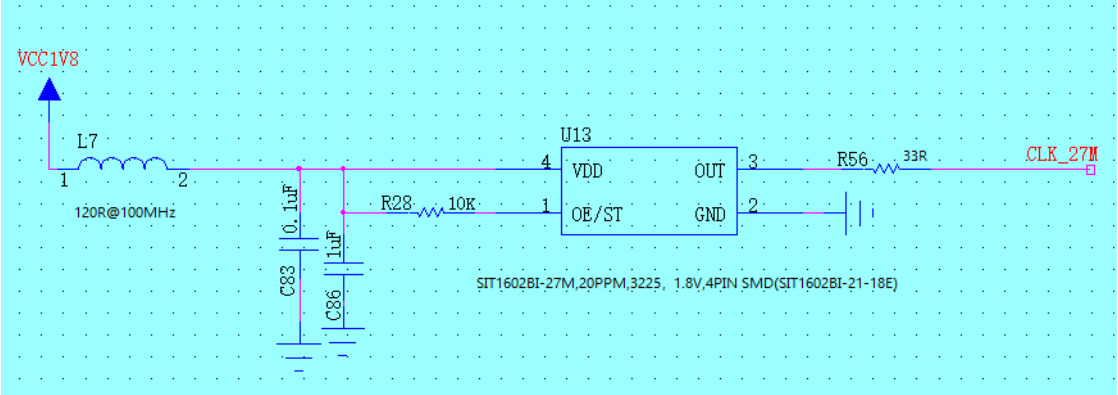


Figure 3-5 Schematic Diagram of Clock Connection

3.4.3 Pin Planning

Table 3-4 Pin Planning of FPGA Clock

Signal name	No. of FPGA pin	BANK	Description	I/O level
CLK_27MHZ_IN	**22**	3	Input from 27MHz active crystal oscillator	1.8V

3.5 Expansion IO

3.5.1 Overview

The board has 2 sets of expansion IO, which are connected via 2 pin holes or stamp holes of 1.27mm-20P. Set 1 consists of: (1) power output of DC3.3V; (2)3 differential pairs of BANK0、BANK1 and BANK3; and (3) 2 GPIOs of BANK0、1 GPIOs of BANK2 and 2 GPIO of BANK3. Set 2 consists of: (1) power output of DC1.8V; (2) 8 differential pairs of BANK1 and BANK2.

3.5.2 Expansion IO

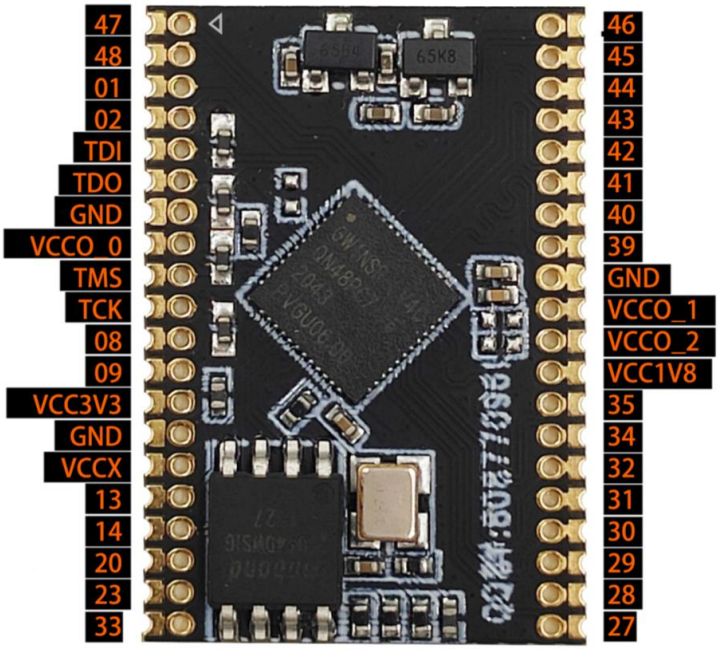


Figure 3-6 Expansion

3.5.3 Pin Planning

Table 3-5 Pin Planning of Expansion IO

Signal name	No. of FPGA pin	BANK	Description	I/O level(default)
IOT10A_01	**1**	0	GPIO	3.3V
IOT10B_02	**2**	0	GPIO	3.3V
IOT4B_08	**8**	0	GPIO	3.3V
IOT5B_09	**9**	0	GPIO	3.3V
IOB4A_13	**13**	3	GPIO	1.8V
IOB4B_14	**14**	3	GPIO	1.8V
IOB16A_20	**20**	3	GPIO	1.8V
IOB22B_23	**23**	3	GPIO	1.8V
IOR17B_27	**27**	2	Differential pair	3.3V
IOR17A_28	**28**	2		3.3V
IOR15B_29	**29**	2	Differential pair	3.3V
IOR15A_30	**30**	2		3.3V
IOR11B_31	**31**	2	Differential pair	3.3V
IOR11A_32	**32**	2		3.3V
IOR9B_33	**33**	2	GPIO	3.3V
IOR2B_34	**34**	2	Differential pair	3.3V
IOR2A_35	**35**	2		3.3V
IOT26A_39	**39**	1	Differential pair	3.3V
IOT26B_40	**40**	1		3.3V
IOT20A_41	**41**	1	Differential pair	3.3V
IOT20B_42	**42**	1		3.3V
IOT17A_43	**43**	1	Differential pair	3.3V
IOT17B_44	**44**	1		3.3V
IOT13A_45	**45**	1	Differential pair	3.3V
IOT13B_46	**46**	1		3.3V
IOT11B_47	**47**	1	Differential pair	3.3V
IOT11A_48	**48**	1		3.3V

3.6 64M SPI Flash

3.6.1 Overview

This development board is equipped with 64Mbit SPI flash, model W25Q64DWSSIG. The program can be downloaded to flsah and saved through JTAG interface.

3.6.2 Schematic Diagram of SPI Flash

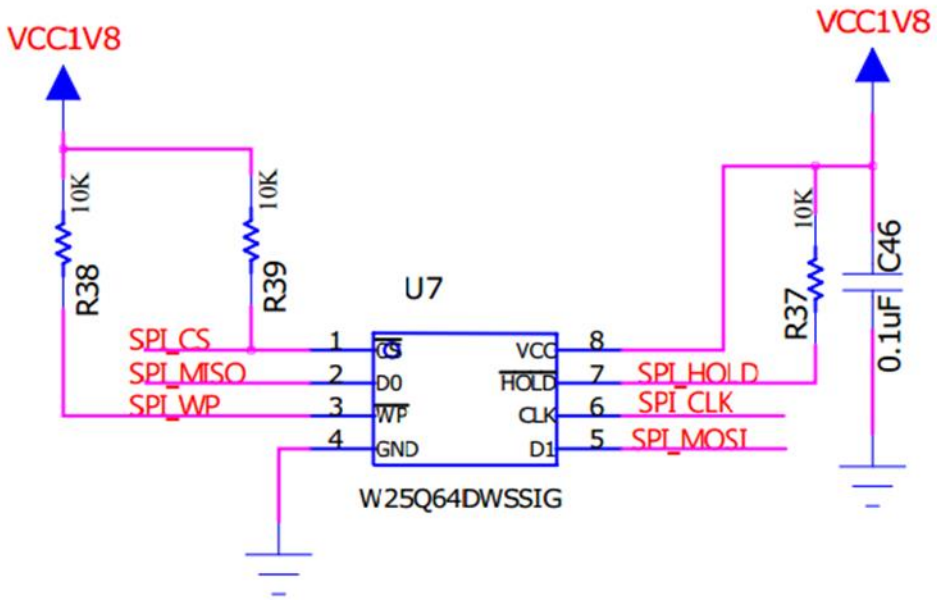


Figure 3-7 Schematic Diagram of SPI Flash

3.6.3 Pin Planning

Table 3-6 Pin Planning of SPI Flash

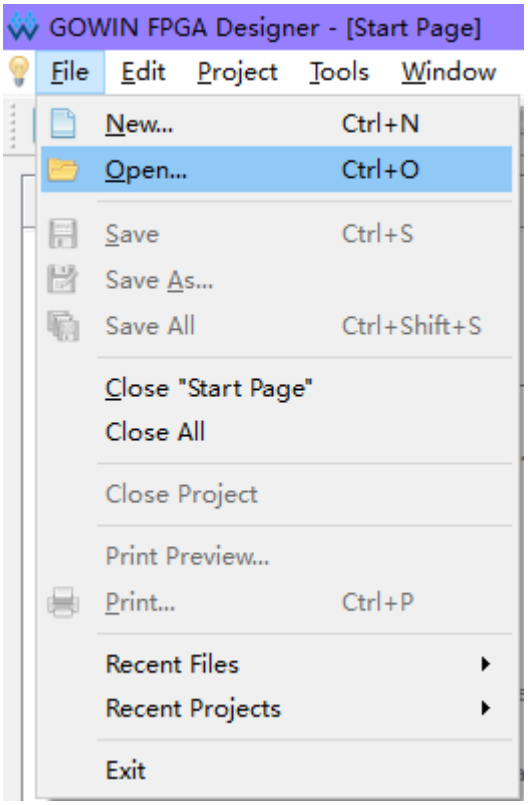
Signal name	No. of FPGA pin	BANK	Description	I/O level
SPI_CS	**17**	3	SPI enable	1.8V
SPI_MISO	**16**	3	Master Input Slave Output	1.8V
SPI_WP	**15**	3	Write protect	1.8V
SPI_HOLD	**18**	3	Data retention	1.8V
SPI_CLK	**19**	3	SPI clock	1.8V
SPI_MOSI	**21**	3	Master Output Slave Input	1.8V

4. Use of the Development Board

4.1 Project Import

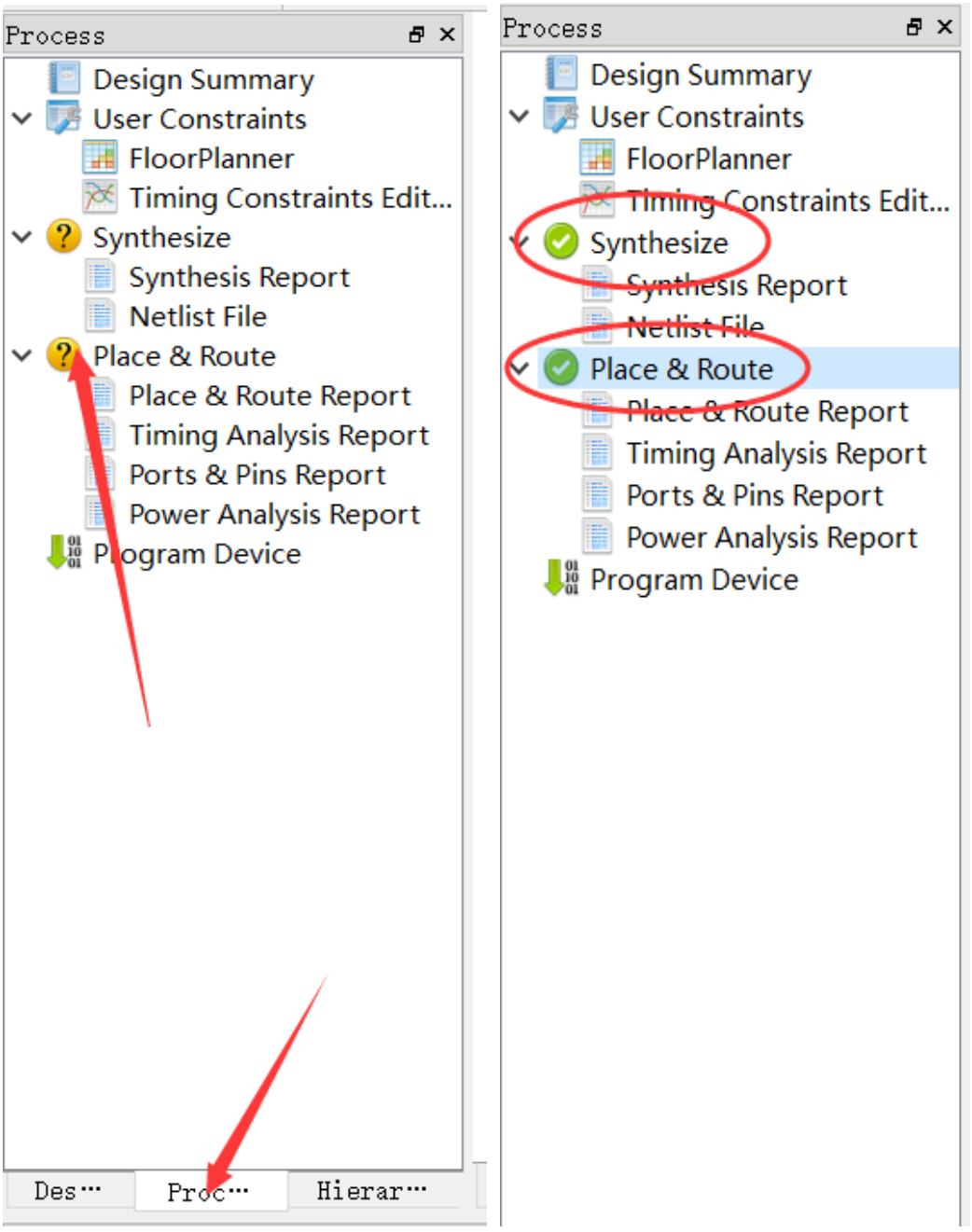
For detailed software operating instructions, see user guide of the SUG100-1.7_Gowin cloud software

1. Click the .gprj file
2. After entering the development software, click “File”→“Open”, and select the .gprj file for import

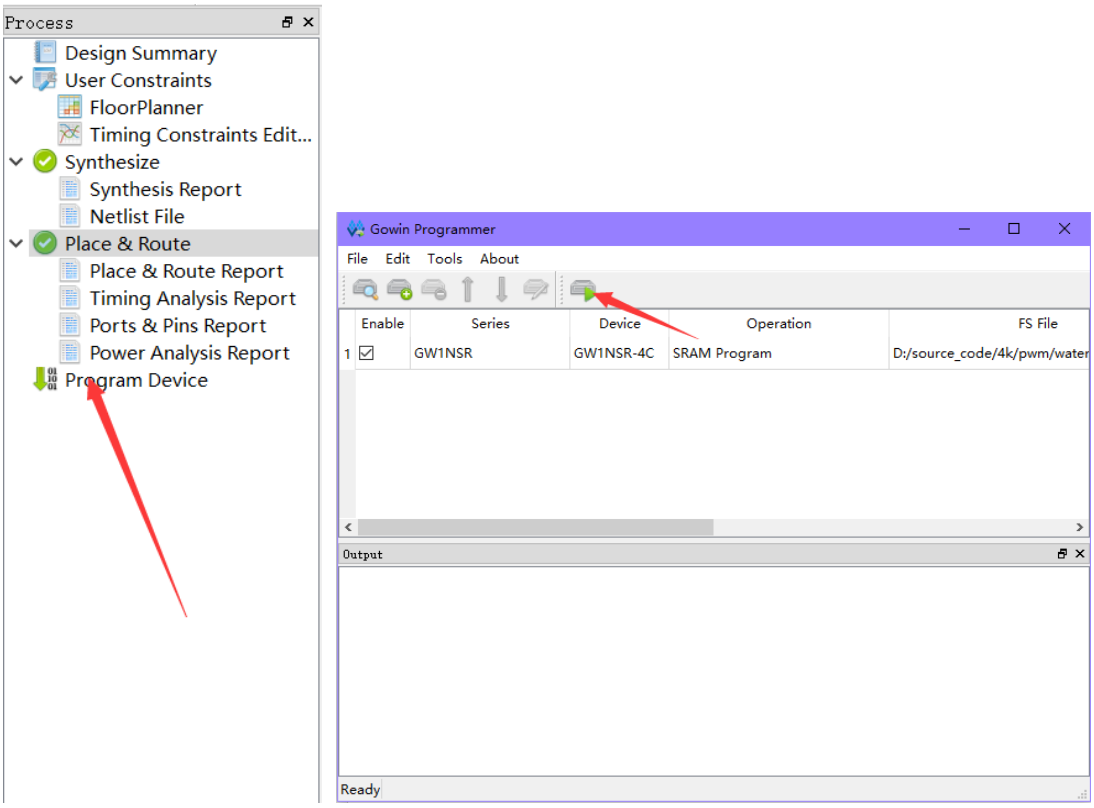


4.2 Program Compiling and Downloading

1. Save the program after coding, click “Process” and click “Place&Route” to begin compiling, after which there will be a green check on the left

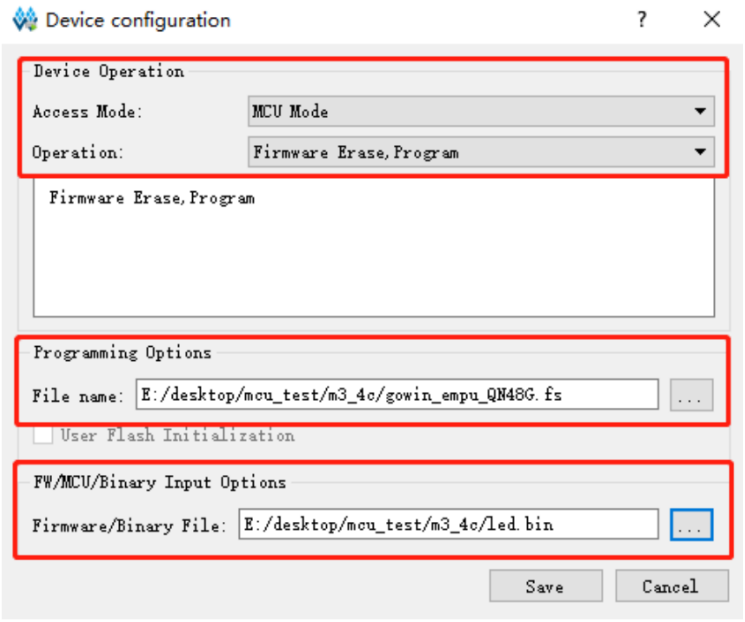


2. After compiling, double-click “Program Device” and the window for downloading will pop up. Click it for downloading



4.4 Hardware and Software Downloading

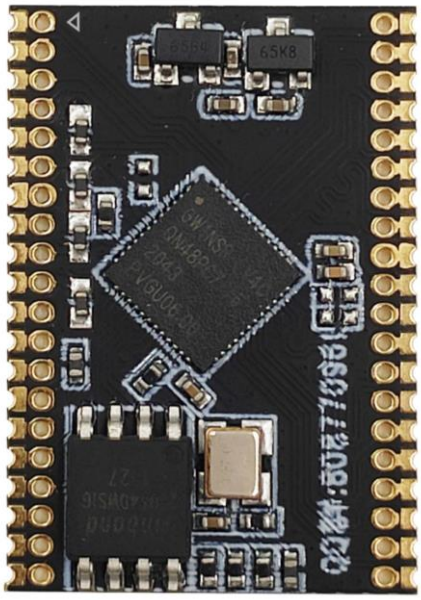
ARM Cortex-M3 hard core processor is embedded in GW1NS-4C. To use EMPU, Gowin_EMPU (GW1NS-4C) code stream file for hardware design and binary BIN file for software programming design need to be downloaded using the download software "Programmer" of the Gowin cloud software. Double-click the device under "device" at the download interface. The download option configuration of GW1NS-4C/GW1NSR-4C is shown below.



For use of EMPU on GW1NS-4C, please see Gowin's official documents and reference design:
http://www.gowinsemi.com.cn/prodshow_view.aspx?TypeId=71&Id=186&FId=t31:71:31#IP

文档
IPUG930, Gowin_EMPU(GW1NS-4C)快速设计参考手册
IPUG931, Gowin_EMPU(GW1NS-4C)软件编程参考手册
IPUG932, Gowin_EMPU(GW1NS-4C)硬件设计参考手册
IPUG928, Gowin_EMPU(GW1NS-4C)IDE 软件参考手册
IPUG929, Gowin_EMPU(GW1NS-4C)串口调试参考手册
RN933, Gowin_EMPU(GW1NS-4C)软件和硬件设计发布说明

4.5 Instructions on Use of the Development Board



1. When using the development board, please handle it with due care, and make good electrostatic protection.
2. When downloading bitstream file to internal Flash or external Flash, the MODE pin state should be set up at proper value.
3. The power should be shut off when connecting the modules.