Simulation of Synchronous Reference Frame PLL for Grid Synchronization using Simulink

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***Abstract*—The important problem in integration of grid and power converter is how to synchronize the inverter with the grid that is one is before connecting an inverter to the grid and other is during operation. The energy transfer between an inverter and grid is improved by proper design of synchronization techniques. The challenges associated with the design is how fast the voltage, phase angle and frequency are estimated and synchronized under ideal and non-ideal conditions. For effective estimation of above quantity, various synchronization methods have been proposed. In this paper, theory of single phase PLL is outlined and design and simulation of Synchronous Reference Frame Phase Locked Loop and the obtained simulation results for various non-ideal conditions like harmonics, voltage dip, phase jump and frequency variations are presented.**

Keywords—grid synchronization, phase locked loop (PLL), synchronous reference frame(SRF), phase detection, smart grid.

I. INTRODUCTION

The raising concern of rapid depletion and increasing cost of fossil fuels, the government policies of developed and developing countries are more encouraging distributed generation (DG) systems to reducethe greenhouse gas emission [3]. Especially, those DG's are considered which are based on renewable energy sources such as hydro, wind turbines and photo-voltaic (PV) plants. If grid-connected renewable systems are compared with off-grid configurations, grid-connected systems are more effective due to government incentives and easiness of integration with existing plant. DG's are showing an impressive growth and smart grid technology are now in literature [4]. In order to make sure that the current drawn from the supply is in phase with the supply voltage and also that the generated phase voltages are able to form balanced three-phase voltages together with the supply voltage, a synchronization unit is needed to provide the phase information of the supply.

Grid-connected system faces certain problems among which grid synchronizationi.e. how to synchronize the grid with the inverter is of great significant. Here there are two cases: one is before connecting the inverter to the grid and other is during operation. If grid synchronization is not accurately designed, it may lead to large transient currents at the time of connection which may cause damage and extra pollution on the electric utility will be injected as harmonic injection, frequency variation and phase shifts. Therefore, harmonic content and the power factor must be controlled.

The aim is to synchronize the inverter with the grid in adverse operating condition like unbalanced or distorted utility condition to meet the actual standards. The synchronization should be properly controlled at the point of common coupling to reduce voltage disturbances and undesirable effects. Hence, the inverter needs to be synchronized properly with the grid or the source to which it is connected so that the system can work properly. Also, the grid information i.e. phase angle, frequency and amplitude of the voltage is needed accurately and in a timely manner so that the inverter is able to synchronize with the grid. [5], [4], [10]. Several solutions and architectures to estimate the phase angle have been proposed [6], [8].

II. DEMANDS AND STANDARDS

In order to connect an inverter with the grid, the generated power has to meet the standards given by utility companies. The standards like IEEE1547 & IEC61727 puts the limitation on maximum amount of injected current into the grid. This limit is very small (0.5% and 1% of rated output currents) which is very difficult to measure. This problem can be resolved by introducing a line frequency transformer between inverter and grid. According to the standard IEC61727 of 10 KW power and IEE1527 of 30KW power, the limit for the current Total Harmonic Distortion (THD) is 5%. Also limit of odd harmonics 3-9 is 4% and 11-15 is 2% respectively [1], [12].

III. SYNCHRONIZATION TECHNIQUES

Basically there are two methods of synchronization: open loop and close loop methods. Open loop method includes zero crossing detection of grid voltage and directly filtering the grid voltage. An example of filtering method is phase-lead low pass filter, space-vector filter method and extended Kalman filter method [13]. These methods have sluggish response with high sensitivity to frequency deviations, voltage distortions and voltage imbalance [5]. Closed loop method includes a mechanism which makes sure that the information obtained is

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accurate. Typical examples include conventional PLL, which is widely used in single phase applications and the other is synchronously rotating reference frame (SRF) PLL which is widely used in three phase applications. Nowadays PLL have been adopted as a part of controllers for most of the grid connected applications e.g. in renewable energy applications, FACTS devices, active power filters, UPS applications and power quality control [10].

A. CONVENTIONAL PLL

PLL is a feedback control system. It automatically matches the phase of a locally generated signal with the phase of input signal. In grid connected system, PLL synchronizes the instantaneous phase angle of inverter voltage with the phase angle of grid voltage to get power factor close to unity. The block diagram of conventional PLL is given in Fig.1.

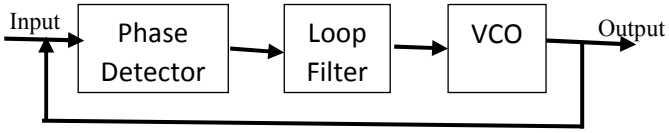


Fig. 1. Block Diagram of conventional PLL [11].

- It consist of phase detector (PD), loop filter (LF), and a voltage controlled oscillator (VCO). The PD measures the phase difference between the input signal and reproduced output signal and then generates a voltage according to the phase difference between the two signals. It can be analog or digital.
- The LP is a low pass filter (LPF) which blocks all higher frequency signals and extracts DC component. The filter regulates the stability of the loop. If it is not designed correctly, then it can build oscillations around the loop and large signals will appear on thetune line. This will result in VCO being forced to sweep over wide band of frequency. Hence, proper filter design is needed.
- The DC component is then amplified and passed to VCO which could be a PI controller to generate a frequency of output signal. The frequency is then integrated to form the phase of output signal.

If the output frequency is locked with the input frequency, the phase difference of PD iseventually driven to zero. As a result, phase of output signal is locked with theinput signal.

MATHEMATICAL ANALYSIS

Fig. 2 shows the control structure of PLL. Different techniques can be used to implement each blocks of PLL. In this case PD is implemented using a multiplier, LF using a LPF and VCO containing PI controller, an integrator and a sinusoidal function.

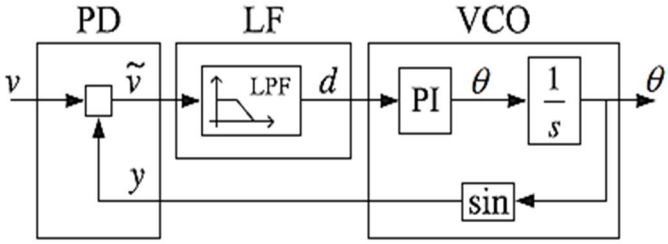


Fig. 2. Control Structure of PLL [10].

For input signal $v = V_m\cos\theta_g$, with $\theta_g = \omega_g + \phi_g$ and output signal $y = \sin\theta$, with $\theta = \omega t + \phi$, the output of PD is:

$$\tilde{v} = vy = V_m\sin\theta\cos\theta_g \quad (1)$$

$$\tilde{v} = \frac{V_m}{2}\sin(\theta - \theta_g) + \frac{V_m}{2}\sin(\theta + \theta_g) \quad (2)$$

$$\tilde{v} = \frac{V_m}{2}\sin[(\omega - \omega_g)t + (\phi - \phi_g)] + \frac{V_m}{2}\sin[(\omega + \omega_g)t + (\phi + \phi_g)] \quad (3)$$

The first term of eq(3) is a low frequency component which contains the phase difference between v and y and the second term is high frequency component which is filtered out by the loop filter. Hence, the output of LF is:

$$d = \frac{V_m}{2}\sin[(\omega - \omega_g)t + (\phi - \phi_g)] \quad (4)$$

which is fed to PI controller to generate estimated frequency $\omega = \theta$ until $d = 0$. The estimated frequency is then integrator to form the phase of output signal $y = \sin\theta$, which is sent back to PD to complete the loop. In steady state, when d is driven to zero and $\omega = \omega_g$ with $\phi = \phi_g$, the phase of output signal is said to be locked with that of input signal v. Hence, phase of input signal and output signal is synchronized.

B. SRF PLL

The widely used technique for frequency insensitive grid synchronization in three phase systems is SRF PLL. The basic idea of PLL is the feedback system with a PI controller tracking the phase angle. In this case, the input is a three phases of the grid voltages and output from the PLL is the phase angle of one of the three phases. There are two choices, one is assuming the grid voltages are balanced and tracking only one of the three phases and then shifting with 120^o for each of the other two phases and the second is having three PLL systems, one for each phase. In SRF PLL, three phase voltage vector is translated from abc natural reference frame to $\alpha\beta$ stationary reference frame by using Clarke's transformation and then to *dq* rotating

reference frame by using Park's transformation as shown in Fig. 3.

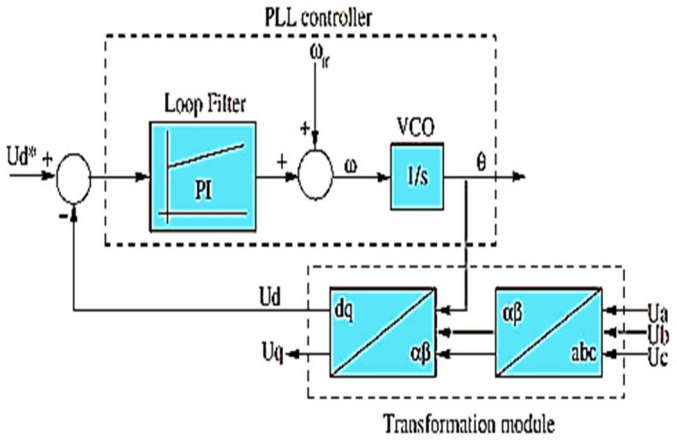


Fig. 3. General Structure of Three Phase SRF PLL.

The angular position of *dq* reference frame is controlled by the feedback loop to make the *d* axis overlappingwith the grid voltage vector. Therefore, in steady state, the *q* axis component represents the amplitude of the voltage vector and the output of the *d* channel feedback loop represents the frequency and the phase of voltage vector.

1) STATIONARY REFERENCE FRAME *αβ*

To track the phase angle, the three phase of the voltage signals V_a, V_b, V_c are transformed to two phases of stationary system V_α and V_β using Clarke transformation as shown in Fig 4.

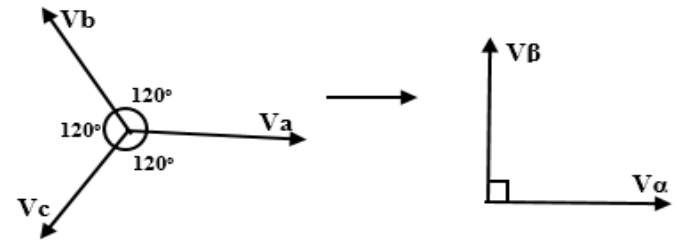


Fig. 4. Clarke Transformation [9].

The three grid voltages are given as:

$$V_{abc} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = V_m \begin{bmatrix} \cos \omega t \\ \cos\left(\omega t - 2\frac{\pi}{3}\right) \\ \cos\left(\omega t + 2\frac{\pi}{3}\right) \end{bmatrix} \quad (5)$$

The αβ-transformation matrix by Clarke's Transformation is:

$$V_{\alpha\beta} = [T_{\alpha\beta}].V_{abc} \quad (6)$$

Where, V_{abc} is three phase utility voltage and $[T_{\alpha\beta}]$ is Clarke's Transformation matrix.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (7)$$

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = V_m \begin{bmatrix} \sin\theta \\ \cos\theta \end{bmatrix} \quad (8)$$

This is two signals (Fig 5) carrying information of phase angle of one of the two phases i.e. V_a

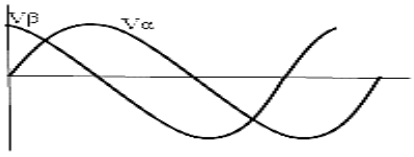


Fig. 5. Two Phase Reference Signal.

So, reference frame with V_α and V_β as co-ordinates is called Stationary reference frame.

2) ROTATING REFERENCE FRAME *dq*:

The phase angle θ is tracked by synchronizing the voltage vector along *d* axis. The two-axis stationary reference frame are transformed into rotating reference frame using Park transformation as shown in Fig. 6.

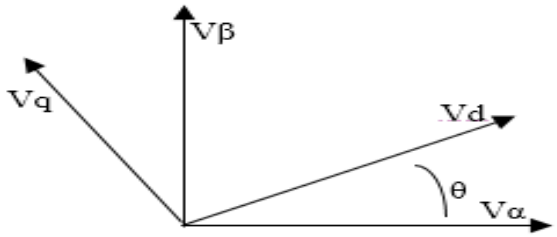


Fig. 6. Park Transformation [9].

The *dq*-transformation matrix by Park's Transformation is:

$$V_{dq} = [T_{dq}] * V_{\alpha\beta} \quad (9)$$

Where, $[Tdq]$ = Park's Transformation matrix.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos(\theta') & \sin(\theta') \\ -\sin(\theta') & \cos(\theta') \end{bmatrix} \begin{bmatrix} V\alpha \\ V\beta \end{bmatrix} \quad (10)$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = V_m \begin{bmatrix} \sin(\theta - \theta') \\ -\cos(\theta - \theta') \end{bmatrix} \quad (11)$$

At steady state, the phase error $\theta - \theta'$ is small and the sine term is approximated as:

$$V_d = V_m \sin(\theta - \theta') \approx V_m(\theta - \theta') \quad (12)$$

The above equation is used to implement a small signal linearized model of SRF PLL (Fig 3).

IV. SIMULATION

The Simulink model for SRF PLL is shown in Fig. 7.

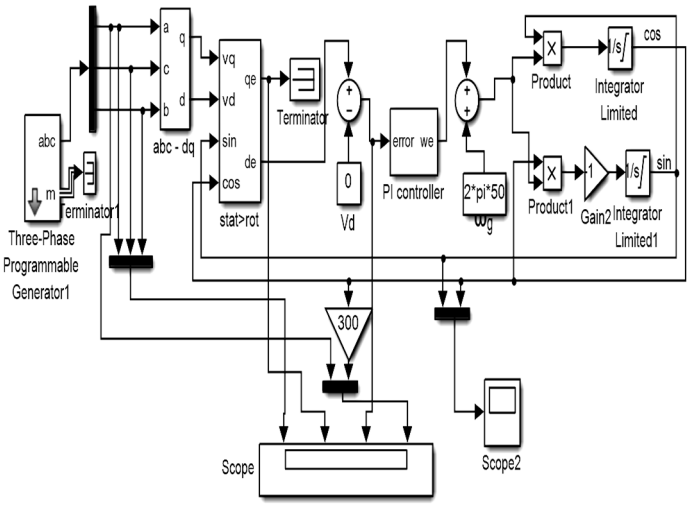


Fig. 7. Simulink Model for SRF PLL.

Our aim is to make the phase difference $(\theta - \theta')$ zero i.e. V_d / V_q = 0. Hence, due to presence of PI controller in the control loop the error ultimately becomes zero. Also, V_q is sufficient for reconstruction of voltage vector. The gains of PI controller isdesigned such thatV_d follows the reference value V_d^* = 0 [6]. This results in estimated phase angle θ' that equals the phase angleθ. The symmetrical optimum method [14] is used for PI parameters tuning. Hence, K_p = 10 and K_i = 200. A feed-forward frequency $\omega_{ff} = 2\pi f_{ff}$, where$f_{ff}$ is the grid natural frequency (314 rad/s), is added at the output of PI controller to improve the dynamic performance and to make the output signal zero [2]. For PI type LF, linearized loop transfer function is given by:

$$H(s) = \frac{2\xi\omega_n s + \omega_n{}^2}{s^2 + 2\xi\omega_n s + \omega_n{}^2} \quad (13)$$

Where, $\omega_n = \sqrt{K_i}$ and $\xi = K_p / 2\sqrt{K_i}$

Well-designed PLL system should meet the following criteria [16]:

- $\xi \approx 0.7$ for optimum transient response.
- Narrow bandwidth i.e. low ω_n for improved noise rejection, in order to produce a pure sinusoidal output signal in the presence of input harmonics.

V. SIMULATION RESULTS

The simulation results of SRF PLL implemented in MATLAB R2015a/Simulink shows that when grid phase equals to inverter phase, the error at the output of the phase detector becomes zero and equal to reference V_d*. Hence, the lock is set by PLL. Fig. 8(a) shows the balanced three phase supply from grid connected inverter with voltage amplitude 300V. In Fig. 8(b),

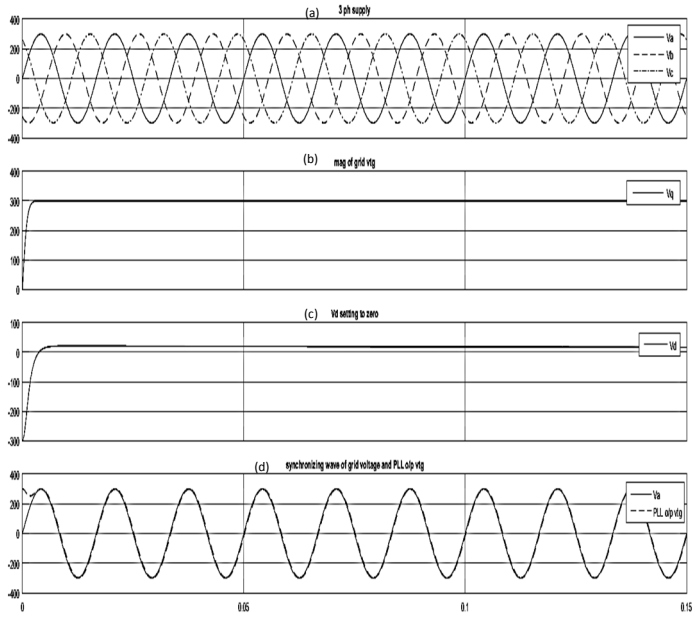
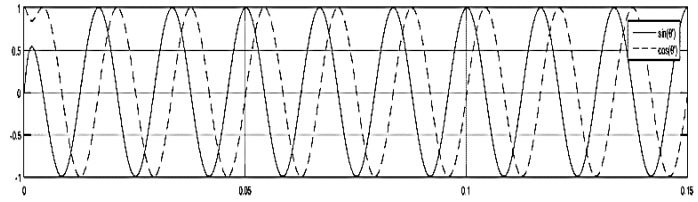


Fig.8. SRF PLL response under ideal grid condition

V_q represents the voltage amplitude of the grid voltage which is 300V and Fig. 8(c) shows V_d is setting to zero by the control loop. The output controlled signal from PI controller to VCO generates the sinθ' and cosθ' (Fig. 9) required for abc to *dq* transformation. PI controller gain is varied to detect accurate inverter phase angle and obtain zero phase error. Synchronization between output of grid phase and inverter phase angle is achieved by locking PLL not only at zero crossing but also at every instant of time between 0 to 2π. Synchronization of PLL output voltage



and grid voltage is shown in Fig. 8(d).

Fig. 9. Sin and cos waveforms.

Under the given cross over frequency ω_c = 314 rad/s, the SRF PLL is simulated for four different distorted conditions which is harmonics, voltage dip, phase jump and frequency variations [15]. The 3rd and 5th harmonics are added to the input of PLL system as shown in Fig. 10. It can be seen that the phase angle of the fundamental frequency is still tracked rather accurately and harmonics are not cancelled completely.

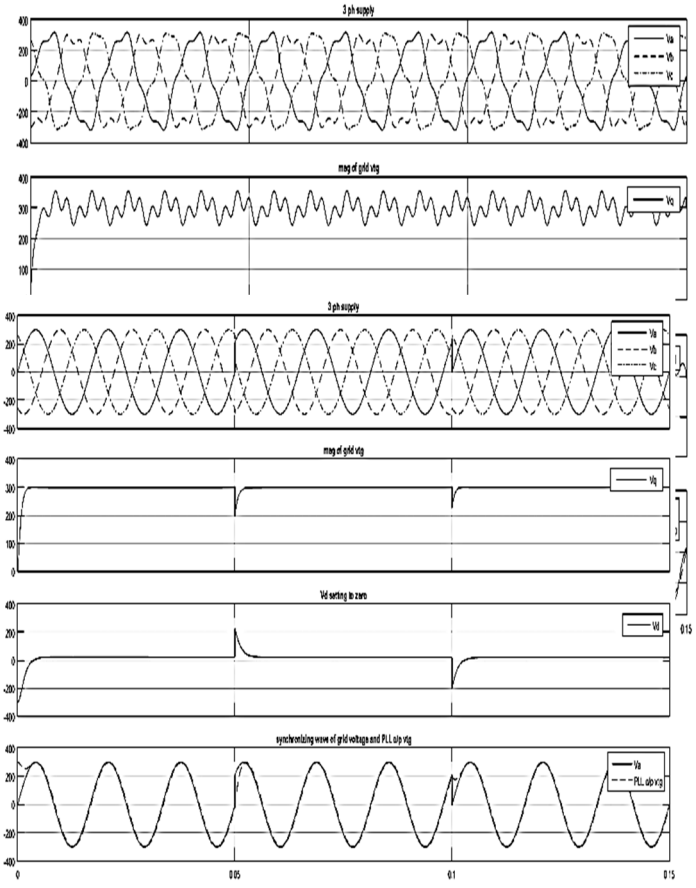


Fig.10. SRF PLL response under harmonic grid condition.

To verify the fundamental task of PLL – phase tracking, a phase jump test is simulated. The grid voltage phase changes stepwise by 45° at t = 0.05s, as shown in Fig. 11. The SRF-PLL responds with high estimated frequency spike, which drives phase error to zero in less than half of period. Lower controller gains allow to respond more smoothly. Thus increasing regulating time.

Fig.11. SRF PLL response under phase jump of grid voltage.

A symmetrical voltage dip is applied to the PLL input system with 33.3% depth at t = 0.05s as shown in Fig.12. The SRF-PLL does not include any filtering in voltage estimation process, therefore magnitude tracking is instantaneous and it does not depend on controller tuning.

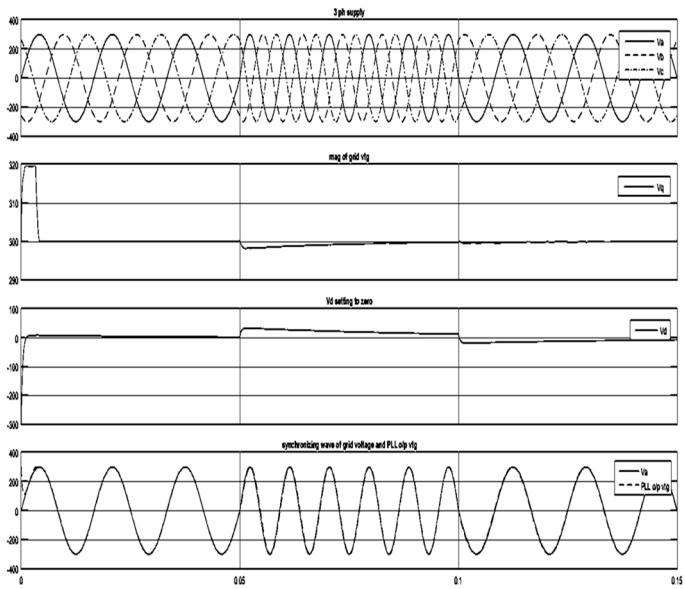
Fig.12. SRF PLL response under balanced voltage dip condition.

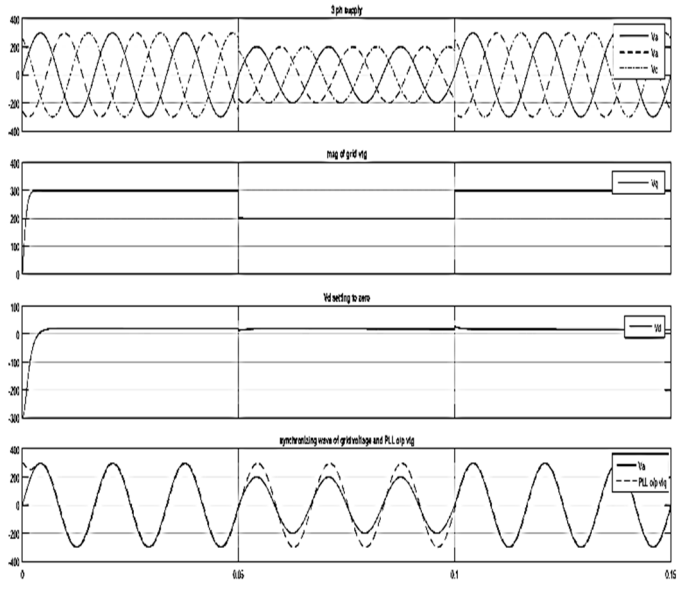
Now, the step frequency change of 50 Hz is applied to theinput voltage of PLL at t = 0.05s which is shown in Fig. 13. The SRF PLL is able to track the phase accurately and error occurring at V*d* signal is less.

Fig. 13. SRF PLL response under frequency step of grid voltage.

VI. CONCLUSION

In this paper, the importance of grid voltage synchronization methods is presented at the beginning. A concise review on single phase PLL for grid synchronization method is provided. In applications of grid connected power converter, proper synchronization requires fast and precise detection of grid voltage phase angle – it is the task of Phase Locked Loop (PLL) algorithm. PLL algorithms should guarantee robustness to grid voltage distortions like voltage dips, phase angle jumps, frequency variations or higher harmonics content. Simulink model of SRF PLL and its simulation results in the above given grid conditions is presented showing the synchronization of grid voltage and PLL output voltage accurately.





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