Signal Conditioning and Analog-Digital conversion

Avionics and Spacionics

Paulo Pedreiras, pbrp@ua.pt

DETI/UA/IT

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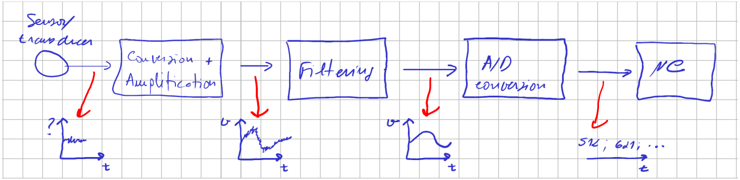
Introduction

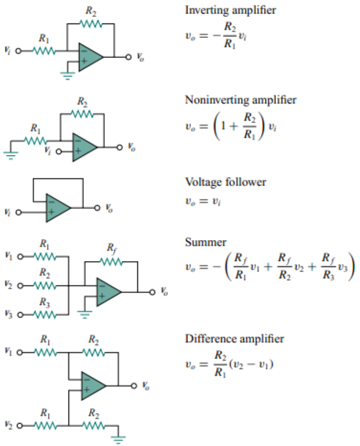


- Sensors and transducers often have outputs that are unsuitable for direct processing. This is the case e.g. of very small voltages and currents, charge output, presence of offset voltages, etc.
- In this case sensor/transducer signals must be properly conditioned.
- Nowadays, at the end of the chain these signals are digital processed, thus we will address also D-A conversion.

Introduction

Topics:

- Introduction to OpAmps
- Basic OpAmp circuits: amplification, filtering, algebraic operations on signals, ...
- Instrumentation amplifier
- DAC and ADC conversion



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Operational Amplifiers

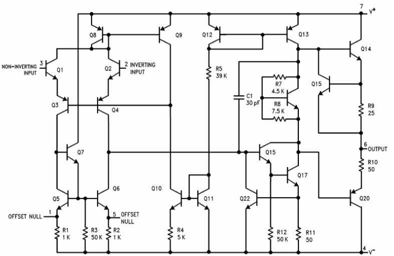
Operational amplifiers (OpAmps) play a critical role in instrumentation systems, where precision and accuracy in signal processing are essential.

Their functions include:

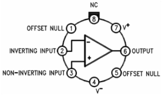
- **Signal Amplification**: amplify weak signals from transducers to a level suitable for further processing (e.g. thermocouples, strain gauges)
- **High Input Impedance**: minimize the loading effect on the transducer and between processing blocs
- **Filtering**: implement filters (e.g. low-pass, high-pass, band-pass) to attenuate noise/interference or to isolate specific frequency components of a signal
- **Offset Adjustment**: adjust the offset of a signal, ensuring that the signal is within the optimal range for subsequent stages.
- **Differential Amplification**: remove offsets, common-mode noise and referencing to ground differential signals (e.g. load cells)
- **Analog Signal Processing**: implement integration, differentiation, sum and other algebraic operations.

Operational Amplifiers

- OpAmps are built using VLSI techniques.
- The functional diagram and pin diagrams of a (classic) LM741 is shown below.

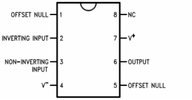


LMC Package
8-Pin TO-99
Top View



LM741H is available per JM38510/10101

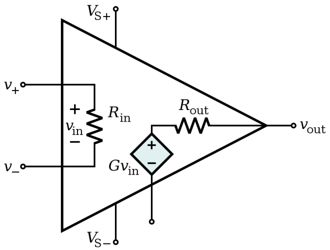
NAB Package
8-Pin CDIP or PDIP
Top View



Source: TI, LM741 SNOSC25D – MAY 1998 – REVISED OCTOBER 2015

Operational Amplifiers

OpAmps can be modeled (simplified) as:



Ideally:

- $R_{in} = \infty$
- $G = \infty$
- $R_o = 0$

Operational Amplifiers

Deviations from the ideal model:

- R_{in} can be as low as a few of hundreds $k\Omega$ (typically $M\Omega$)
- G can be a few thousands
- R_o of several $k\Omega$
- Input and output voltage does not reach the supply voltage (the margin can be up to 5 V).
  - Rail-to-rail Opamps allow voltages to swing up to supply voltages.
- Gain is reduced with frequency (product Gain-Bandwidth is constant)
- Slew rate is limited
- ...

Note

Datahseets are, to a certain extent, a collection of the non-idealities of opamps.
They are long, detailed and need to be consulted!

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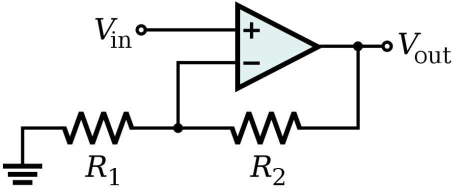
Operational Amplifiers - circuits

Non-inverting amplifier

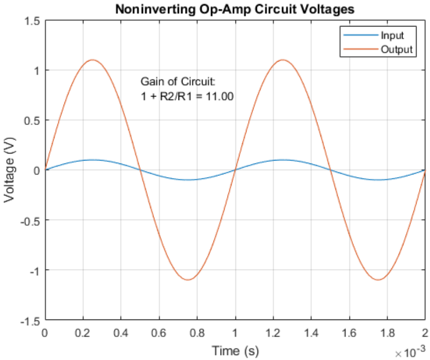


$V_o = V_{in}(1 + \frac{R2}{R1})$

Note that the gain is always greater than 1

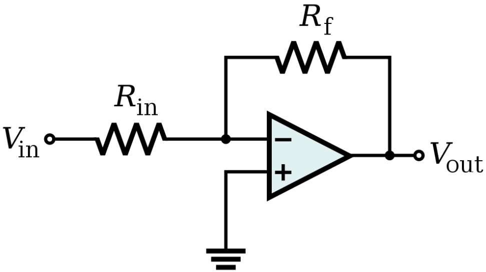
Operational Amplifiers - circuits

Non-inverting amplifier



Operational Amplifiers - circuits

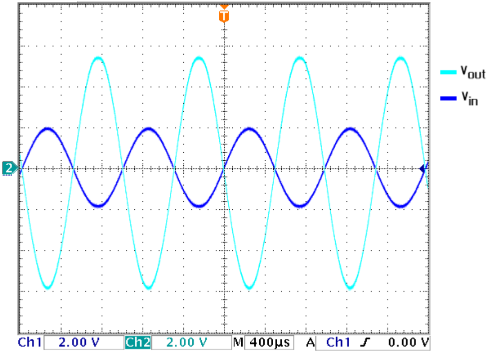
Inverting amplifier



$$V_o = -V_{in}\frac{R2}{R1}$$

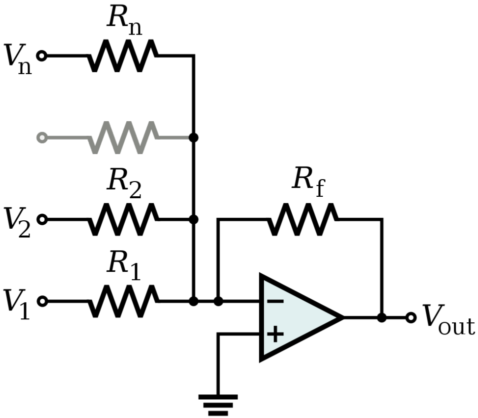
Operational Amplifiers - circuits

Inverting amplifier



Operational Amplifiers - circuits

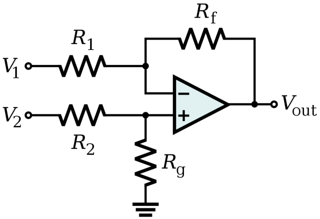
Summing amplifier



$$V_o = -R_f(\frac{V_1}{R_1} + \frac{V_2}{R_2} + ... + \frac{V_n}{R_n})$$

Operational Amplifiers - circuits

Difference amplifier



$V_o = -V_1 \frac{R_f}{R_1} + V_2 \left(\frac{R_g}{R_2+R_g}\right)\left(\frac{R_1+R_f}{R_1}\right)$

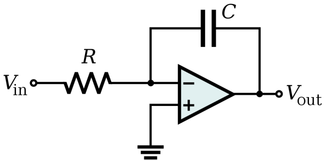
If $R_1 = R_2$ and $R_f = R_g$ then we have:

$$V_o = (V_2 - V_1)\frac{R_f}{R_1}$$

Note that common mode voltages (e.g. noise, pedestal voltages) are removed!

Operational Amplifiers - circuits

Integrator / Low-pass filter

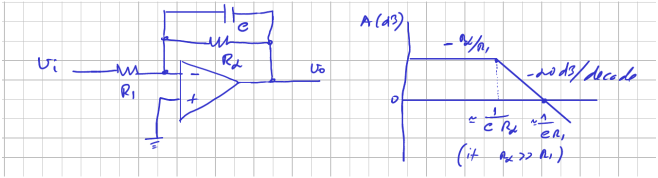


$$V_{out} = -\frac{1}{R \cdot C} \int_0^T V_{in} dt$$

Note that this circuit **does not work** in practice!
The output will saturate at one of the supply voltages.
Why?

Operational Amplifiers - circuits

Integrator - a practical circuit

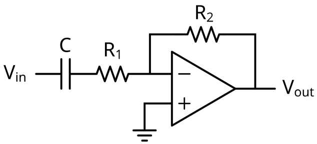


$$V_o = V_i \frac{R_2}{R_1}\left(\frac{1}{1+sR_2C}\right)$$

- R_2 provides a (negative) feedback path for DC.
- At low frequencies R_2 dominates the feedback impedance
- At high frequencies C dominates the feedback impedance

Operational Amplifiers - circuits

High-pass filter / Differentiator



- Capacitor moved with respect to LP/integrator filter
- At low frequencies the impedance of C is very high and thus the gain tends to zero
- At high frequencies the impedance of C tends to zero and the gain is $-\frac{R_2}{R_1}$
- The cut-off frequency is given by $\omega = \frac{1}{R_1 C}$

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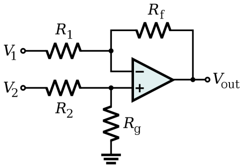
Instrumentation amplifier

Issues with the difference amplifier

- Match between resistor values is critical for the CMRR
  - $\frac{R_f}{R_1}$ must be equal to $\frac{R_g}{R_2}$
- Gain depends on pairs of resistances
- Input resistance is different on both inputs
- Circuit is sensible to the output resistance of signal sources
- Internal voltages can create issues



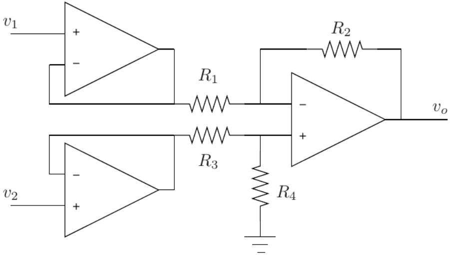
Instrumentation amplifier

- It is a difference amplifier
- Has a differential input and monopolar output
- High and symmetric input impedance
- Gain depends on single resistor

Instrumentation amplifier

IA implementations - input buffers

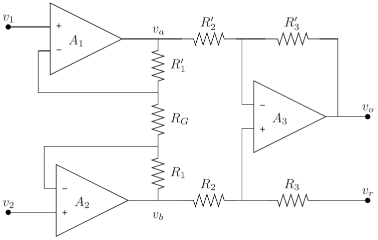
- Solves only some of the issues … which ones?



Instrumentation amplifier

IA implementations - three opamps - most popular

- Solves most of the problems before mentioned
- Gain depends on single resistor
- High R_{in} and equal at both inputs
- Low R_o

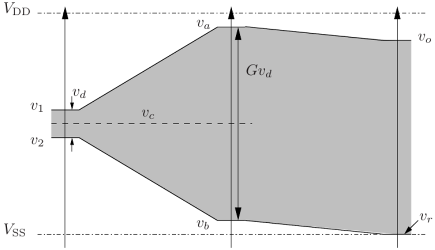


$$v_o = \frac{R_3}{R_2}\left(1 + 2\frac{R1}{R_G}\right)(v_2 - v_1) + v_r$$

Instrumentation amplifier

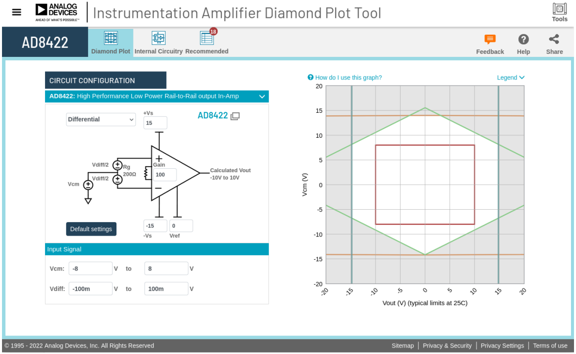
Three opamp IA - internal voltages

- Prone to internal saturation!
- **Limited gain when common mode voltage is low!**



Setting the proper operation

Analog Devices Instrumentation Amplifier Diamond Tool



https://tools.analog.com/en/diamond/

Some help on this tool: Kämmerer, C. (2017, September). The Secret of the Diamond Plot Tool. Analog Dialogue. https://www.analog.com/en/analog-dialogue/studentzone/studentzone-september-2017.html

Application example

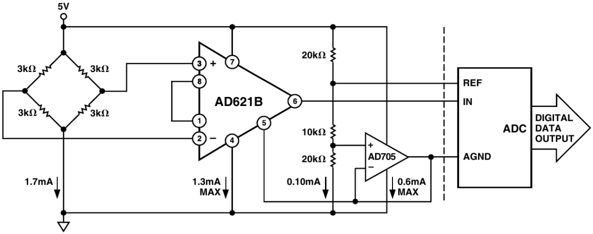


Figure 5. A Pressure Monitor Circuit which Operates on a 5 V Power Supply

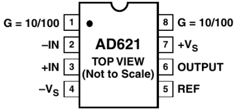


Table III. Practical 1% External Resistor Values for Gains Between 10 and 100

Desired Gain	Recommended 1% Resistor Value	Gain Error	Temperature Coefficient (TC)
10	∞ (Pins 1 and 8 Open)	*	5 ppm/°C max
20	4.42 kΩ	±10%	≈0.4 (50 ppm/°C + Resistor TC)
50	698 Ω	±10%	≈0.4 (50 ppm/°C + Resistor TC)
100	0 (Pins 1 and 8 Shorted)	*	5 ppm/°C max

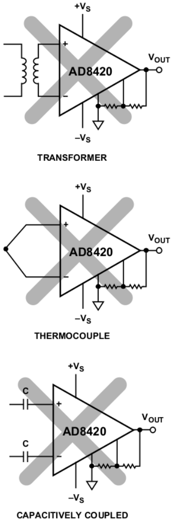
*Factory trimmed–exact value depends on grade.

Source: AD621 Datasheet

What is wrong?...

The AD8420
datasheet includes the figure on the right. What is wrong with these circuits?

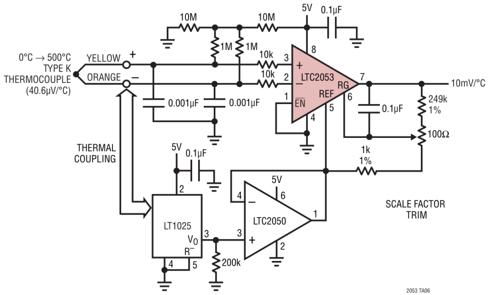
Check for the solutions in the datasheet)



Thermocouple interface

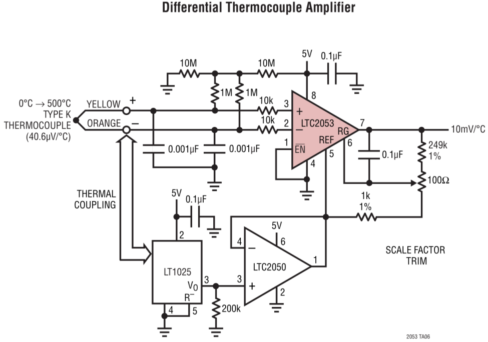
Example with LTC2053 Instrumentation Amplifier

Differential Thermocouple Amplifier



Thermocouple interface

Example with LTC2053 Instrumentation Amplifier



Features

- Biasing the thermocouple input to half-way power supply span
- Cold junction compensation (LT1025 is a circuit for cold junction compensation)

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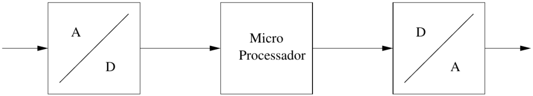
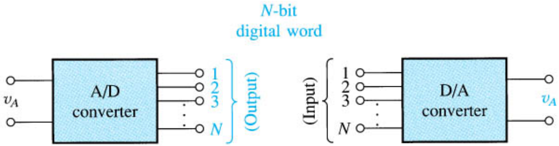
Instrumentation Chain



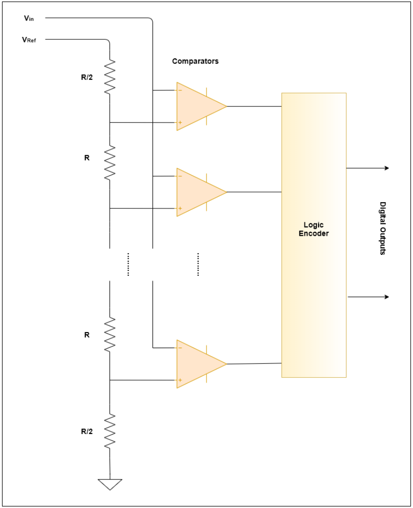


- Nowadays most of the instrumentation systems incorporate microprocessors/micro-controllers
- This requires the use of AD and DA converters to interface with the (analog) real world - sensors and actuators
- Since the principles of AD and DA are largely the same, we will mostly focus on AD (more common)

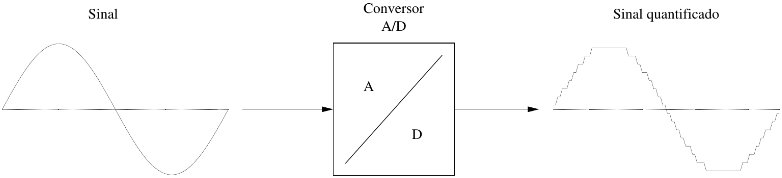
Example of DA converter circuit

There
are many ways to realize ADCs (and DACs), with different advantages/disadvantages

One of the (conceptually) more simple ones is the Flash ADC



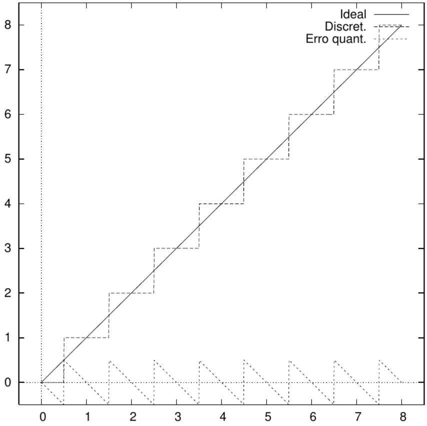
Signal Quantization



Accuracy difference between analog value and corresponding digital value. In the best case, it is bound by 1/2 LSB.

Quantization error Error resulting from the conversion of a continuous (analog) value into a discrete (digital) value.

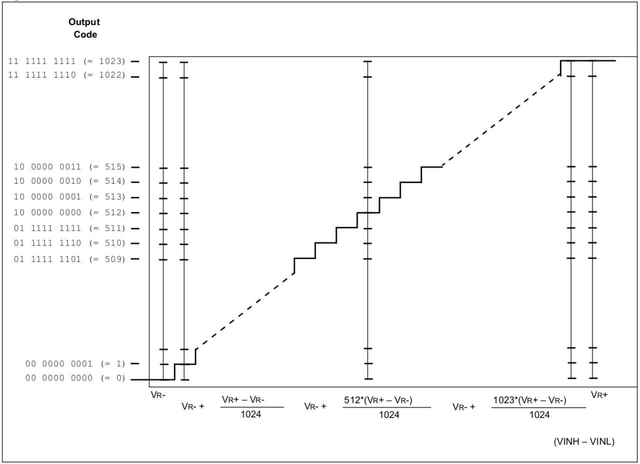
DACs and ADCs



$$
\begin{aligned}
\text{Quantization error} &= \text{Digital signal} - \text{Analog signal} \\
&= \text{Discrete signal} - \text{Continuous signal}
\end{aligned}
$$

PIC32 ADC transfer function

Figure 17-20: ADC Transfer Function



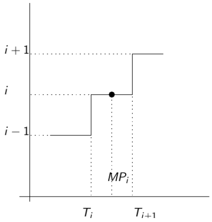
DACs and ADCs

Resolution Smallest change in the ADC input between one transition and the next transition.

Dynamic range Ratio between the range of values on the converter input and its resolution.

- Depends on the number of bits, n
- $G = \frac{V_{max} - V_{min}}{q}$, where $q = \text{LSB}$
- $2^n - 1$ or $20\log(2^n - 1)$ [dB]

Midpoint of a code



- T_i: value where converter makes the transition from code $i-1$ to code i
- T_{i+1}: value where converter makes the transition from code i to code $i+1$
- The converter outputs the code i when input value $\in [T_i, T_{i+1}]$
- $MP_i = \frac{T_i + T_{i+1}}{2}$

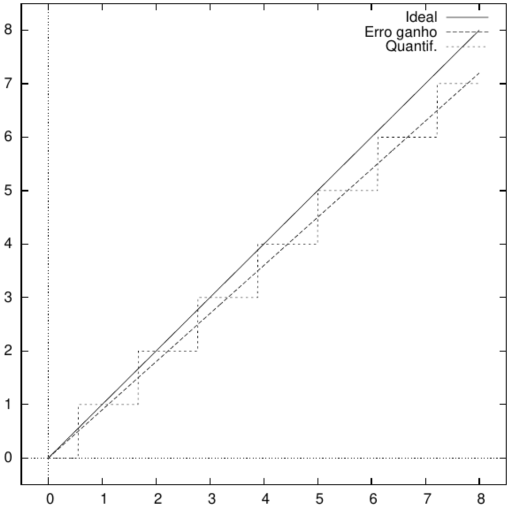
DACs and ADCs

Offset Error (or zero error) deviation of the actual ADC's transfer function from the ideal straight line at zero input voltage.

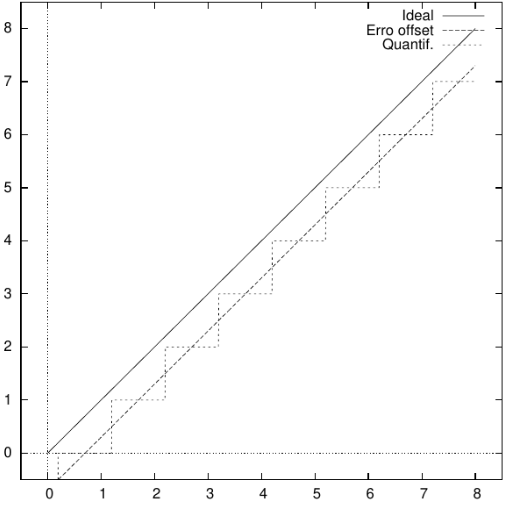
Scale error (or gain error) deviation of the last output step's midpoint from the ideal straight line, after compensating for offset error..

Hysteresis Difference between the transition values at two consecutive levels when the transition is made in opposite directions.

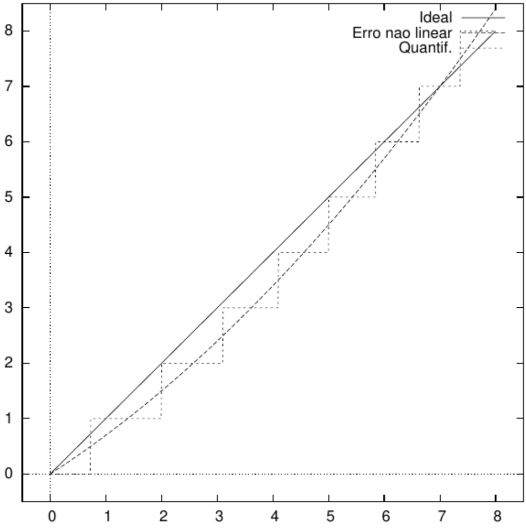
Scale error



Offset error



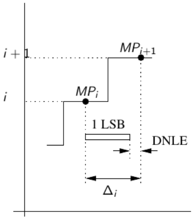
Non-linearity Error



DACs and ADCs

Linearity Approximation of the Central Points of each level to a straight line. It is measured by Integral Non-Linearity Error (INLE) and Differential Non-Linearity Error (DNLE)

DNLE



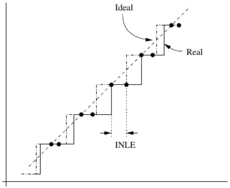
DNLE, Diferential Non-Linearity Error

$DNLE = \max_i(MP_{i+1} - MP_i - LSB)$

$DNLE = \max_i(\Delta_i - LSB)$

$DNLE = \max_i \left(\frac{\Delta_i}{LSB} - 1 \right), \quad \Delta_i = MP_{i+1} - MP_i$

INLE



- INLE: Integral Non-Linearity Error
  - MP_i: Actual Code Midpoints
  - MPI_i: Ideal Code Midpoints

$$INLE = \max_i(MP_i - MPI_i)$$

DACs and ADCs

Settling Time For a DAC, settling time is the interval between a command to update (change) its output value and the instant it reaches its final value, within a specified percentage.[1]

Conversion rate Number of conversions (DA or AD) that a converter can execute in a second.

Temperature coefficient Measure of the variation of characteristics (including errors) with temperature

[1] Maxim Integrated. (2002). Types of ADCs and DACs. Maxim Integrated. https://www.maximintegrated.com/en/design/technical-documents/tutorials/6/641.html

DACs and ADCs

PSRR, Power Suplly Rejection Ratio defines the ability of the comparator to reject power supply noise (relative to the inputs) when making a differential comparison between the inputs. A comparator with a PSRR of 60 dB will interpret 1-V power supply noise the same as 1 mV of differential input voltage.[2]

[2] Feddeler, J., and Lucas, B. (2003). *ADC Definitions and Specifications* (Application Note AN2438/D; p. 22). Freescale Semiconductor, Inc..

ENOB

Signal-to-Noise Ratio in a perfect signal, quantified with n bits:

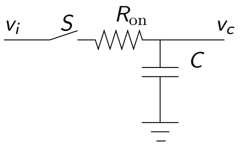
$$\mathrm{SNR} = 6.02n + 1.76$$

ENOB = Effective Number of Bits

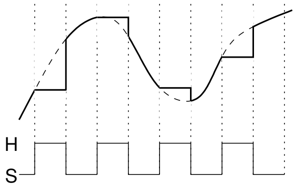
$$\text{ENOB} = \frac{\mathrm{SNR} - 1.76}{6.02}$$

ENOB = Indication of how many bits are valid (effective) in the digital signal

Sample and Hold circuits

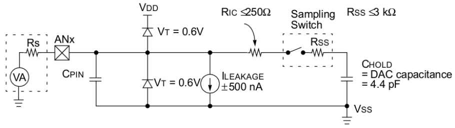


Switch	State	Action
Closed	Sample	v_c follows v_i
Open	Hold	v_c is constant



Real case: PIC32 S/H circuit

Figure 17-22: 10-bit ADC Analog Input Model



Note: The CPIN value depends on the device package and is not tested. The effect of the CPIN is negligible if Rs ≤5 kΩ.

Legend:

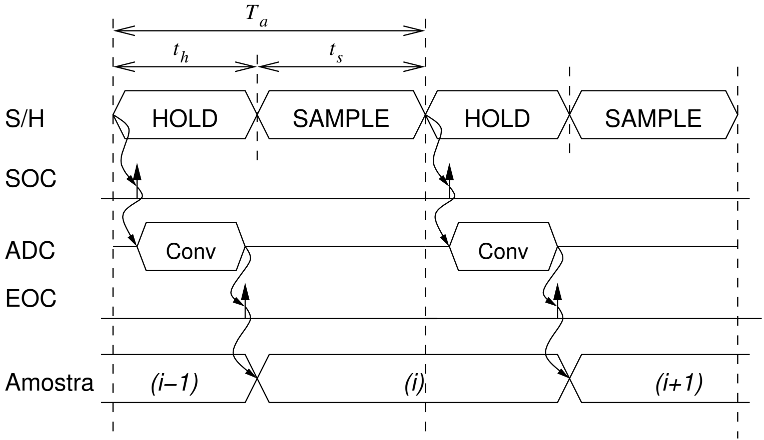
CPIN = input capacitance
RSS = sampling switch resistance
Rs = source resistance
ILEAKAGE = leakage current at the pin due to various junctions
VT = threshold voltage
RIC = interconnect resistance
CHOLD = sample/hold capacitance

[Microchip, PIC32 Reference Manual, Section 17]

Sample phase duration is crucial

- Signal source output resistance + multiplexer circuitry + switching circuitry form an RC integrator circuit
- Sampling time must allow the sampling capacitor C_{HOLD} to "fully charge" to the signal voltage value at the input pin
- E.g. $t_s = \tau$: 63.2% $t_s = 3\tau$: 95.0% $t_s = 5\tau$: 99.3%

Sample and Hold circuits



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- Paul Horowitz, Winfield Hill, The Art of Electronics, 3rd Edition, ISBN: 9780521809269
- Microchip PIC32 data converters Developer Help (https://developerhelp.microchip.com/xwiki/bin/view/products/data-converters/, accessed 2024/09/02)
- The ABC of ADCs: Understanding how ADC errors affect performance (AN 748). Dallas/Maxim.

Note: some slides were adapted for the "Electronic Instrumentation Systems" Course Unit and were originally produces by Prof. Pedro Fonseca