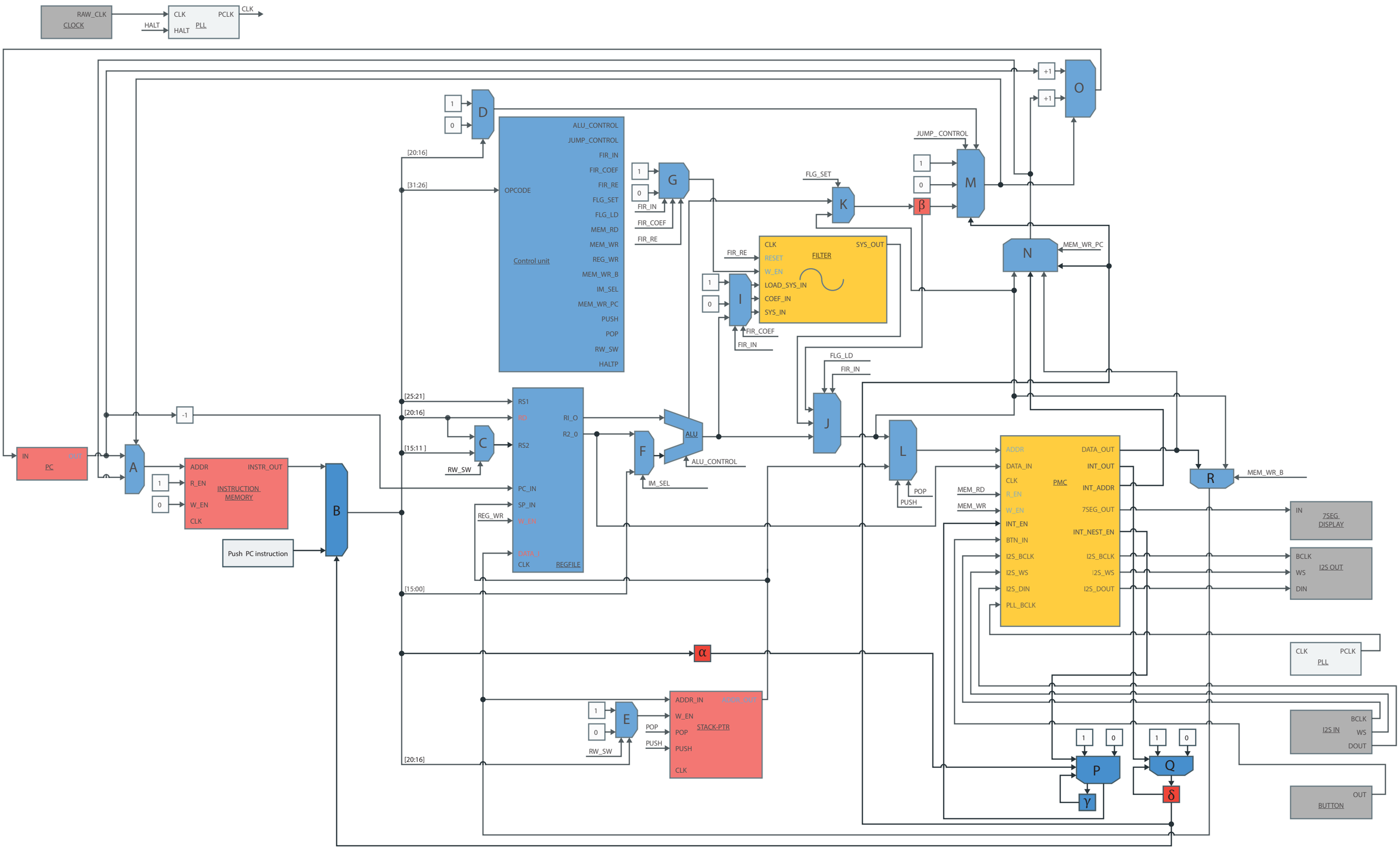
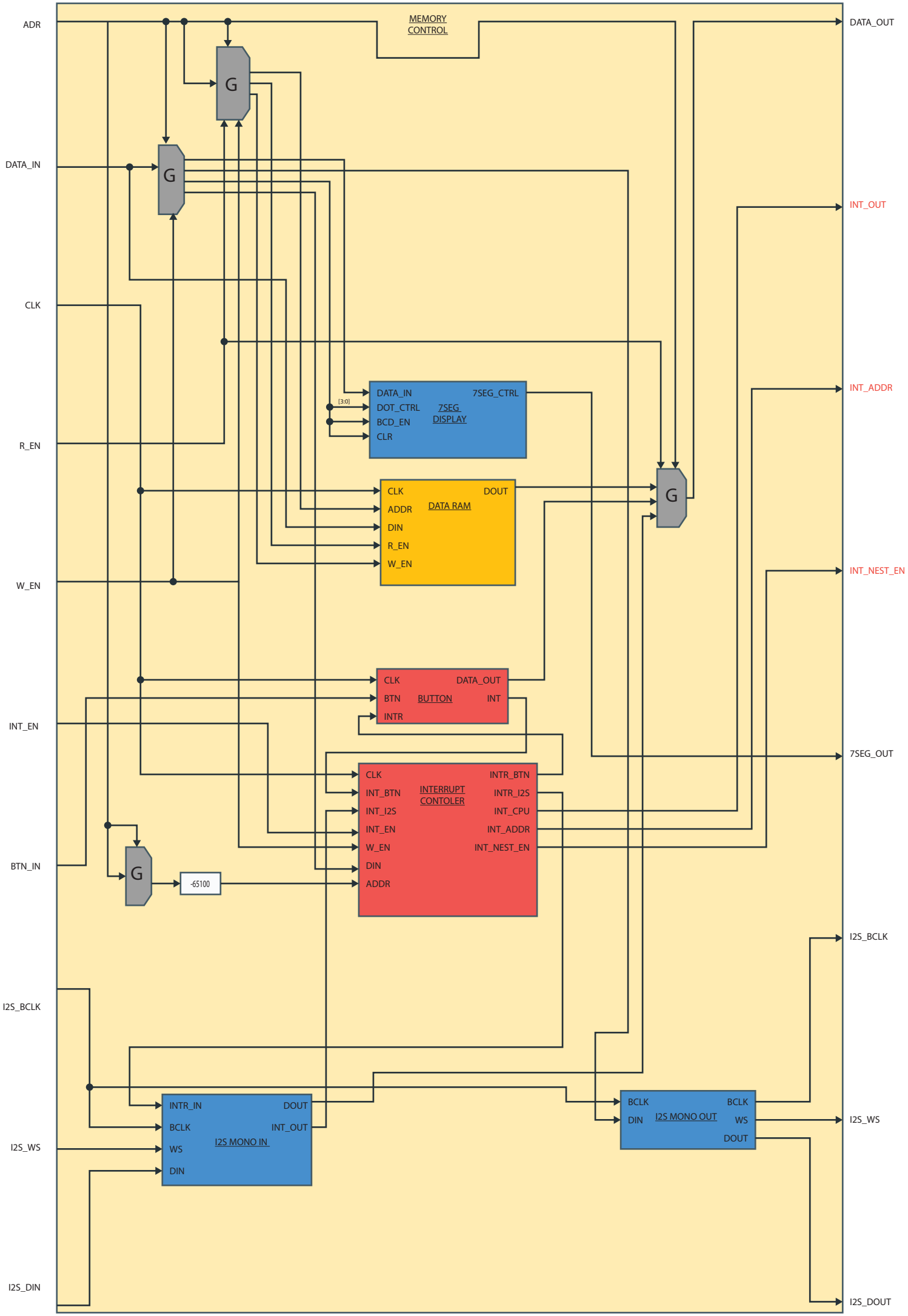

RAW_CLK
CLOCK
CLK
PCLK
HALT
PLL
HALT
CLK
IN
OUT
PC
A
ADDR
INSTR_OUT
R_EN
INSTRUCTION MEMORY
W_EN
CLK
Push PC instruction
B
D
ALU_CONTROL
JUMP_CONTROL
FIR_IN
FIR_COEF
FIR_RE
FLG_SET
FLG_LD
MEM_RD
MEM_WR
REG_WR
MEM_WR_B
IM_SEL
MEM_WR_PC
PUSH
POP
RW_SW
HALTP
OPCODE
Control unit
[20:16]
[31:26]
[25:21]
[15:11]
[15:00]
G
K
M
O
N
I
J
L
R
C
F
ALU
ALU_CONTROL
RS1
RD
RS2
RI_O
R2_0
PC_IN
SP_IN
DATA_I
REGFILE
FILTER
SYS_OUT
LOAD_SYS_IN
COEF_IN
SYS_IN
PMC
DATA_OUT
DATA_IN
INT_OUT
INT_ADDR
7SEG_OUT
INT_NEST_EN
INT_EN
BTN_IN
I2S_BCLK
I2S_WS
I2S_DIN
I2S_DOUT
PLL_BCLK
7SEG DISPLAY
I2S OUT
BCLK
WS
DIN
PLL
I2S IN
DOUT
BUTTON
E
STACK-PTR
ADDR_IN
ADDR_OUT
P
Q
α
β
γ
δ
+1
-1


ADR
DATA_IN
CLK
R_EN
W_EN
INT_EN
BTN_IN
I2S_BCLK
I2S_WS
I2S_DIN
MEMORY CONTROL
G
G
G
G
G
DATA_IN
DOT_CTRL
BCD_EN
CLR
[3:0]
7SEG DISPLAY
7SEG_CTRL
CLK
ADDR
DIN
R_EN
W_EN
DATA RAM
DOUT
CLK
BTN
INTR
BUTTON
DATA_OUT
INT
CLK
INT_BTN
INT_I2S
INT_EN
W_EN
DIN
ADDR
INTERRUPT CONTOLER
INTR_BTN
INTR_I2S
INT_CPU
INT_ADDR
INT_NEST_EN
-65100
INTR_IN
BCLK
WS
DIN
I2S MONO IN
DOUT
INT_OUT
BCLK
DIN
I2S MONO OUT
BCLK
WS
DOUT
DATA_OUT
INT_OUT
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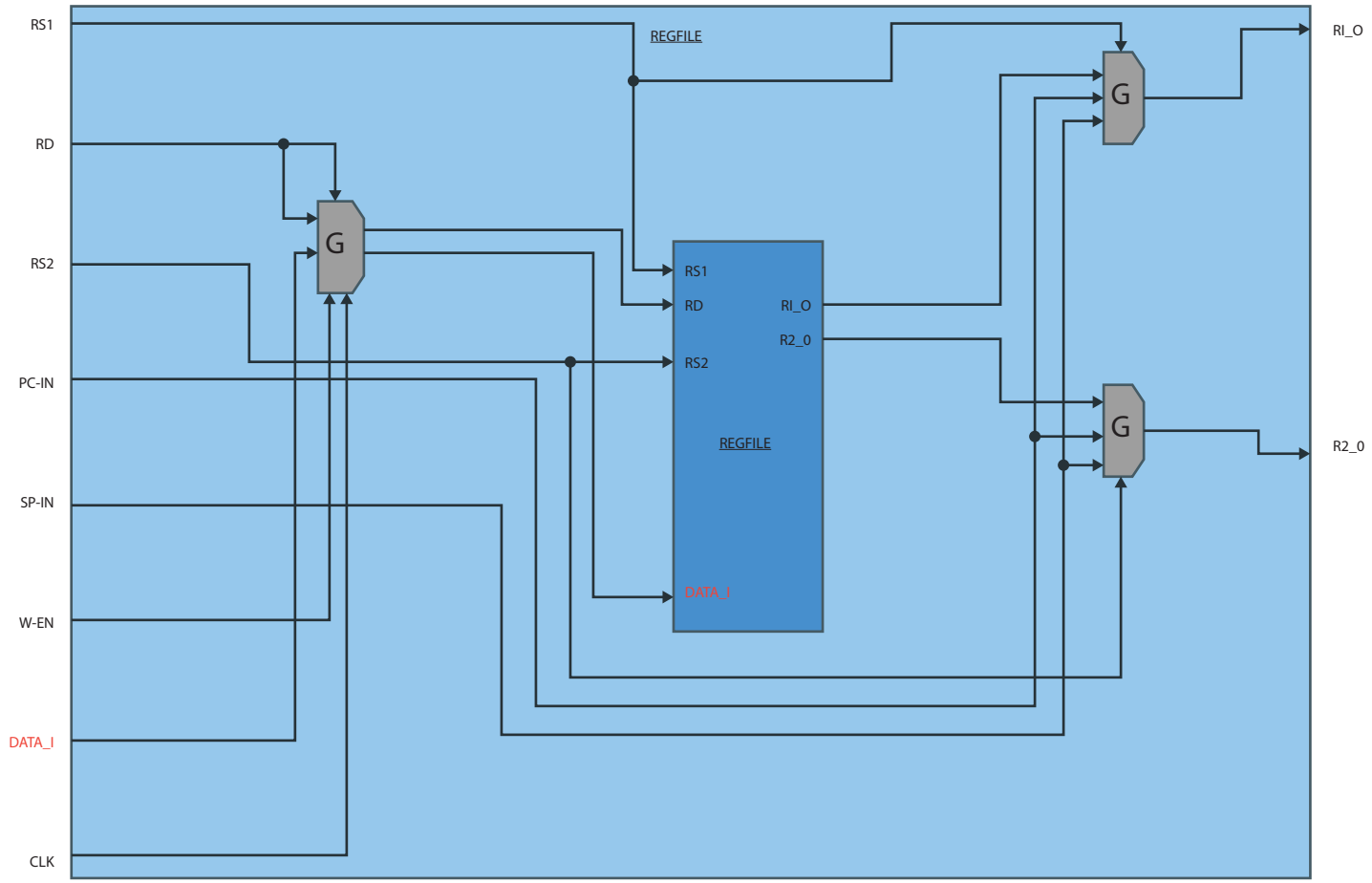
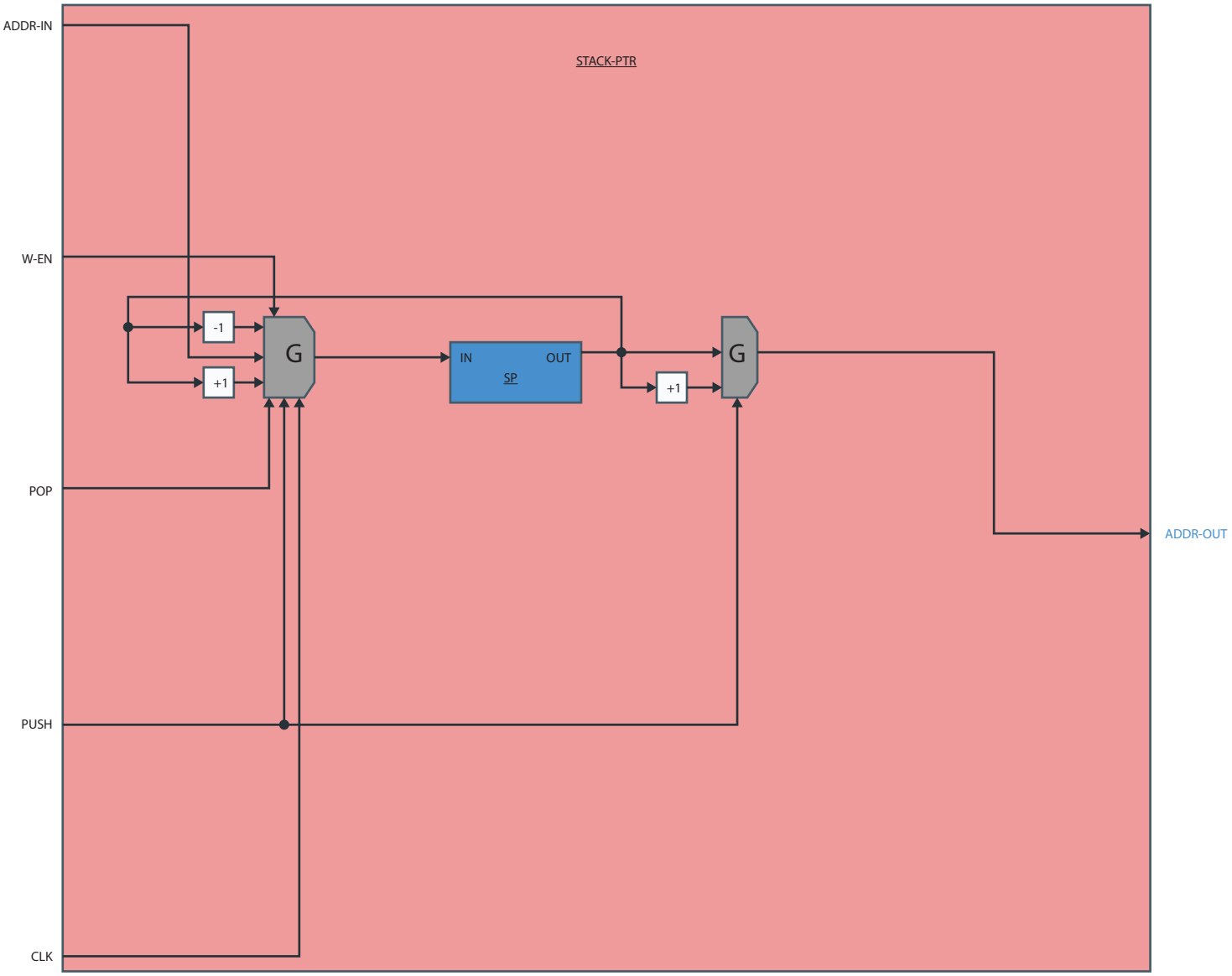
INT_NEST_EN
7SEG_OUT
I2S_BCLK
I2S_WS
I2S_DOUT


RS1
RD
RS2
PC-IN
SP-IN
W-EN
DATA_I
CLK
REGFILE
G
RS1
RD
RS2
RI_O
R2_0
REGFILE
DATA_I
G
G
RI_O
R2_0


ADDR-IN
STACK-PTR
W-EN
-1
+1
G
IN
OUT
SP
+1
G
POP
ADDR-OUT
PUSH
CLK