

HP's 5 1/4-Inch Winchester Disc Drive Service Documentation



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Section I The Winchester Disc Drive

Chapter 1

General Information

- General Description
- Technical Specifications

General Description

The Winchester disc drive is a random access storage device utilizing up to three non-removable 5 1/4-inch discs or platters as storage media. Each surface employs one movable head to service 153/306 data tracks. The platter configurations (triple, dual, and single) of the Winchester drives used in the 913X products appear next:

- ST506 - Dual-Platter 5-Mbyte (early units)
- ST406 - Single-Platter 5-Mbyte (improved track density)
- ST412 - Dual-Platter 10-Mbyte (improved track density)
- ST419 - Triple-Platter 15-Mbyte (improved track density)

Mechanical and contamination protection for the heads, actuator, and discs is provided by an impact-resistant aluminum enclosure. Both electronic printed circuit assemblies are mounted outside this enclosure. A self-contained recirculating system supplies clean air through a 0.3-micron filter. A second port in the filter assembly allows pressure equalization with ambient air without chance of contamination.

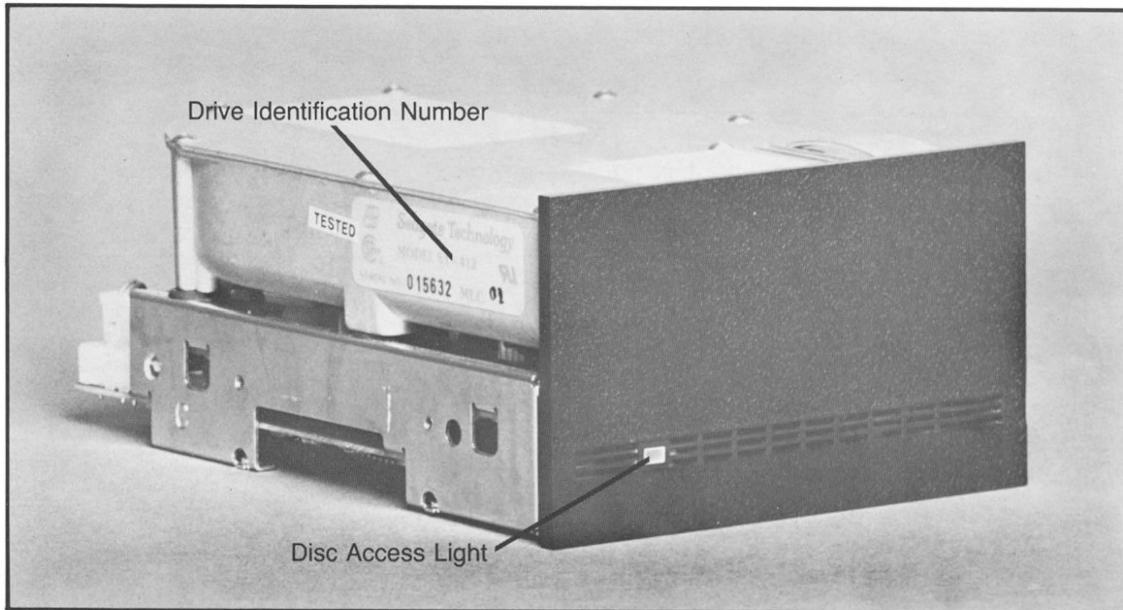


Figure 1-1. The Winchester Disc Drive

Technical Specifications

Listed below are the electrical and physical specifications for the 5 1/4-inch Winchester disc drive.

Formatted Storage Capacities:

Standard = 4.6 Mbyte – 4-Volume

("A" versions only)

Option 10 = 4.8 Mbyte – Single-Volume

("A" versions only)

Standard = 4.8-Mbyte – Single-Volume

("V" versions only)

Option 004 = 4.6-Mbyte – 4-Volume

("V" versions only)

Standard = 9.68 Mbyte – Single-Volume

("B" versions only)

Triple-Platter Capacity = 14.57 Mbyte

("XV" versions only)

Average Access Time: 85 ms for the single-platter 5-Mbyte and dual-platter 10-Mbyte drive.

170 ms for the dual-platter 5-Mbyte.

Data Transfer Rates:

Sustained Average is 50 Kbytes/s. Your system transfer rate may vary due to your mainframe.

Rotational Speed: 3600RPM ± 1 %

Environmental Specs:

See the tabbed section for product environmental specs.

NOTE

The Winchester drive has no write protect capability. Therefore, caution must be used to avoid erasing or initializing over data you want to keep.

CAUTION

THE WINCHESTER DISC IS A DELICATE INSTRUMENT.
MECHANICAL SHOCK CAN MISALIGN THE READ/WRITE HEADS
RESULTING IN READ ERRORS AND/OR DAMAGED DISCS
WHETHER OR NOT THE DISC IS OPERATING.

Chapter 2

Theory of Operation

- Winchester Disc Drive Theory of Operation
- Drive Electronics Theory of Operation
- Disc Drive Adjustments

Winchester Disc Drive Theory of Operation

Functional Characteristics

The following description is given for the 5, 10, and 15-Mbyte drives. The different configurations are presented in the following table:

Table 2-1. Winchester Configurations

	5 Mbyte Dual Platter	5 Mbyte Single Platter	10 Mbyte Dual Platter	15 Mbyte Triple Platter
Capacity (Mbyte)	5	5	10	15
Cylinders	153	306	306	306
Platters	2	1	2	3
Heads	4	2	4	6

The Winchester drive assembly consists of read/write electronics, read/write heads, head positioning actuator, media, and air filtration system. These components perform the following functions:

- Interpret and generate control signals.
- Position the heads over the desired tracks.
- Read and write data.
- Provide a contamination free environment for the media and heads.

Read/Write Control Electronics

The read/write electronics are packaged on two PCAs. One PCA contains circuitry which provides the following:

- Index detection.
- Head positioning.
- Read and write capability.
- Drive speed sensing.
- Head selection.
- Write fault detection.
- Stepper motor control.
- Drive selection.
- Track zero detection.

The second PCA mounted under the one just described provides power and speed control to the spindle motor.

Drive Mechanism

A brushless DC motor rotates the spindle at 3600 rpm. The spindle is driven directly (no belt or pulley is used). A brake is used to provide a fast stop for the spindle motor when power is removed. This minimizes the time that the heads are in contact with the platter(s) as the motor slows.

Air Filtration System

The discs and read/write heads are fully enclosed in a module using an integral recirculation air system with an absolute filter which maintains a clean environment. Integral to the filter is a port which also permits pressure equalization with the ambient air without contaminant entry. The filter is not a replaceable assembly.

Head Positioning Mechanism

The read/write heads are mounted on a ball bearing support which is positioned by a split band actuator connected to the 2-phase stepper motor shaft.

Read/Write Heads and Discs

The storage disc consists of a lubricated thin magnetic oxide coating on one, two, or three 130mm (5.125 in.) diameter aluminum substrates. This coating formulation together with the low load force/low mass (9 grams) Winchester type flying heads, permits reliable head/media contact during start and stop operations. For each platter, there are two read/write heads (one for each disc surface); each head accesses 306 tracks for the 5, 10, or 15-Mbytes of data storage (153 tracks for the earlier ST506 drives).

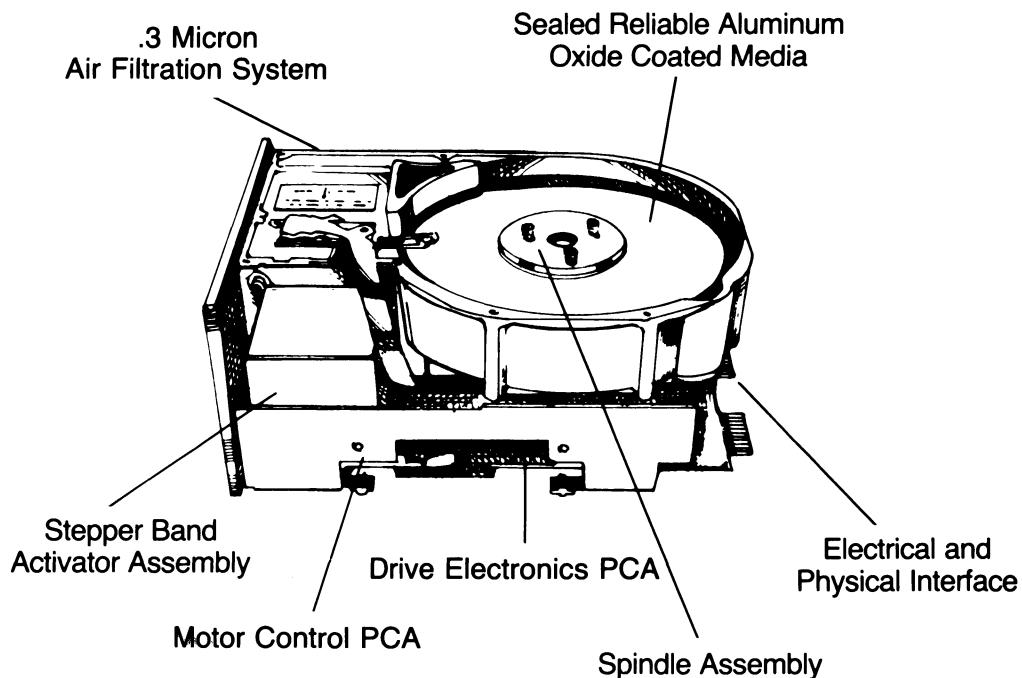


Figure 2-1. Winchester Drive Structure

Functional Operation

Power Sequencing

The +5 VDC and +12 VDC can be applied in any order. The spindle motor requires +12 VDC for operation. A motor speed sense circuit counts 512 revolutions of the disc. After 512 revolutions, the heads automatically recalibrate to track 0. For this recalibration to occur, the step input must be inactive. Track 0, SEEK COMPLETE, and READY signals are all set true sequentially (refer to Figure 2-2). The drive will not perform read, write or seek operations until READY is set true.

Drive Selection

The drive select allows up to four drives to be connected to a controller PCA. The select lines are wire-OR'ed so that the one drive is always selected.

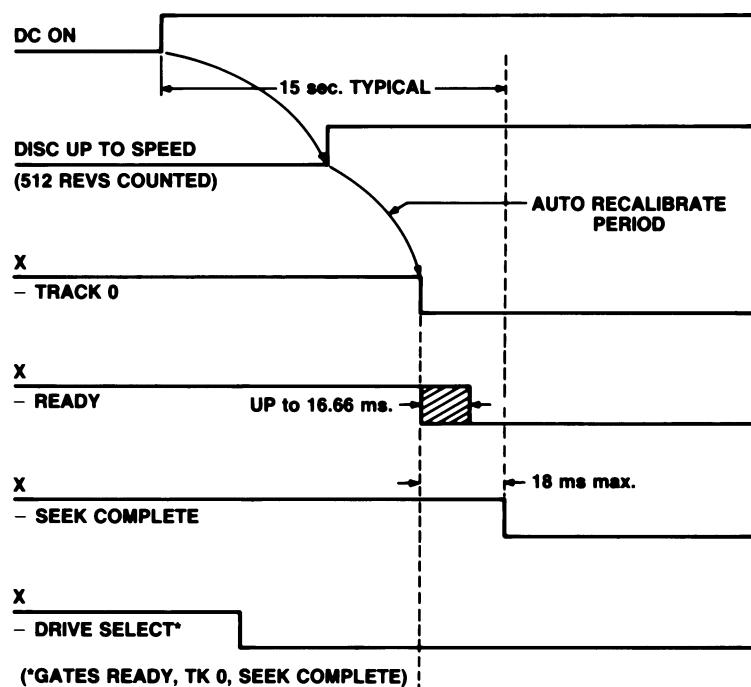


Figure 2-2. Power-Up Sequence

Track Accessing

Read/Write head positioning is accomplished by the following items after the drive is in the READY condition with SEEK COMPLETE true.

- Deactivating the WRITE GATE line.
- Activating the appropriate drive select line.
- Selecting the appropriate direction.
- Pulsing the STEP line.

Each step pulse causes the heads to move either in one track or out one track depending on the level of the DIRECTION line. A true on the DIRECTION line causes the heads to seek inward toward the spindle; a false causes a seek outward toward track 0 (outer edge of platter).

Head Selection

Any of the heads can be selected by placing the head's binary address on the three HEAD SELECT lines.

Read Operation

Reading data from a disc is accomplished by the following items after assuring the drive is READY.

Deactivating the WRITE GATE line.

Activating the appropriate DRIVE SELECT line.

Selecting the appropriate head.

Write Operation

Writing data onto the disc is accomplished by the following after assuring the drive is READY and that no write fault conditions exist.

Activating the appropriate DRIVE SELECT line.

Selecting the appropriate head.

Activating the WRITE GATE line and placing data on the WRITE DATA line.

Drive Electronics Theory of Operation

The drive electronics PCA contains the head select, read/write circuitry, and head positioning circuitry.

One to three head select lines are used to select one of two, four, or six heads. All the heads step simultaneously.

The read circuitry amplifies the output of the selected read head, provides noise rejection, wave shaping, and outputs the differential read circuit voltages to the controller PCA.

The write circuitry accepts the differential write data voltage from the controller. The write circuitry is enabled by the WRITE GATE from the controller and provides the write current source. The Reduce WRITE CURRENT line selects the write current level. The write circuitry also provides precompensation to the write data.

The drive select allows up to four drives to be connected to a controller PCA. The select lines are wire-OR'ed so that the one drive is always selected.

The STEP and DIRECTION inputs to the head positioning circuitry from the controller PCA are converted to signals which drive the 2-phase stepper motor. The SEEK COMPLETE line then signals the controller PCA that the seek operation is completed. The READY line indicates to the controller that the motor speed is correct and that the head is ready. The DIRECTION line, during a step, is low when the heads step toward track 0 and pulses once for each track stepped. There is an optical sensor on the stepper motor which indicates when track 0 is detected. The INDEX signal is provided by a HALL-effect switch on the disc rotor.

The fault detect circuitry prevents writing and head-stepping activity when a fault condition is detected. The fault detect circuitry is enabled under the following conditions:

Power supplies are out of tolerance.
 Multiple heads are selected.
 No head selected.
 WRITE CURRENT but with no WRITE GATE.
 WRITE GATE but no WRITE CURRENT.

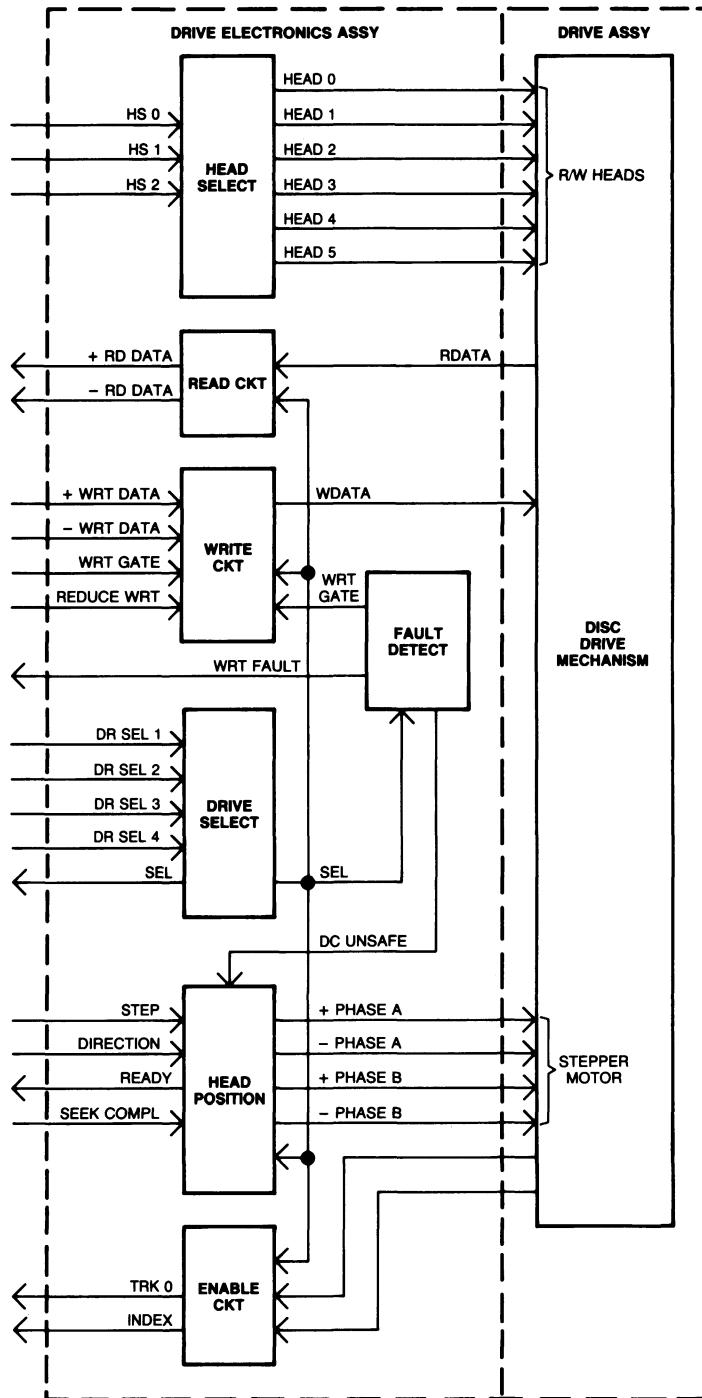


Figure 2-3. Winchester Drive Electronics PCA Block Diagram

Winchester Disc Drive Adjustments

There are three adjustments on the Winchester drive which may be performed in the field. They are as follows:

1. Brake adjustment (on earlier Winchester drives)

This should be performed whenever:

- a. The Brake/Index assembly is replaced.
- b. The unit won't come READY (won't come up to speed).
- c. A squeal or rubbing noise is heard coming from the Winchester.

2. Index Sensor Adjustment

This should be performed whenever:

- a. The brake is adjusted.
- b. Data errors occur frequently.
- c. Motor speed increases too rapidly.

3. Motor Speed Adjustment

This should be checked and performed if necessary whenever data errors occur frequently.

Equipment Required

HP 5308A 75 MHz Timer/Counter or equivalent

5/64" Allen Wrench or the proper Torx driver – Torx set P/N 8710-1426

Feeler Gauge (0.010 in. and 0.030 in.)

Brake Adjustment (Earlier Winchester Drives)

To adjust the brake on the Winchester drive, first disconnect the disc memory from any AC power source. Refer to Chapter 2 of Section II (Assembly Access) and remove the top cover, Winchester controller PCA, Winchester drive assembly and drive electronics PCA. Place the drive assembly on a clean dry surface bottom side up. Check the clearance between the drive hub and the brake pad and adjust if necessary for a clearance of 0.010 inch. To do this, loosen the two screws (A) shown in Figure 2-4, place the 0.010 inch feeler gauge between the hub and the brake pad and move the brake/index/ground assembly toward the hub until snug. Tighten the screws previously loosened and proceed to the index sensor adjustment.

Index Sensor Adjustment

To perform this adjustment, first disconnect the disc memory from any AC power source. Refer to Chapter 2 Section II (Assembly Access) and remove the top cover, Winchester Controller PCA, Winchester drive assembly and drive electronics PCA. Place the drive assembly on a clean, dry surface, bottom side up. Check and adjust the clearance between the index sensor and metal tab on the hub shown in Figure 2-5. Adjust the index sensor clearance by loosening the two screws shown in Figure 2-5 and inserting the 0.030 inch feeler gauge between the index sensor and the metal tab. Tighten the two retaining screws previously loosened. Reassemble the drive assembly.

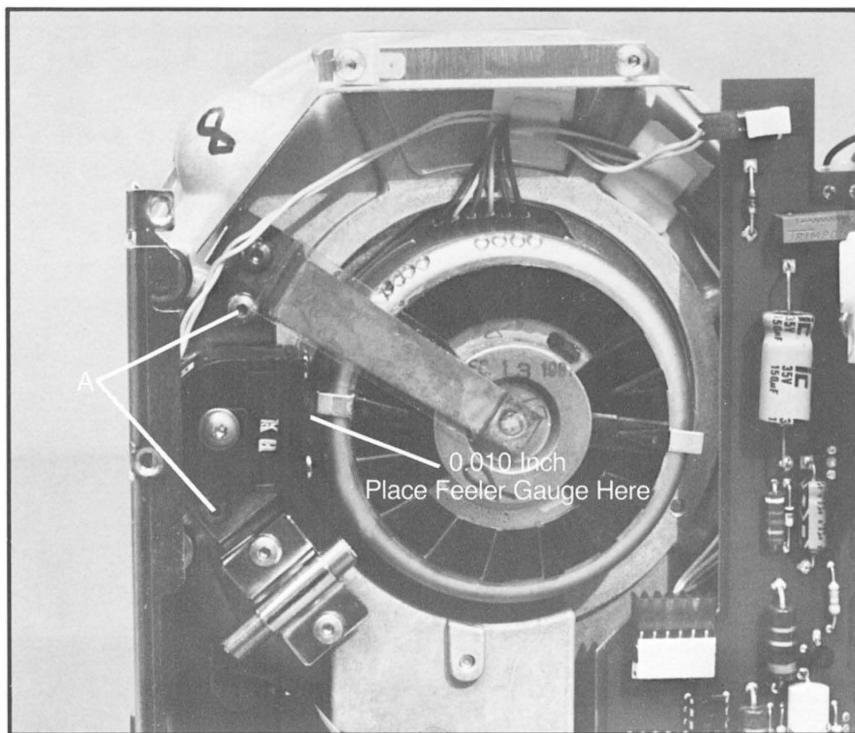


Figure 2-4. Brake/Index Assembly

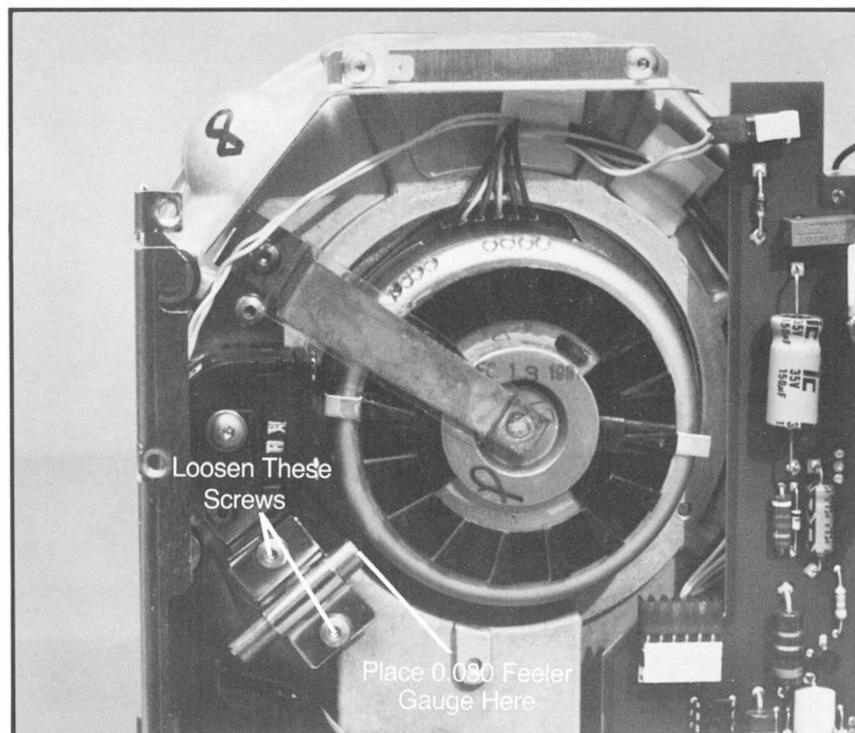


Figure 2-5. Index Sensor Adjustment

Motor Speed Adjustment

To adjust the motor speed on the Winchester drive, first disconnect the disc memory from any AC power source. Refer to Chapter 2 in Section II (Assembly Access) and remove the top cover, Winchester Controller PCA and Winchester drive support plate, leaving the drive attached to the support plate. Be sure to have the DC power connected to the Winchester drive electronics PCA. Carefully place the Winchester support plate on its side as shown in Figure 2-6.

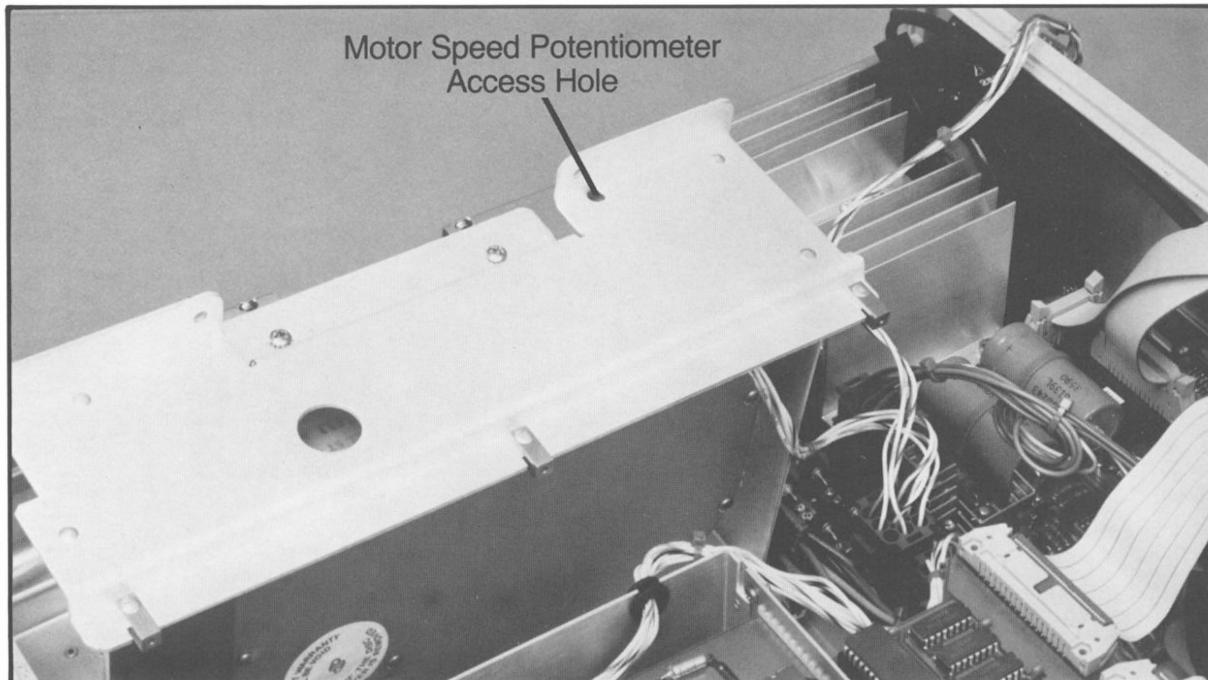


Figure 2-6. Winchester Motor Speed Adjustment Test Setup

Connect the 5308A as follows:

Channel B input to the Input Pulse test point
Ground to TP10

Set the controls on the 5308A as follows:

Trigger to (trigger on leading edge)
Attenuators to COM B
X1
AC
PER B
Time Base to 1 μ S

Apply power to the Disc Memory

Observe the 5308A display and, if necessary, adjust the potentiometer shown in Figure 2-6 for a 001666.6 μ s period ($\pm 1\% \text{ MAX.}$)

Disconnect all AC power and reassemble the unit.

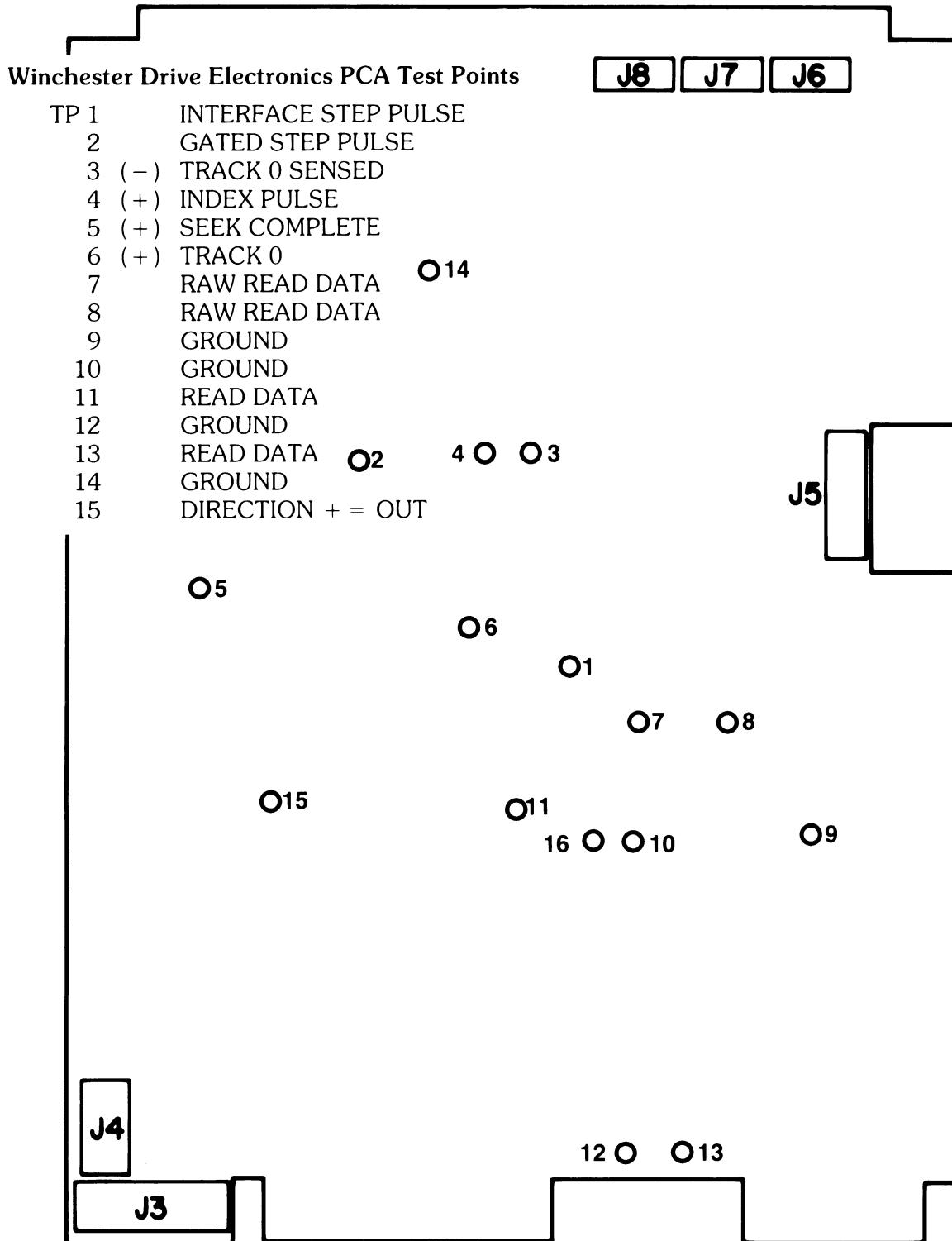


Figure 2-7. Drive Electronics PCA (P/N 09135-69502) Test Points and Connector Locations

Drive Electronics PCA - P/N 09133-69101 or 09133-69103

The following test point description along with the Figure 2-8 is presented as a troubleshooting aid in isolating the Drive Electronics assembly. The Drive Electronics assembly is used with the 406 drive. Check the part number of the Drive Electronics assembly to be sure you have the right assembly.

Test Point 3 (Track Zero Sensor)

Test Point 3 can be used to monitor the Track Zero sensor. A high logic level is a valid Track Zero indication.

Test Point 4 (Index Sensor)

The Point 4 can be used to monitor the Index Sensor. A high logic level is a valid Index indication. Only the leading edge of the pulse can be considered valid. The typical signal at Test Point 4 should resemble the signal shown in Figure 2-8.

Test Point 5 (Seek Complete)

Test Point 5 can be used to monitor the Seek Complete line. A high logic level is a valid Seek Complete indication.

Test Point 6 (True Track Zero)

Test Point 6 can be used to monitor the Track Zero signal that is gated to the host controller. A high logic level is a valid Track Zero indication.

Test Points 7 & 8 (Differential Read Filter)

Test Points 7 & 8 can be used to observe the differential read data. The typical amplitude of the signal resulting from adding the two channels is 300 millivolts. Test Point 9 should be used as ground to reduce noise.

Components of 1.25, 1.66, and 2.5 MHz should be observed. A full track record of high frequency data (0000 or 1111) should resemble the one shown in Figure 2-8.

Test Points 11 & 13 (Read Data)

Test Points 11 & 13 can be used to observe the Read Data from the Time Domain Filter. Trigger on Test Point 11 and monitor the delay at Test Point 13. Typically, the delay observed should be 50 nanoseconds. A full track record of high frequency data (0000 or 1111) should resemble the one shown in Figure 2-8.

Test Point 20 (5V Pullup)

Test Point 20 is a 5 volt pullup location. To use the pullup the line at J01 must be cut.

Test Point 9,10,12,14,15,16,21,22, & 23 (Convenience Grounds)

For any of the above functions, use the ground test point that is in the closest proximity to the active test point.

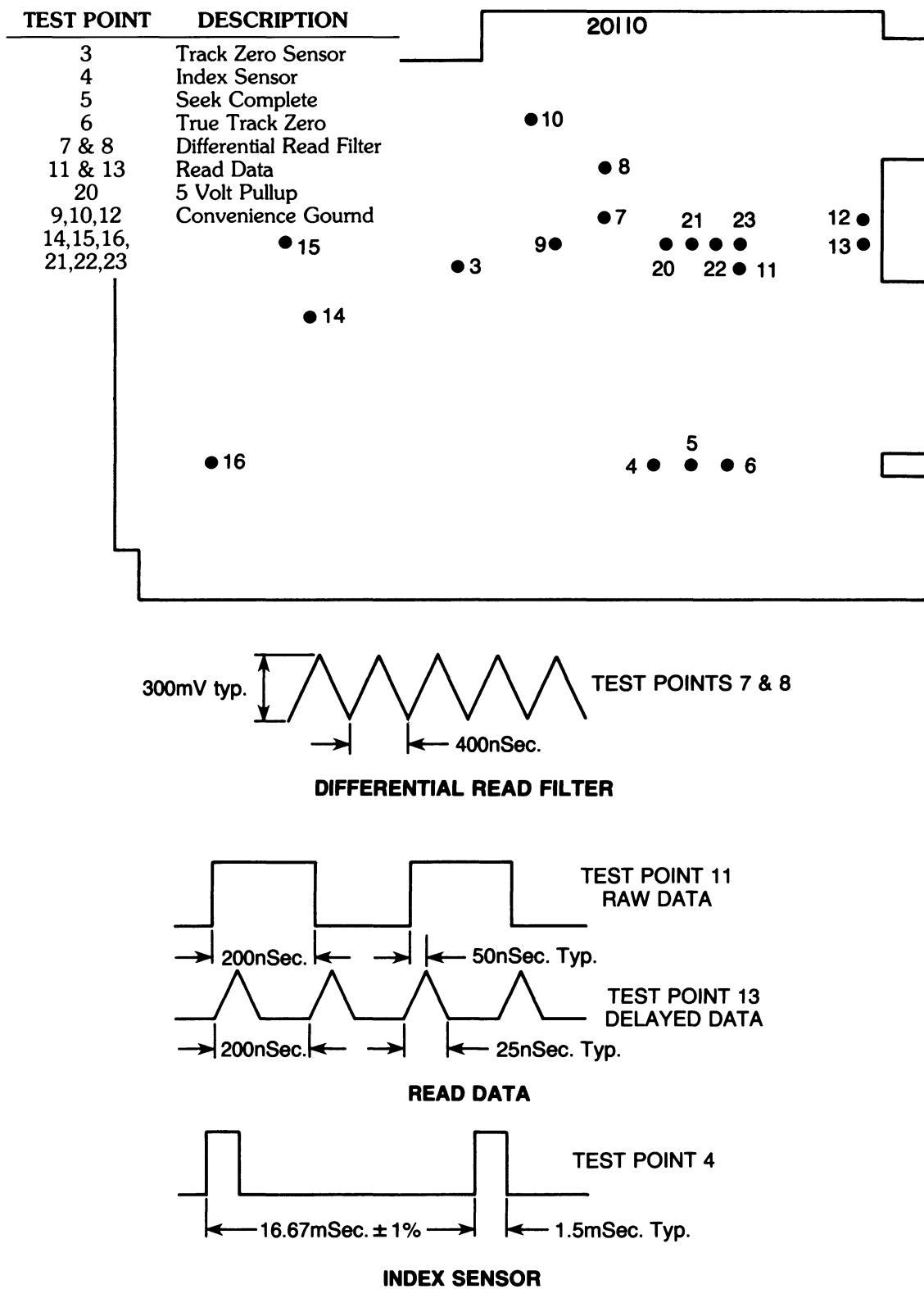


Figure 2-8. Drive Electronics PCA (P/N 09133-69101 or 09133-69103) Test Point Layout and Timing

Drive Electronics PCA - P/N 09133-69101 or 09133-69103

The following test point description along with Figure 2-9 is presented as a troubleshooting aid in isolating the Drive Electronics assembly. The assembly is used with the 412 drive. Check the part number of the drive electronics assembly to be sure you have the right assembly.

Test Points 1 & 2 (Differential Read Filter)

Test Points 1 and 2 can be used to observe the differential read data. The typical amplitude of the signal resulting from adding the two channels is 300 millivolts. Test Point 8 should be used as ground to reduce noise.

Components of 1.25, 1.66, and 2.5 MHz should be observed. A full track record of high frequency data (0000 and 1111) should resemble the one shown in Figure 2-9.

Test Point 3 & 4 (Read Data)

Test Points 3 and 4 can be used to observe the Read Data from the operation of the Time Domain Filter. Trigger on Test Point 3 and monitor the delay at Test Point 4. Typically, the delay observed should be 50 nanoseconds. A full track record of high frequency data (0000 or 1111) should resemble the one shown in Figure 2-9.

Test Point 5 (Track Zero Sensor)

Test Point 5 can be used to monitor the Track Zero sensor. A high logic level is a valid Track Zero indication.

Test Point 6 (Index Sensor)

Test Point 6 can be used to monitor the Index sensor. A high logic level is a valid indication. Only the leading edge of the pulse can be considered valid. The typical signal at Test Point 6 should resemble the one shown in Figure 2-9.

Test Point 6 can be used to adjust the spindle motor speed. Monitor Test Point 6 and adjust R3 on the Motor Control PCA (accessible through the side frame) for a period of 16.67 milliseconds, $\pm 1\%$.

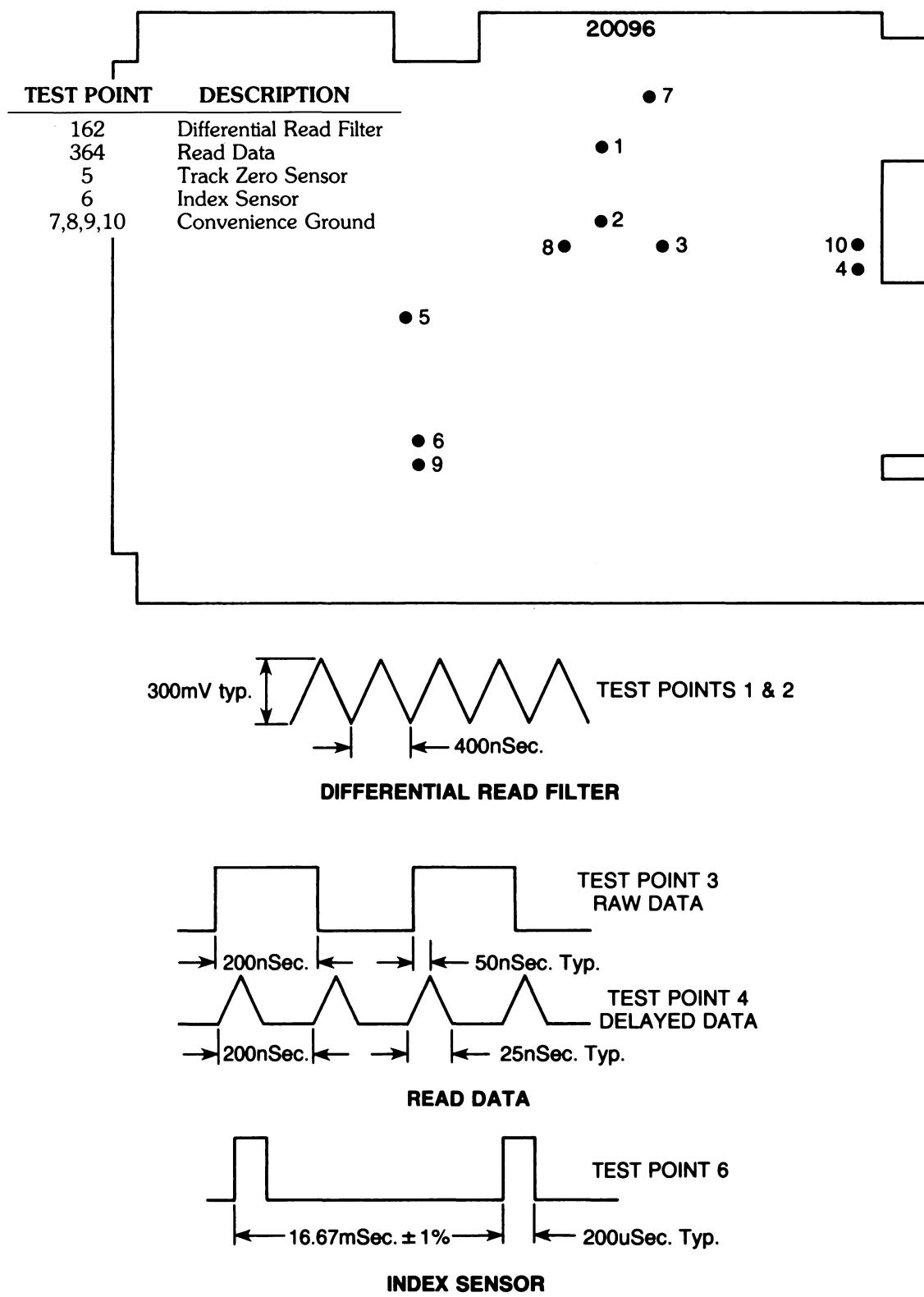


Figure 2-9. Drive Electronics PCA (P/N 09133-69101 or 09133-69103) Test Point Layout and Timing

Section II HP 9133A/B, 9134A/B & 9135A Disc Memory Products

Chapter 1

Theory Of Operation

- General Description
- Controller Theory of Operation
- Power Supply Theory of Operation
- Controller Selftests
- Controller Jumper Configuration

General Description

This manual describes the HP Winchester Disc Drives. The A version of the product is a 5-Mbyte drive (9133A, 9134A, and the 9135A). These A versions can be configured for two types of operation. These are shown next:

- Standard - 4.6-Mbyte, 4-Volume
 Option 10 - 4.8-Mbyte, Single-Volume

The B version of the same product is a 10-Mbyte drive (9133B or the 9134B). The B version of the 9135 Disc Drive was not produced.

The 5 1/4-inch Winchester disc drive contained in the 913XA products (See the following list) provides either 4.6 or 4.8 Mbytes of storage capacity. The standard (4-Volume) configuration causes the drive to appear as an HP 9895A Flexible Disc Drive master with three slave drives (1.15 Mbytes per volume) and the option 10 (Single-Volume) configuration causes the drive to appear as one large 4.8 Mbyte volume.

913XA/B Family

	A (5 Mbyte)	B (10 Mbyte)	3 1/2-inch Flexible Disc	5 1/4-inch Flexible Disc
HP 9133	X		X	
HP 9134	X		X	
HP 9135	X			X

The A versions of the 913X products are available in either the 4-Volume or Single-Volume configuration. The B versions are only available in the Single-Volume form. The user's mainframe must have an operating system designed to support the selected volume configuration.

The original controller PCA installed in the 913XA products was designed and manufactured by Microcomputer Systems Corporation. It is not serviced by HP except for assembly replacement. Information on this MSC controller is at the back of the Appendix.

The latest controller PCA is designed and manufactured by HP and is installed in all current 913XA and B products. The 4-Volume or Single-Volume operation is configured using jumpers on the PCA as well as the selection of 5 or 10-Mbyte Winchester disc configuration.

The power supply PCA is designed to power all 913X products. It powers the Winchester drive, the Winchester controller PCA, a flexible disc drive, the flexible disc drive controller PCA and an I/O assembly. The I/O assembly is contained on the same PCA as the power supply.

Product Configuration

The following tables list the firmware by part number for the different product configurations as well as the jumper positions for the 10-Mbyte drive.

Table 1-1. Product Configuration

Product	Drive	Drive Electronics	Controller	Processor-IC	ROM-IC
HP 9133					
A	09135-69600	09135-69502	09135-69515	09135-85500	09135-85501
A#10	9135-69600	09135-69502	09135-69501	88134-85500	88134-85501
After SN 2239A01446 model A and A Option10 change to the following:					
	09133-69100	09133-69103	09133-69514	N/A	N/A
B	09133-69102	09133-69101	09133-69514	N/A	N/A
HP 9134					
A	09135-69600	09135-69502	09135-69515	09135-85500	09135-85501
A#10	09135-69600	09135-69502	09135-69501	88134-85500	88134-85501
After SN 2203A03086 model A and A Option 10 change to the following:					
	09133-69100	09133-69103	09133-69514	N/A	N/A
B	09133-69102	09133-69101	09133-69514	N/A	N/A
HP 9135					
A	09135-69600	09135-69502	09135-69515	09135-85500	09135-85501
A#10	09135-69600	09135-69502	09135-69501	88134-85500	88134-85501
After SN 2151A04165 model A and A Option 10 change to the following:					
	09133-69100	09133-69103	09133-69514	N/A	N/A
HP 250					
20	09135-69600	09135-69502	88134-69910	88134-85500	88134-85501
After SN xxxxxxxxxxx model 20 changes to the following:					
	09133-69100	09133-69103	09133-69514	N/A	N/A
25	09133-69102	09133-69101	09133-69514	N/A	N/A
HP 9000					
20	09855-69963	N/A	09855-69886	N/A	N/A

Jumper Configuration for the 09133-69514 controller assembly appears in the next table:

Table 1-2. 10-Mbyte Jumper Configuration

Product	10M	Jumpers One Volume	4XX
9133A	Removed	Removed	Installed
Option 10 9133A	Removed	Installed	Installed
9133B	Installed	Installed	Installed
9134A	Removed	Removed	Installed
Option 10 9134A	Removed	Installed	Installed
9134B	Installed	Installed	Installed
9135A	Removed	Removed	Installed
Option 10 9135A	Removed	Installed	Installed

Removing the 10M jumper indicates a 5-Mbyte drive and removing the One-Volume jumper indicates the 4-Volume configuration. The 4XX drive refers to the ST406 and ST412 drives. The 4XX jumper removed indicates the ST506 Dual-Platter drive. The ST506 Dual-Platter drive uses the MSC controller (88134-69910, 09135-69515, and 09135-69501). See the next section.

The platter configurations (dual and single) of the drives that are used in the 913X products appear next:

- ST506 - Dual Platter 5-Mbyte (early units)
- ST406 - Single Platter 5-Mbyte (improved track density)
- ST412 - Dual Platter 10-Mbyte (improved track density)

Winchester Controller PCA Theory of Operation (88134-69910, 09135-69515, and 09135-69501)

There are two sets of firmware available. They are the "D" code and "L" code PROM's with the appropriate processor chip which contains onboard ROM. The "D" code firmware emulates 9895A drives (four volumes) and the "L" code firmware (used on the HP 250) causes the Winchester to appear as one 4.8-Mbyte volume. In the case of the "L" code firmware, the read/write heads access 153 (0-152) tracks of each disc surface. The following controller PCA have been used on the 5-Mbyte drives.

- P/N 88134-69910 "L" Code - HP 250 Model 20
- P/N 09135-69515 "D" Code - 4-Volume 5-Mbyte
- P/N 09135-69501 "L" Code - Single-Volume 5-Mbyte

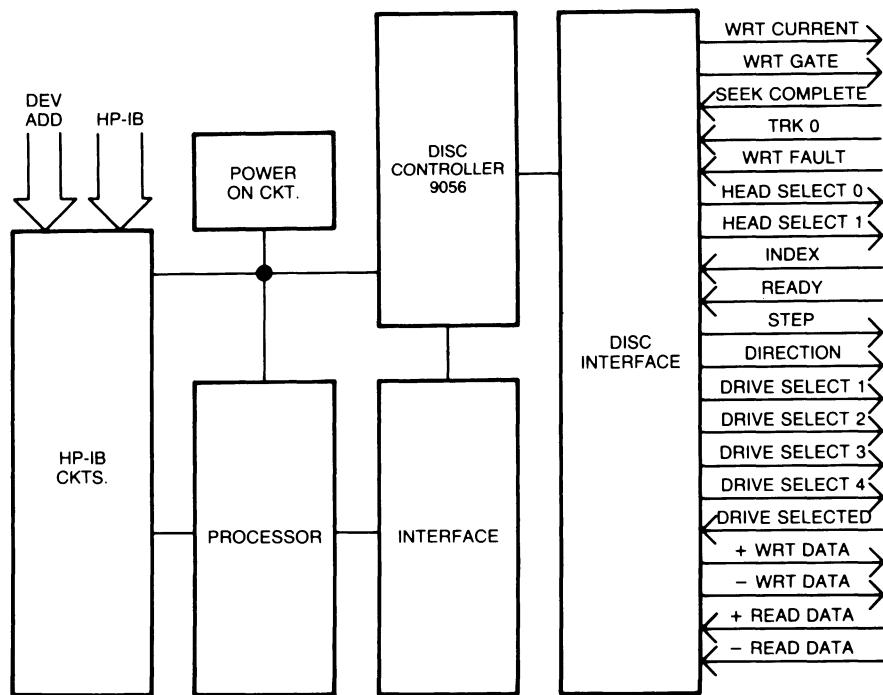


Figure 1-1. Winchester Controller Block Diagram

The power-on circuit resets the processor, HP-IB circuit and the 9056 module (the large black module attached to the Winchester controller PCA). All data transfers between the HP-IB and the internal data bus are controlled by the processor. The HP-IB bus controller (9914 HP-IB chip) manages the data transfers across the HP-IB channel.

The 9056 module provides data buffering and management, status checking and control of the drive assembly, head selection, head positioning and verification, write fault monitoring, error detection (up to 22-bit bursts), error correction (up to 11-bit bursts), WRITE GATE enable, and WRITE CURRENT level switching.

Controller Theory of Operation (09133-69514)

The controller PCA is designed to interface the 5-Mbyte single-platter and the 10-Mbyte dual-platter versions of the Winchester drives to the mainframe. Jumpers are used to tailor the controller to the Winchester drive. These jumpers select the Winchester drive capacity and configure for either single-volume or four-volume operation (5-Mbyte drives only). The following controller PCA have been used on the 5 and 10-Mbyte drives.

P/N 09133-69514 5/10-Mbyte - Jumper Selectable

Refer to the block diagram of Figure 1-2 while reading the following.

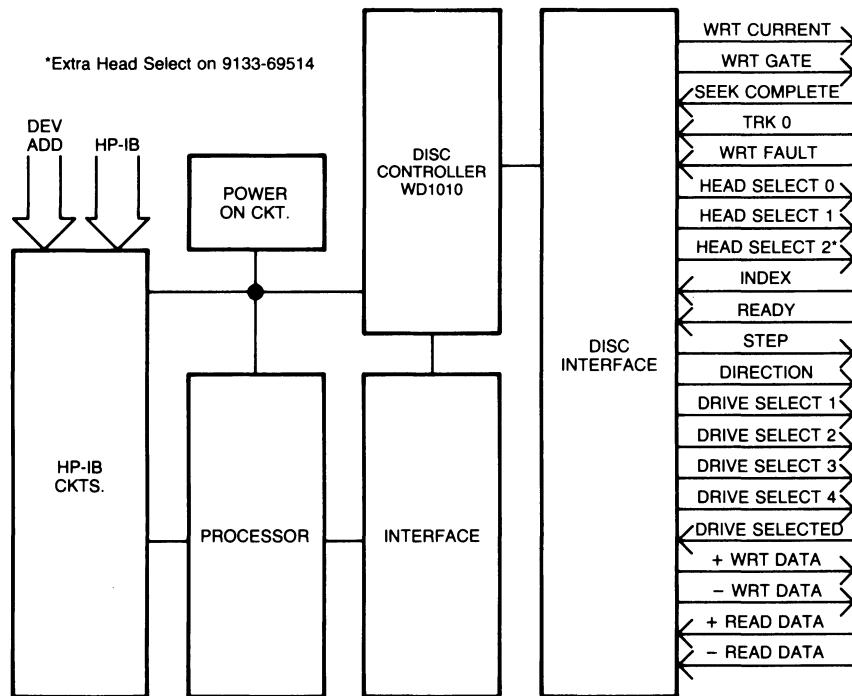


Figure 1-2. Controller Block Diagram

Microprocessor Circuit

The microprocessor is a 68B09 8-bit processor with a 2-MHz bus rate. Timing is provided by an internal oscillator which drives an 8-MHz crystal. The output of the oscillator is divided by four to provide 2-MHz signals (E and Q). The signals are phase shifted 90 degrees with respect to each other, so that Q leads E. The address present on the address bus is valid whenever either E or Q is high.

Program memory for the microprocessor is stored in an 8-Kbyte ROM. The ROM is selected whenever address line A15 is high and the VMA (valid memory address = E + Q) is high.

Scratch-pad memory for the processor consists of 128 bytes of RAM. The RAM is selected by three of the chip select lines provided on the chip. The condition necessary to select the RAM is A15 low and A07 high and E high.

Disc Controller, HP-IB Chip, Input and Output Ports

The disc controller, HP-IB chip (8291A) and input and output ports are selected by strobe lines from a 3-line to 8-line decoder. The decoder is selected when VMA = Q + E and the ROM is not selected (A15 low). When the decoder is selected, one of the 8 output lines is pulled low depending on the sense of address lines A05, A06, and A07. The four outputs that correspond to A07 being 1 are not used since the RAM is addressed when this occurs.

The input port is 8 bits wide. The bit assignments are as follows:

BIT 7--Not Used

BIT 6--LED_ON_L (CURRENT STATE OF SELFTEST LED)

BIT 5--5_H/10_L (5 OR 10 MBYTE DRIVE)
BIT 4--D_H/L_L (SINGLE VOLUME OR 9895 A LOOK-ALIKE)
BIT 3--5XX_L/4XX_H
BIT 2--ADDR2_L (MSB OF HP-IB ADDRESS)
BIT 1--ADDR1_L
BIT 0--ADDR0_L (LSB OF HP = IB ADDRESS)

The output port is 8 bits wide. The bit assignments are as follows:

BIT 7--BUFFER_READY_H
BIT 6--LED_ON_L
BIT 5--NOT CONNECTED
BIT 4--NO ASSIGNMENT
BIT 3--PRE_COMP_DISABLE_H
BIT 2--BUFFER_COUNTER_CLEAR_L
BIT 1--NOT CONNECTED
BIT 0--WD_RESET_L

The disc controller chip provides most of the control signals needed by the drive. It communicates with the microprocessor through 7 input and output registers and an external RAM buffer. The disc controller chip keeps track of which cylinder the head is positioned over, and when it is necessary to move the head. It controls the direction line and issues the appropriate number of step pulses. It also does the parallel-to-serial conversion, MFM encoding, and generates the precomp control signals necessary for a write operation. On a read operation, the disc controller chip does the MFM decoding, and the serial-to-parallel conversion. The disc controller chip also provides verification of sector headers, control of the phase-lock loop, checking of the error detecting CRC bytes, and automatic initiation of up to 8 retries if an error is detected.

The data separator reconstructs the clock from the incoming MFM-encoded bit stream and generates a 5-MHz clock with phase relationship to the incoming data such that nominal data transitions are centered on one level of the read clock and nominal clock transitions are centered on the other level. The read clock is generated by dividing down a 10-MHz clock that is phase locked to a delayed copy of the incoming data. The phase-lock loop uses a digital phase detector whose output is pump-up or pump-down pulses with a pulse width proportional to the phase error. The phase-up line is provided to allow the VCO (Voltage Controlled Oscillator) to be started up in phase with the incoming data signal to minimize lock-up time.

Power Supply Theory of Operation

Refer to the power supply schematic diagram (Chapter 4, Section II) while reading the following text. The regulated DC voltages provided by the power supply are +5 VDC, +12 VDC, and -5 VDC. Regulation for the +5 VDC and +12 VDC is accomplished by two differential amplifiers U2B and U2D.

The secondary voltages are rectified by three full-wave bridge networks and applied to the collectors of three series pass transistors Q1, Q6, and Q7.

Voltage Reference Circuit

The voltage at the emitter of Q1 is applied to the inverting input of U2A, so that if the emitter voltage of Q1 ("1") decreases, the output of U2A goes positive. This increases conduction of Q1 and thereby increases the emitter voltage.

Regulators +5 VDC and +12 VDC

Action of the +5 VDC regulator and +12 VDC regulator is the same as that of U2A/Q1. Darlington transistor configurations are used at the outputs of the +5 VDC and +12 VDC regulators to increase their current handling capabilities.

The zener diodes at the outputs of the +5 VDC, +12 VDC and -5 VDC regulators provide protection, should the voltage levels at those points exceed the voltage ratings of the zener diodes. If this should happen, the zeners will short out and open the fuse. Check the zeners with an ohmmeter to find which has shorted and replace the faulty zener and the fuse before re-applying power. The fuse won't blow if the zener on the -5 VDC line shorts because the -5 VDC regulator is current limited.

VREF Circuit

The reference voltage (VREF) applied to pins 3, 5 and 12 of U2 is held at +5.1 VDC by zener diode CR1 and filtered by capacitor C2.

Crowbar Circuit

The purpose of this circuit is to blow the primary fuse if the device is connected to 220 VAC or 240 VAC and the voltage select switches are set to 110 or 120 VAC position.

The Crowbar circuit consists of a 30V zener diode CR6, SCR CR5 and associated circuitry. When the voltage at the cathode of CR6 exceeds 30 VDC, the diode conducts to increase the voltage on the gate of SCR CR5. In turn CR5 conducts very heavily and shorts the output of the bridge to ground. This will in turn blow the fuse, F1, in the primary circuit (only if the proper fuse is installed).

WARNING

IT IS IMPORTANT THAT THE PRIMARY FUSE F1 IS THE CORRECT RATING. CHECK THE PRIMARY FUSE FOR THE CORRECT RATING WHEN SERVICING THE UNIT.

Controller Selftests (88134-69910, 09135-69515, and 09135-69501)

The Winchester controller PCA is equipped with a selftest switch and status LED. The selftest switch is located on the component side of the board near its rear edge (see Figure 1-3).

The tests performed during the selftest of the Winchester are as follows:

1. Power On Selftest - Verifies track 0/sector 0
2. Format Status - Tests hardware operation

3. Read/Write - Writes to, then Reads from the maintenance track.

While the Winchester selftest is being executed, the status LED located on the component side of the PCA flashes. If the selftest passes without error, the status LED is brightly lit. If an error condition is detected, the LED is dimly lit or off. See the MSC selftest command at the back of the Appendix.

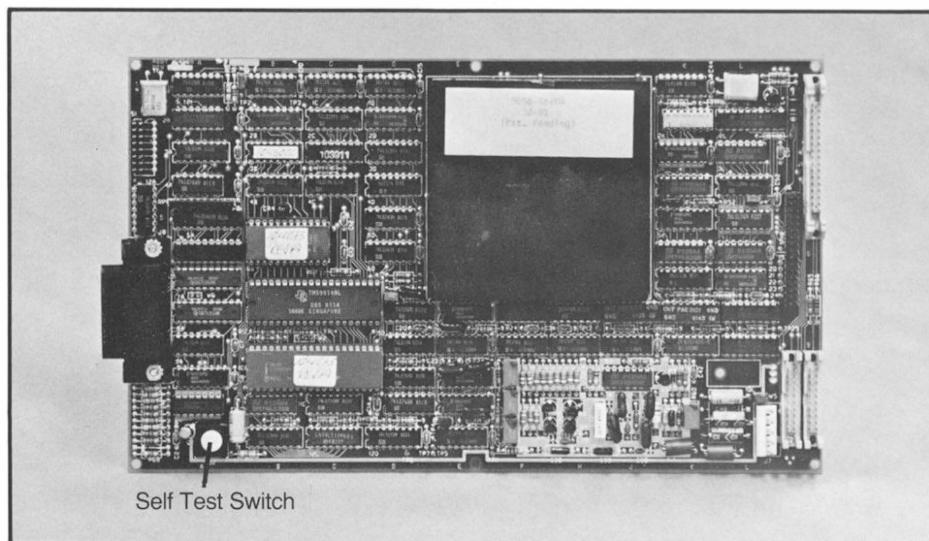


Figure 1-3. Selftest Switch

Controller Selftests (09133-69514)

There are two selftest procedures provided on this controller PCA. They are the Power-on Self-test, and Initiate Selftest command issued from the mainframe. The power-on selftest is not identical to the selftest done in response to the Initiate Selftest command. Some continual self-testing is also done during normal command execution. See the Initiate Selftest command description in the Appendix for details on all of these modes of selftest.

Selftest Results

The selftest results are two bytes that describe the most recently detected hardware error. These bytes are cleared when the Read Selftest command is executed.

The format of the two bytes is:

E 0 U U 0 H H H
C C C C C C C C

where: E is a bit indicating that an error was detected

UU gives the current unit when the error was detected

HHH gives the head selected when the error was detected

CCCCCCCC is an error code describing the failure

If the E bit is zero (no error), then both bytes are zero.

Controller (P/N 09133-69514) Jumper Configurations

The Winchester controller PCA (P/N 09133-69514) can be configured to interface the following three versions of the Winchester drive.

- Single-Platter 5-Mbyte drive
- Dual-Platter 10-Mbyte drive

The single-platter 5-Mbyte can be configured to appear as either a single 4.8-Mbyte volume or as a four-volume (1.15 Mbyte per volume - 9895A master with three slave drives). The dual-platter 10-Mbyte drive can be configured only as one large 10-Mbyte volume. Jumpers are plugged onto pins of J6 and the configurations are as follows. Also see Figure 1-4. "The 09133-69514 Controller PCA".

J6 Pins	Configuration	Legend
00		
00	Not Assigned	
00		XX -- 10 Mbyte
00		XX -- One Volume
00	Single-Platter 5-Mbyte 4-Volume	XX -- 4XX Drives
XX		
00		
XX	Not Assigned	
00		
00		
XX		
XX	Single-Platter 5-Mbyte Single-Volume	
XX		
XX		
00	Not Assigned	
00		
XX		
00	Not Assigned	
XX		
XX		
XX	Not Assigned	
00		
XX		
XX		
XX	Dual-Platter 10-Mbyte Single-Volume	
XX		

XX = jumper installed
00 = jumper not installed

Controller PCA Test Point Location and Waveform Description

Test point location and waveform description found at these test points are presented to assist you in isolating troubles which may be either in the Winchester drive or controller PCA.

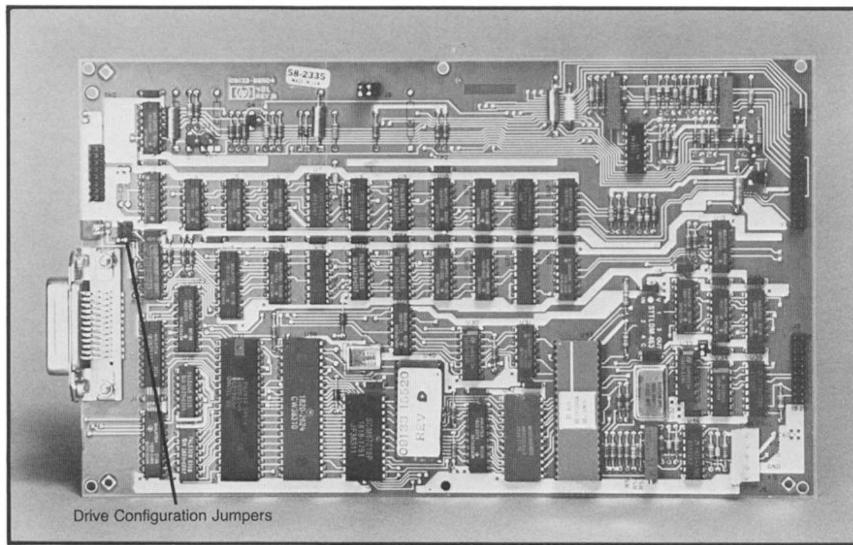


Figure 1-4. The 09133-69514 Controller PCA

Test Point	Signal Name	Waveform Description
TP GND	GROUND	
TP2	DELAYED DATA	TTL wave (4VPP) at approximately 10 MHz with leading edge in phase with leading edge of reconstructed clock signal.
TP4	RECONSTRUCTED CLOCK	Square wave TTL signal in phase with delayed data.
TP5	ERROR VOLTAGE	
TP6	RAW DATA	Positive TTL signal approximately 0.4 milliseconds in duration.
TP7	PRECOMPENSATED WRITE DATA	Negative TTL signal approximately 0.4 milliseconds in duration.
P9	SEEK COMPLETE	+ 4 VDC level after seek complete.
TP10	TRACK 00	+ 4 VDC level after reaching track 00
TP11	WRITE FAULT	Normally low.
TP12	INDEX	Positive going TTL square wave approximately 2.2 milliseconds in duration.
TP13	READY	Normally + 4 VDC
TP14	STEP	
TP15	WRITE GATE	Normally + 4 VDC. Low for approximately 400 microseconds when writing data.
TP16	VMA	2 MHz clock.

Chapter 2

Assembly Access

- Introduction
- Safety Considerations
- Assembly Access

Introduction

This chapter provides information for disassembly and reassembly of the Winchester disc drive within the HP 913X disc memories. An exploded view is also provided with the instructions. Disassembly procedures are given only for the exchange items. The exploded view which appears in this chapter also appears in Chapter 3, the replaceable parts section, with the parts list appearing in disassembly order and all replaceable parts keyed with item numbers. Be sure to retain any unmentioned hardware when disassembling the disc memories for reassembly.

The disassembly procedure for the 5 1/4 flexible disc drive is presented after the Winchester drive section. This is for the 9135A only. All information on the 3 1/2-inch flexible disc drive included in the 9133A/B products is found in the 3 1/2-inch service manual (P/N 09121-90030).

WARNING

REMOVE POWER TO THE DISC MEMORY BEFORE REMOVING
ANY ASSEMBLY.

NOTE

Unless otherwise indicated in the procedures, the disc memory assemblies are installed by reversing the procedures given for their removal.

The following tools are required for disassembly and reassembly of the disc memories.

- #1 Posidrive Screwdriver
- #2 Posidrive Screwdriver
- 5/64" Allen Wrench or the proper Torx driver – Torx set P/N 8710-1426
- Needlenose Pliers
- Small Flat Blade Screwdriver

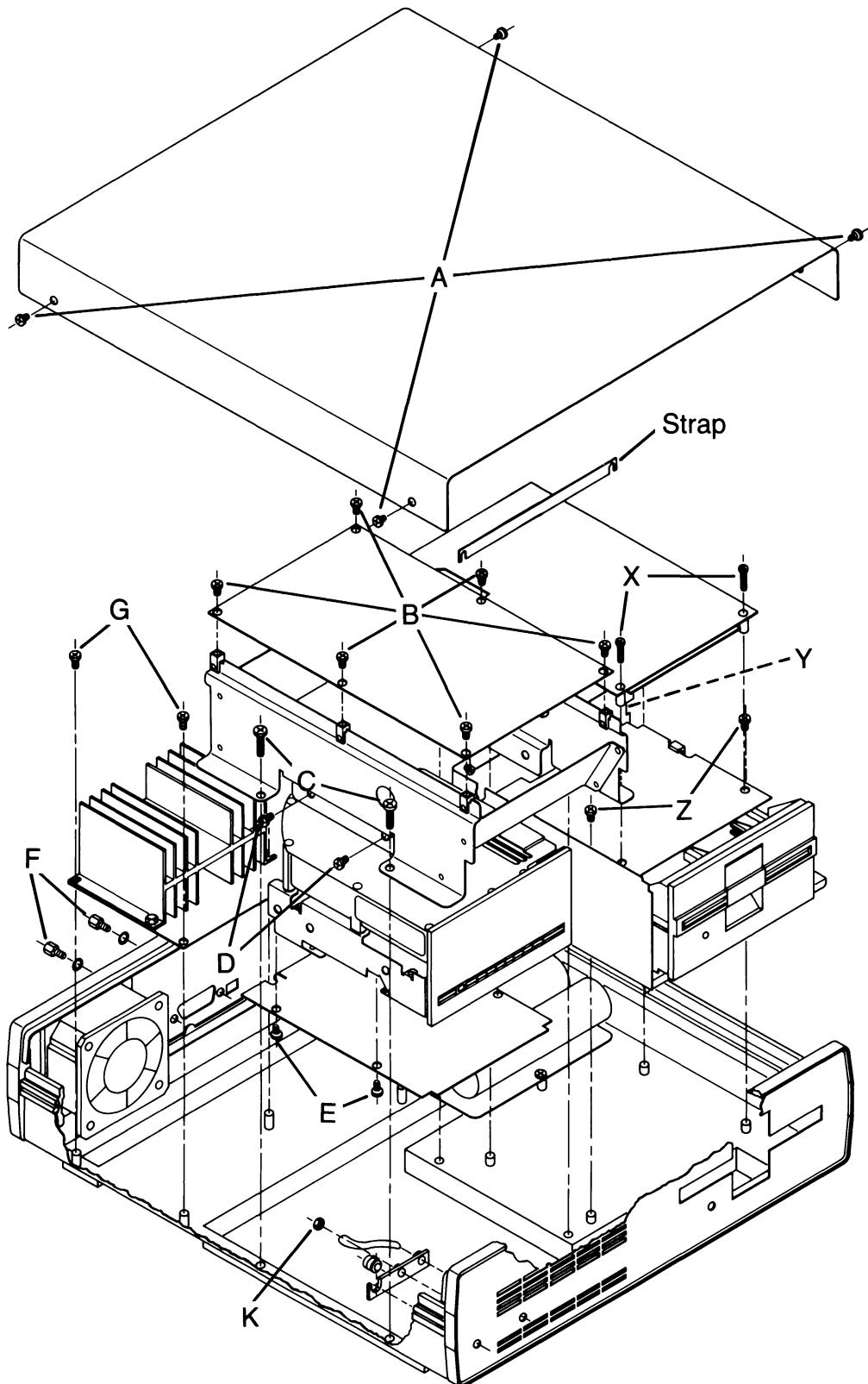


Figure 2-1. HP 913X Disc Memory Exploded View

Safety Considerations

General

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

Safety Symbols



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.



Indicates hazardous voltages.



Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which if not correctly performed, could result in damage to, or destruction of, part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

Safety Earth Ground

This is a safety class I product and is provided with a protective earthing terminal. An uninterrupted safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

Before Applying Power

Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual, and that the correct primary fuse rating is installed.

If this product is to be energized via an auto-transformer (for voltage reduction), make sure the common terminal is connected to the earth terminal of the main power source.

Servicing

Any servicing, adjustment, maintenance or repair of this product must be performed only by service-trained personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when the product is disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow) are to be used for replacement.

Top Cover Removal

To access the internal assemblies, the top cover must first be removed. Remove the four screws (Labeled A in Figure 2-1) and lift the top cover. Next remove the hex nut securing the ground strap to the cover and lift the cover off.

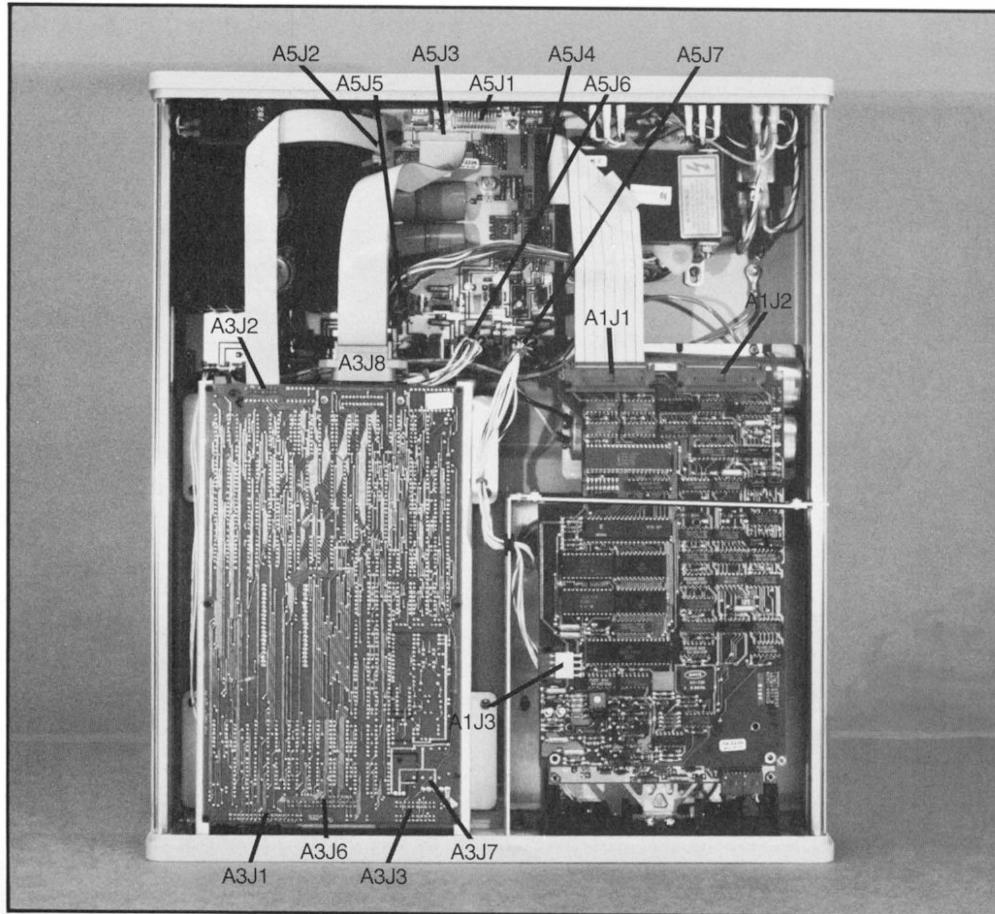


Figure 2-2. Connector Locations

CAUTION

CAUTION MUST BE USED WHEN REINSTALLING CONNECTORS ON THE POWER SUPPLY PCA. IT IS POSSIBLE TO INSERT THE CONNECTORS IN THE WRONG POSITIONS. REFER TO FIGURE 2-2 FOR THE CORRECT POSITIONS FOR THE CONNECTORS.

Winchester Disc Drive Controller PCA Removal

The Winchester controller PCA does not have to be removed to gain access to the Winchester drive or its electronics PCA.

The controller PCA is removed by completing the following steps. First remove the power connector A5J6 from the power supply PCA. Next remove the six screws (Labeled B in Figure 2-1) and lift the PCA upward. Rotate the controller PCA onto its side. Remove the power connector (A3P6) and the ribbon cable connectors (A3P1 and A3P8).

CAUTION

IT IS POSSIBLE TO INSERT THE POWER CONNECTOR (A3P6) AND RIBBON CABLE CONNECTOR (A3P8) ON THE WINCHESTER CONTROLLER PCA IMPROPERLY. BE CAREFUL WHEN REPLACING THESE CONNECTORS. REFER TO FIGURE 2-3 FOR CORRECT INSTALLATION OF THE CONNECTORS.

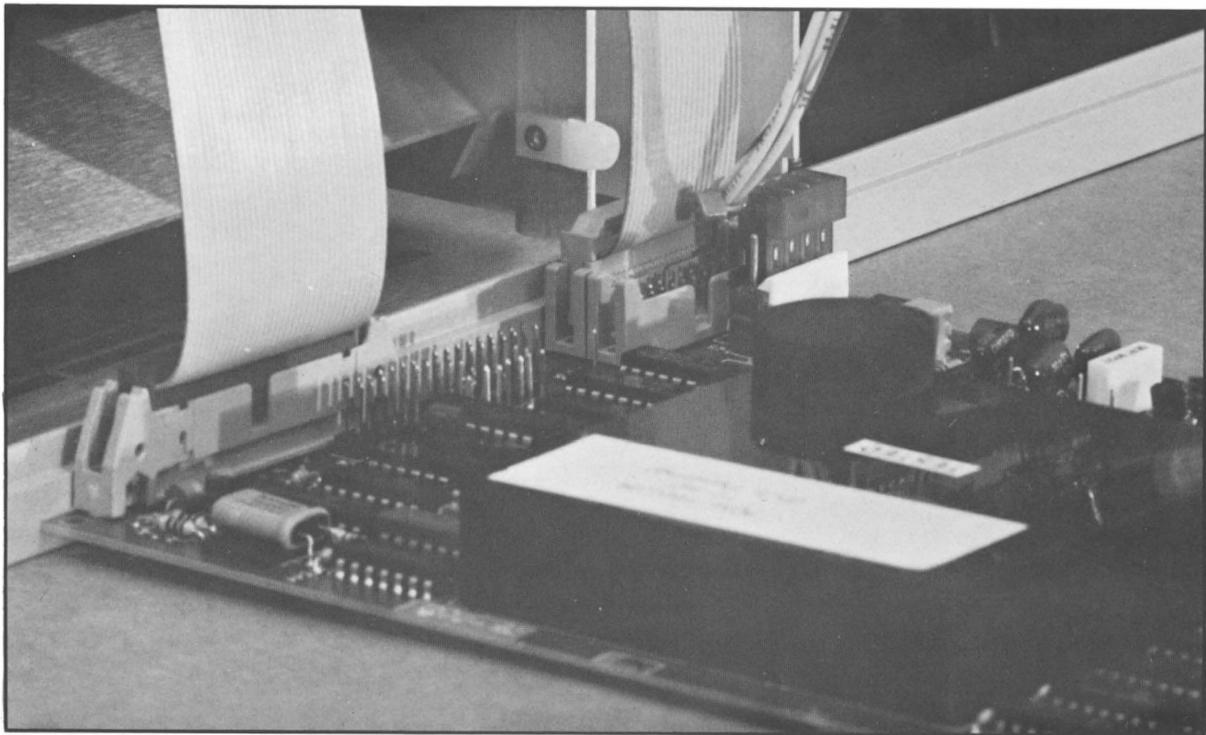


Figure 2-3. Winchester Controller PCA Connectors.

Drive Assembly Removal

The Winchester disc drive support bracket must first be removed to gain access to the drive. To do this, remove the power connector (A5P6) on the power supply board. Remove the four screws (Labeled C in Figure 2-1) holding the support bracket to the chassis.

To remove the Winchester disc drive assembly from the support bracket, remove the four screws (D, two from each side) and carefully slide it out of the bracket.

Drive Electronics PCA Removal

To remove the drive electronics PCA from the Winchester disc drive assembly, remove the ribbon cable connectors (A3P1 and A3P2). Turn the unit over and carefully remove the connectors A4P4, P5, P6, P7, and P8. Using a 5/64" Allen Wrench or the proper Torx, remove the four screws (Labeled E in Figure 2-1) and slide the PCA out.

Power Supply PCA Removal

To remove the power supply PCA, remove connectors A5P1, A5P2, A5P3, A5P4, and A5P5. Remove the two HP-IB plate screws (Labeled F in Figure 2-1) and the four screws (Labeled G in Figure 2-1) and lift the power supply board out of the chassis.

NOTE

The HP-IB connector screws are easily broken during removal and reinstallation of the power supply PCA. Use caution when removing and reinstalling them.

Front Panel Removal

To remove the front panel, first remove the power indicator LED by prying the LED retainer ring from around the LED holder. Remove the light pipe holder by removing nut (K). Next remove the six nuts which hold the front panel in place. Carefully slide the front panel outward.

Rear Panel Removal

The rear panel can be removed with or without the components attached to it. The voltage select switches are held in place by two screws and two nuts each. The power switch is pressed in from the outside, so that the wires attached to it must be removed prior to pressing it out. The fan is held in place by two nuts. The line filter is held in place by two nuts. The rear panel can be removed by removing the six nuts around the inside of the rear panel.

Bottom Panel Removal

The power transformer can be removed at this time. The power transformer is held in place by four screws. The bottom panel can now be removed by removing its four screws.

Front and Rear Panel Bezel Removal

The front and rear panel bezels are held to the side rails by four screws each.

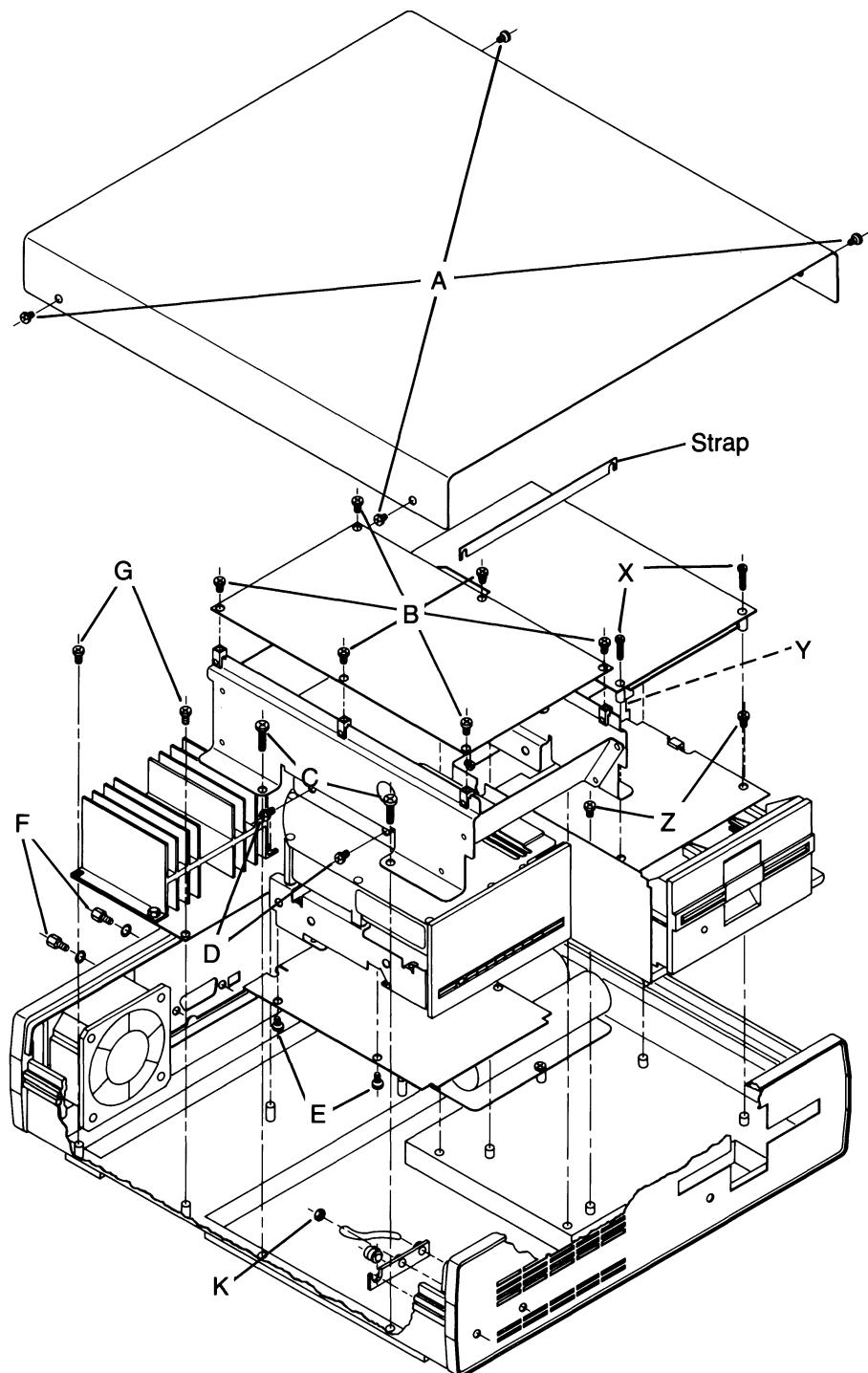


Figure 2-4. 5 1/4-inch Flexible Disc Drive Exploded View

5 1/4 Flexible Disc Drive Disassembly

This section provides information for disassembly and reassembly of the 5 1/4-inch Flexible Disc Drive. An exploded view is also provided with the instructions. Disassembly procedures are given only for the exchange items. Be sure to retain any unmentioned hardware when disassembling the disc drive for reassembly.

To access the internal assemblies, the top cover must first be removed. See the previous section titled "Top Cover Removal" for that information.

CAUTION

CAUTION MUST BE USED WHEN RE-INSTALLING CONNECTORS ON THE POWER SUPPLY PCA. IT IS POSSIBLE TO INSERT THE CONNECTORS IN THE WRONG POSITIONS. REFER TO FIGURE 2-5 FOR THE CORRECT POSITIONS FOR THE CONNECTORS.

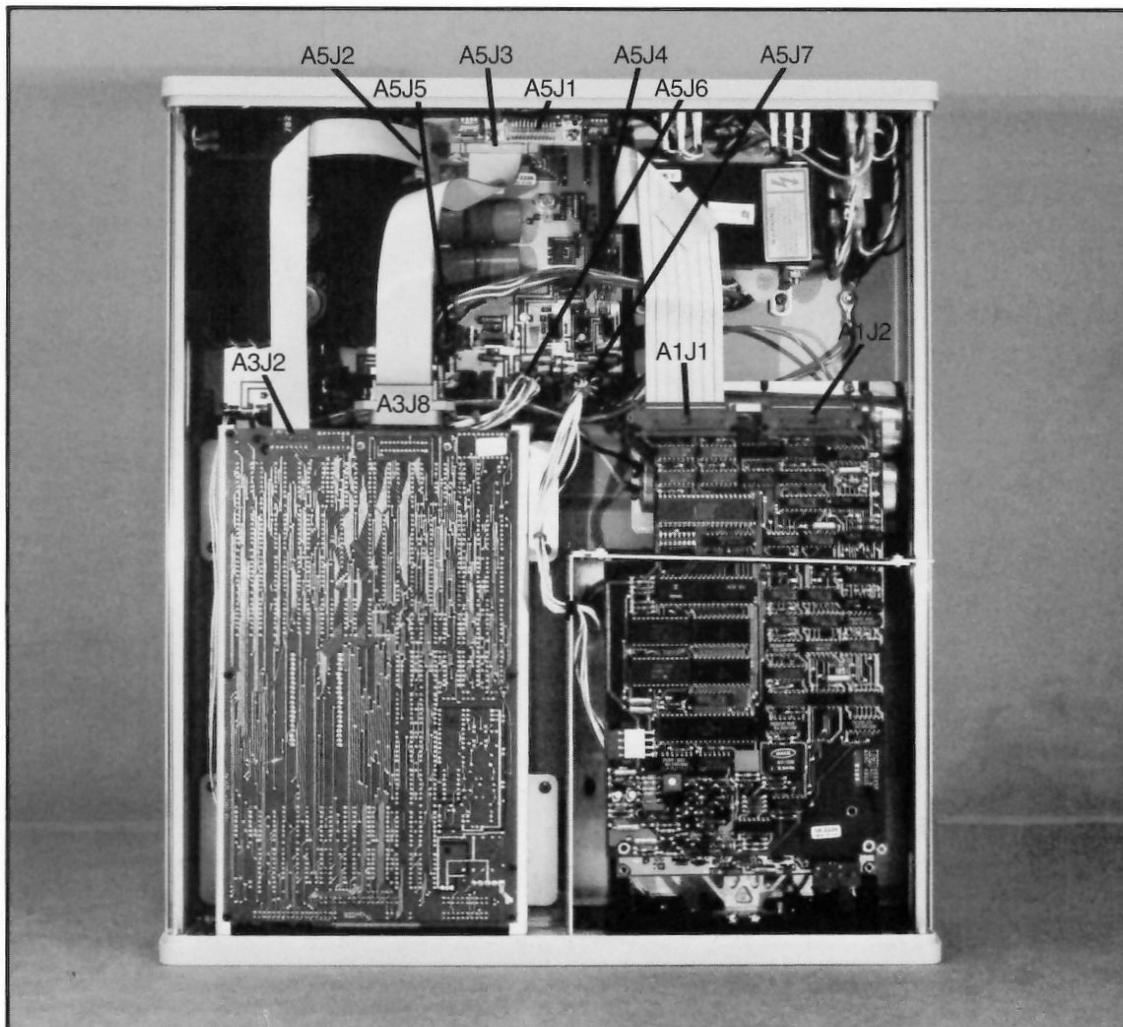


Figure 2-5. Power Supply Connector Locations

Flexible Disc Drive Controller PCA Removal

If you wish to access the drive assembly or the drive electronics PCA, removal of the controller PCA is not required.

Remove the two ribbon cable connectors from the rear of the controller PCA (A1P1 and A1P2) and the power connector (A5P7) from the right side of the power supply PCA. Remove the power connector (A1P7) from the left side of the controller PCA. Next loosen the two screws (Y) and lift off the aluminum strap containing the rubber channel. Remove the two screws (X) and lift the PCA from the top of the drive assembly and place the assembly on a clean, dry surface.

Flexible Disc Drive Assembly Removal

Lift the cable grommet from the slot in the aluminum bracket to the left of the drive. Remove the four screws (Z) and carefully lift the drive and its support bracket partially from the chassis assembly. Remove the power connector (A2P2) and the ribbon cable connector (A2P1) from the rear side of the drive electronics assembly. Four screws hold the drive assembly to the support bracket.

Chapter 3

Replaceable parts

- Introduction
- Replaceable Parts List
- 5 1/4-inch Flexible Disc Parts

Introduction

This chapter contains the replaceable parts list for the Winchester drive, 5 1/4-inch flexible disc drive, power supply, and the case assembly. The parts list for the mechanical assembly is shown in disassembly order with all parts keyed.

Reference designators are used in lieu of item numbers on printed circuit assemblies and the total quantity of each part is shown only once in the TQ column.

The check digit shown in the CD column is required when ordering a part from HP. Please include this number with your order.

The Winchester disc drive, its controller and servo PCAs are "exchange only" assemblies and are not broken down to any lower level.

The various 913X series products are listed with a "Usage Code" assigned to each product. The usage code shows how many, and on what product, the parts are used. The parts which do not have a usage code, are used on all 913X products.

Replaceable Parts List

ITEM NUMBER	REF DES	PART NUMBER	CD	TQ	DESCRIPTION	USAGE CODE
21	F1	2110-0083 OR 2110-0043	6	1	Fuse, 2.5A, 250V, Normal Blow	
			8	1	Fuse, 1.5A, 250V, Normal Blow	
22		2110-0565	9	1	Cap, Fuse	
23	XF1	2110-0610	5	1	Fuseholder	
24	FL1	9135-0136	9	1	Filter, Line	
Attaching Parts						
		2260-0009	3	2	Nut, Hex, 4-40	

25		0403-0106		4	Feet, Case	
26		7101-0674	7	1	Plate, Base	
Attaching Parts						
		2360-0195	0	4	Screw, # 6 X .312	

27		4040-2084	4	1	Light Pipe	
28		4040-2085	5	1	Bracket, Light Pipe	
Attaching Parts						
		0590-0305	9	1	Nut, Hex, 6-32	

29	CR2	09130-61604	9	1	Diode, LED Assy, Power	
30		7101-0671 OR 7101-0670 OR 09133-04401 OR 01934-04404 OR 09133-04403	4	1	Panel, Front, HP 9134A	C
			3	1	Panel, Front, HP 9135A	B
				1	Panel, Front, HP 9133A	A
				1	Panel, Front, HP 9134B	D
				1	Panel, Front, HP 9133B	E
Attaching Parts						
		0590-0305	9	6	Nut, Hex, 6-32	

31		7101-0673	6	1	Panel, Rear	
Attaching Parts						
		0590-0305	9	6	Nut, Hex, 6-32	

32		82901-20014	7	2	Bezel, Front/Rear	

ITEM NUMBER	REF DES	PART NUMBER	CD	TQ	DESCRIPTION	USAGE CODE
Attaching Parts						
		2510-0667	0	8	Screw, Mach, 8-32X.375	

33		7101-0667	8	2	Siderails	

5 1/4-inch Flexible Disc Parts

Replaceable Parts List

ITEM NUMBER	REF DES	PART NUMBER	CD	TQ	DESCRIPTION	DESCRIPTION
1	W1	09135-61600	0	1	Cable, Flexible Disc Controller	
2	W2	09135-61601	1	1	Cable, Power, Flexible Disc	
3		1600-0951	5	1	Bracket, Clamp	
Attaching Parts						
		2200-0521	8	2	Screw, Mach	

4	A1	82901-69002 OR 82901-69503	4	1	Controller PCA, Flexible Disc	
4			0	1	Controller PCA, Flexible Disc	
Attaching Parts						
		2200-0119	0	2	Screw, Mach, 4-40X1.0	

5	A2	09130-69600	1	1	Drive, Flexible Disc	
Attaching Parts						
		2360-0113	2	4	Screw, Locking, # 6X.25	

6	A2A1	09130-66501	5	1	Drive Elect PCA, Flexible Disc	
Attaching Parts						
		2200-0521	8	2	Screw, Mach, 4-40X.25	

7		1600-1252	1	1	Sub-panel, Flexible Disc Drive	
Attaching Parts						
		2360-0113	2	4	Screw, Locking, # 6X.25	

Chapter 4

Schematic Diagrams

- **Introduction**

Introduction

This chapter provides the schematic diagram for the power supply including the primary power wiring. Two power supplies are shown here; the 09135-69500, and the 09135-69510.

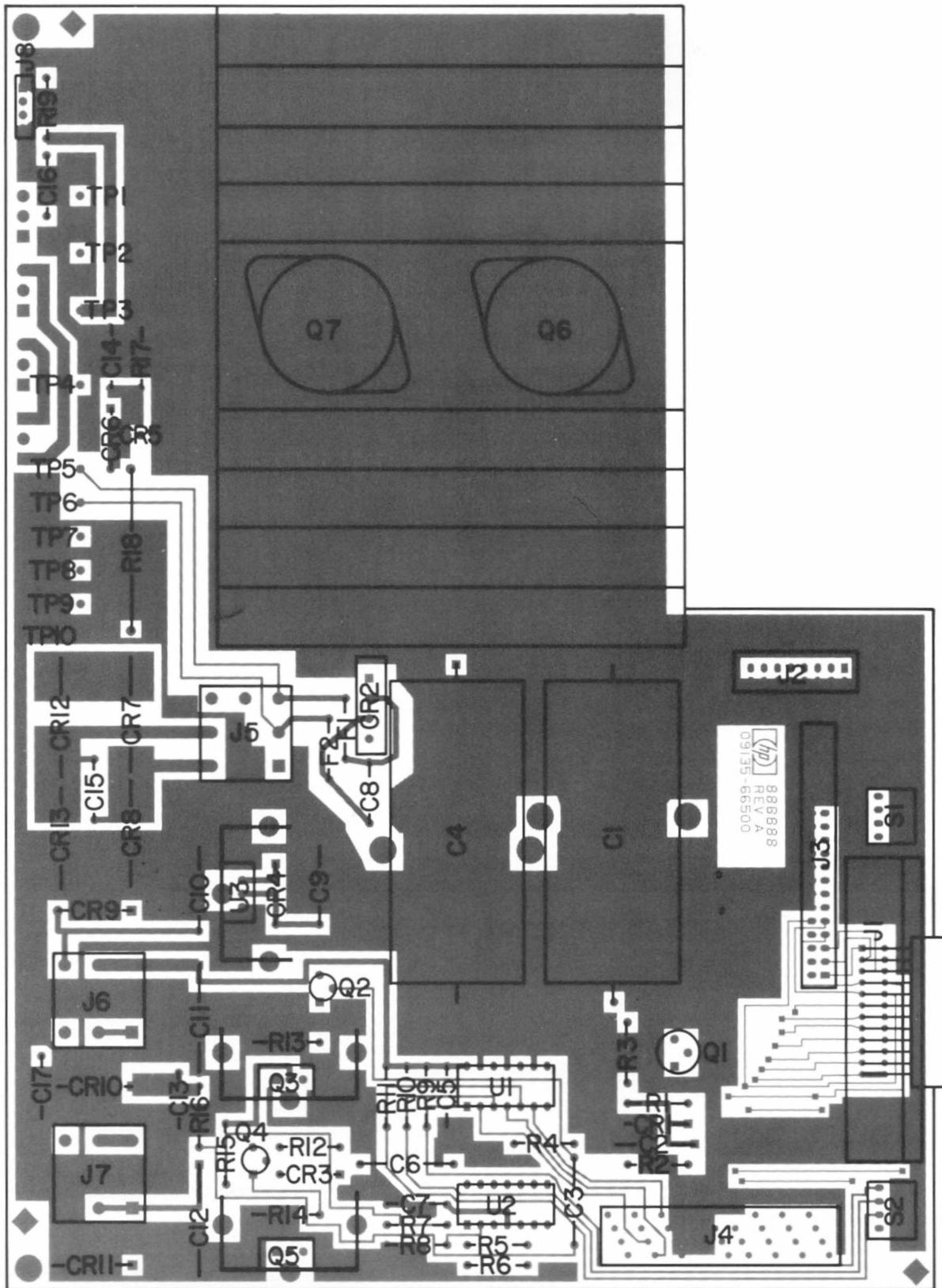


Figure 4-1. Component Locator 09135-69500

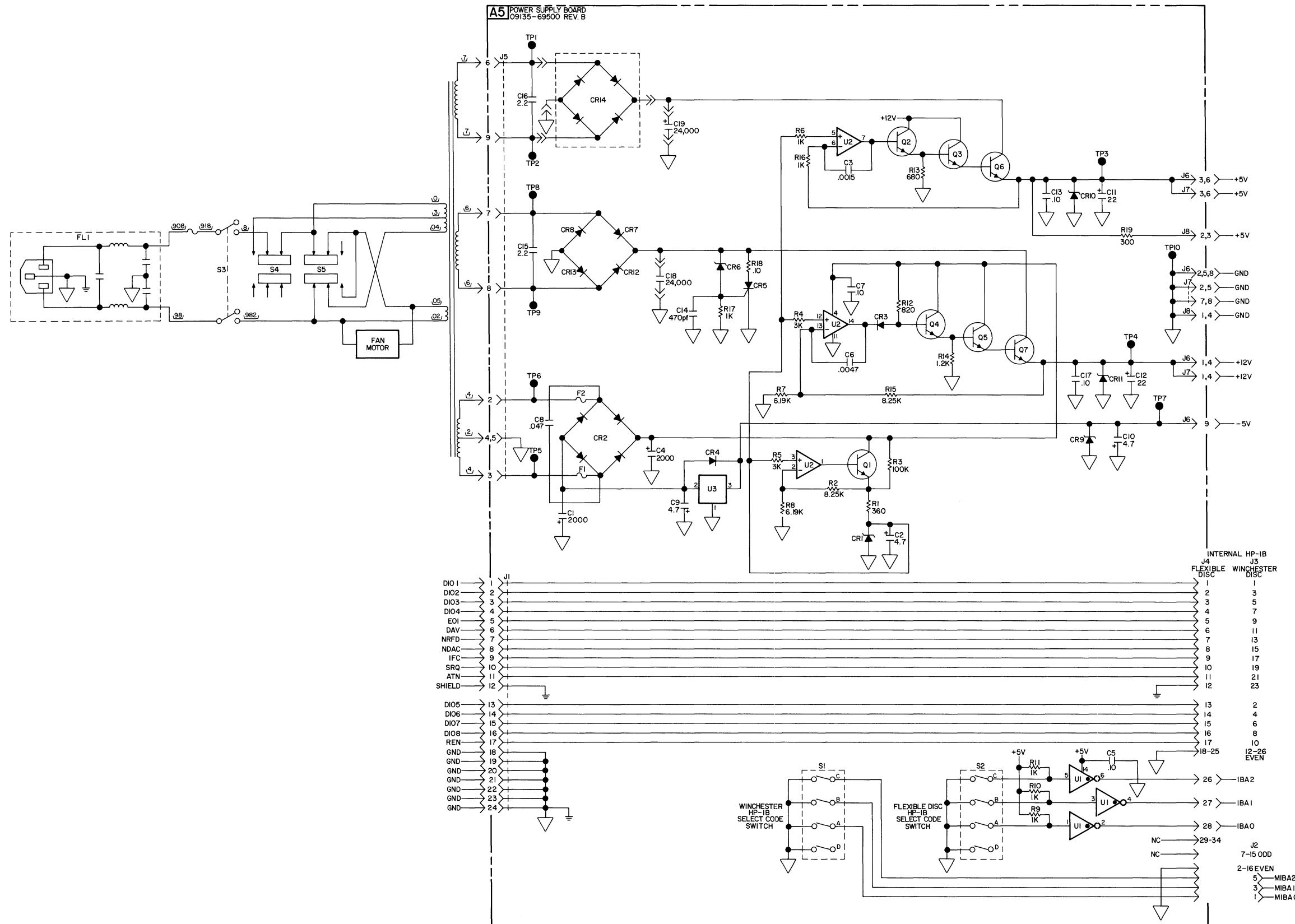


Figure 4-2. Power Supply Schematic 09135-69500

4-4 Schematic Diagrams

HP 9133A/B, 9134A/B, and 9135A

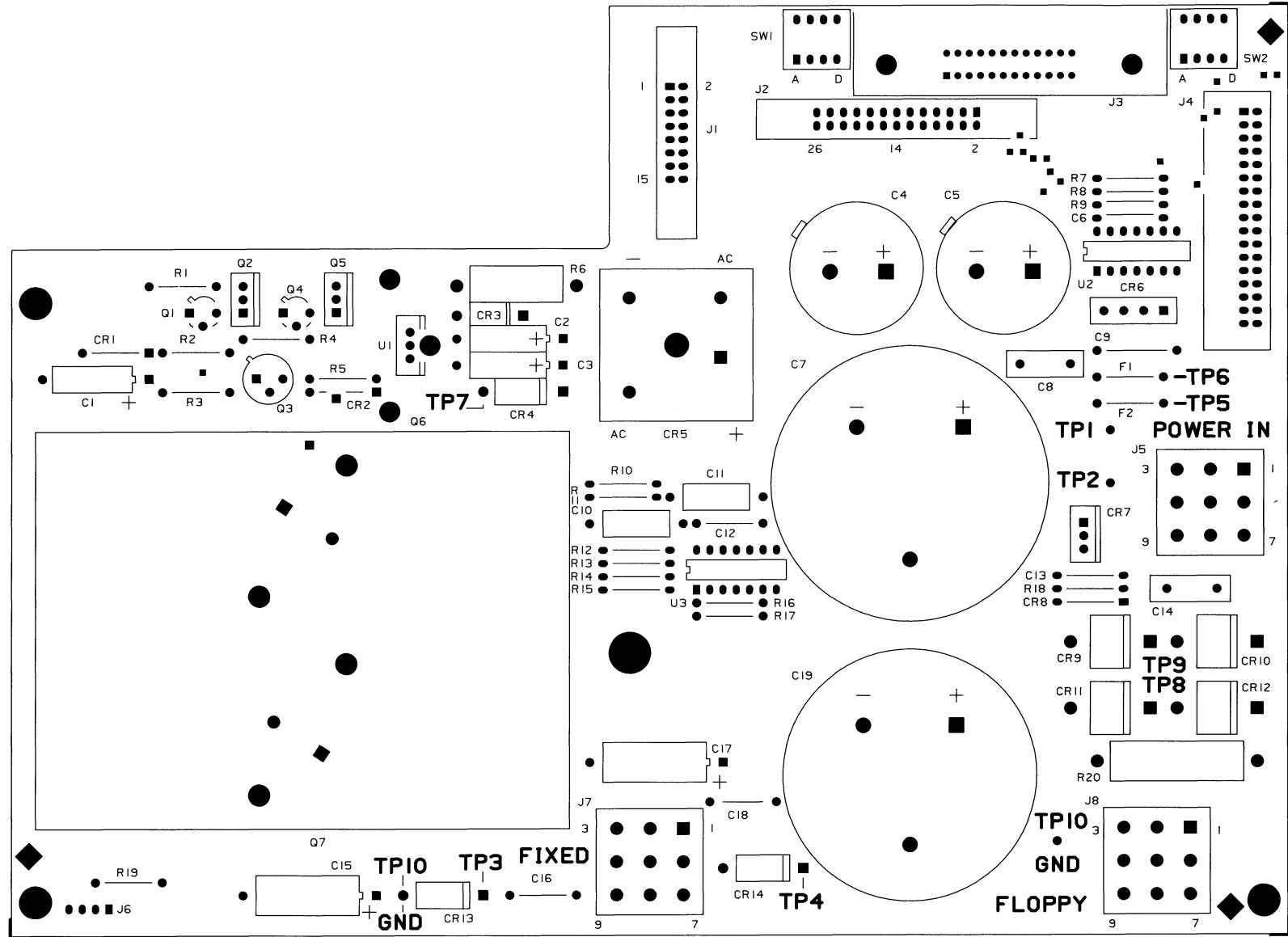


Figure 4-3. Component Locator 09135-69510

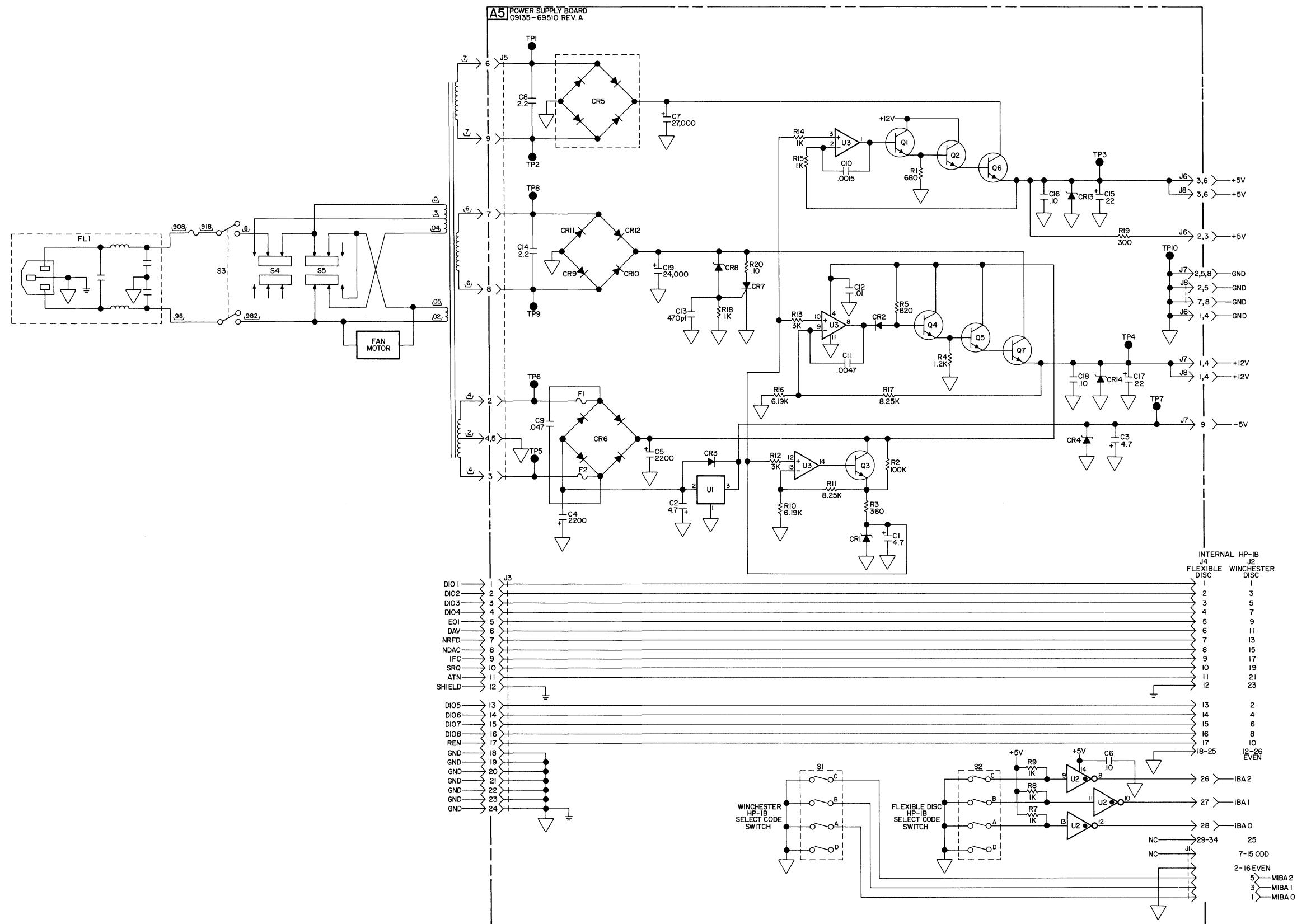


Figure 4-4. Power Supply Schematic 09135-69510

Chapter 5

Product Operation and Specifications

- HP 9133A/B Disc Memory
- HP 9134A/B Disc Memory
- HP 9135A Disc Memory

HP 9133A/B Disc Memory

The HP 9133A/B disc memory (Figure 5-1) is a random access data storage device which contains a 5-Mbyte 5 1/4-inch Winchester disc drive and a 3 1/2-inch flexible disc drive.

The 3 1/2-inch flexible disc emulates the HP 82902M 5 1/4-inch flexible disc drive with 286 Kbytes of data storage capacity. The Winchester drive within the 9133A has been designed to emulate an HP 9895A 8-inch flexible disc drive master with three slave drives (1.15 Mbytes per drive). Thus, HP computers that support the 9895A and 82902M flexible disc drives can operate the 9133A.

The HP 9133A Option 010 consists of a modification to the Winchester controller printed circuit assembly which causes the Winchester drive to appear as one large 4.82-Mbyte volume. The Winchester with option 010 responds to most of the commands used on the 9895A flexible disc drive.

The Winchester drive found in the 9133B provides 10 Mbytes of storage capacity in a single volume.

Refer to your computer's Mass Storage Manual for programming information for the HP 82902M and 9895A flexible disc drives.

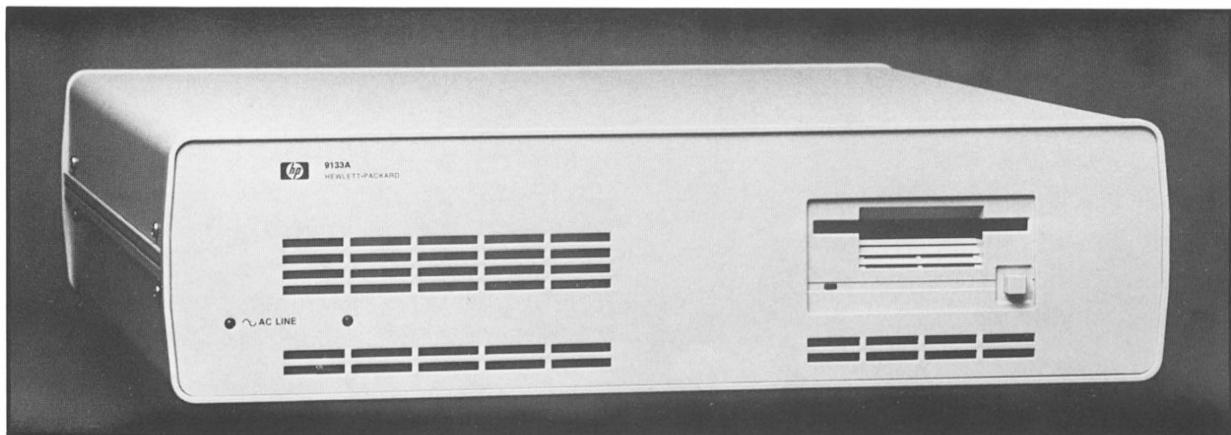


Figure 5-1. HP 9133A/B Disc Memory

Technical Specifications

Listed below are the physical, electrical, and environmental specifications for the HP 9133A/B disc memory.

Physical

Number of Drives:	1 - Winchester 1 - 3 1/2-inch flexible disc
Net Weight:	15.5 kg (34.7 lbs)
Height:	130 mm (5.125 in.)
Depth:	476 mm (18.7 in.)
Width:	425 mm (17 in.)
Formatted Storage Capacities:	4.6 Mbytes (9133A Standard 4-Volume) 4.8 Mbytes (9133A Optio 10 Single-Volume) 9.68 Mbytes (9133B)

Electrical

Power Source Requirements:	140 Watts
Line Frequency:	48 Hz to 66 Hz

Environmental

Operating Temperature:	10 to 40°C (50 to 104°F)
Operating Humidity:	20 to 80 %
Max. Wet Bulb Temperature:	25.5°C
Storage Humidity:	5 to 95 % (non-condensing)
Operating Altitude:	0 to 4600 m (0 to 15,000 ft)
Storage Temperature:	-40° to 70°C (-40° to 158°F)
Storage Altitude:	-300 to 15,200 m (-1000 to 50,000ft)

3 1/2-inch Flexible Disc Drive

HP Double Density Format

Encoding:	MFM
Rotational Speed:	600 RPM
Bit Density @ 600 RPM:	Track 69 (Inside track) 7610 BPI
Track Density:	135 tracks per inch
Tracks per Surface:	70
Surfaces used per disc:	1
Capacity	
Bytes/Sector:	256
Sectors/Track:	16
Tracks:	70
Bytes/Drive (Formatted):	286 Kbytes

Access Time

Track-to-Track Seek:	15 ms/track, plus 15 ms settling
----------------------	----------------------------------

Maximum Track-to-Track	
Seek (70 tracks):	1065 ms
Average Track-to-Track:	365 ms
Maximum Rotational Latency:	100 ms
Average Rotational Latency:	50 ms
Spindle Motor on time:	1 second
Maximum Data Access Time (Seek plus Latency plus Motor on time):	2.165 second
Average Data Access Time:	415 ms

Data Transfer Rates: (3 1/2-inch flexible disc only)

Interleave	Average Transfer Rate (Kbytes/second)
1	2.6
2	17.1
3	12.1
4	9.3
5	7.6
6	6.4
7	5.5
8	4.8
9	4.3
10	3.9
11	3.5
12	3.2
13	3.0
14	2.8
15	2.6

Maximum burst transfer rate for the 3 1/2-inch drive is 64.5 Kbytes/s writing and 67 Kbytes/s for reading. This is the capability of the 3 1/2-inch drive; your system transfer may vary due to your controller.

Interleave for the Winchester is preset at the factory and cannot be changed.

Refer to the beginning of this manual (Section I Chapter 1) for specifications on the Winchester drive.

System Operation

Refer to the 9121D/S Service Manual P/N 09121-90030 for operation of the 3 1/2-inch flexible disc.

Write Protection

There is no write protect capability on the Winchester drive. Caution must be used to avoid erasing or initializing over data you want to keep.

Controls and Indicators

The indicators are located on the front panel. The indicators, as shown in Figure 5-2, are the disc access light for the Winchester drive and the head load indicator for the 3 1/2-inch flexible disc drive. The Winchester drive light is illuminated whenever the disc is accessed for data storage or retrieval and momentarily when the drive is powered-up. The flexible disc drive light lights up whenever the unit is powered-up, the head is loaded or when the drive is selected.

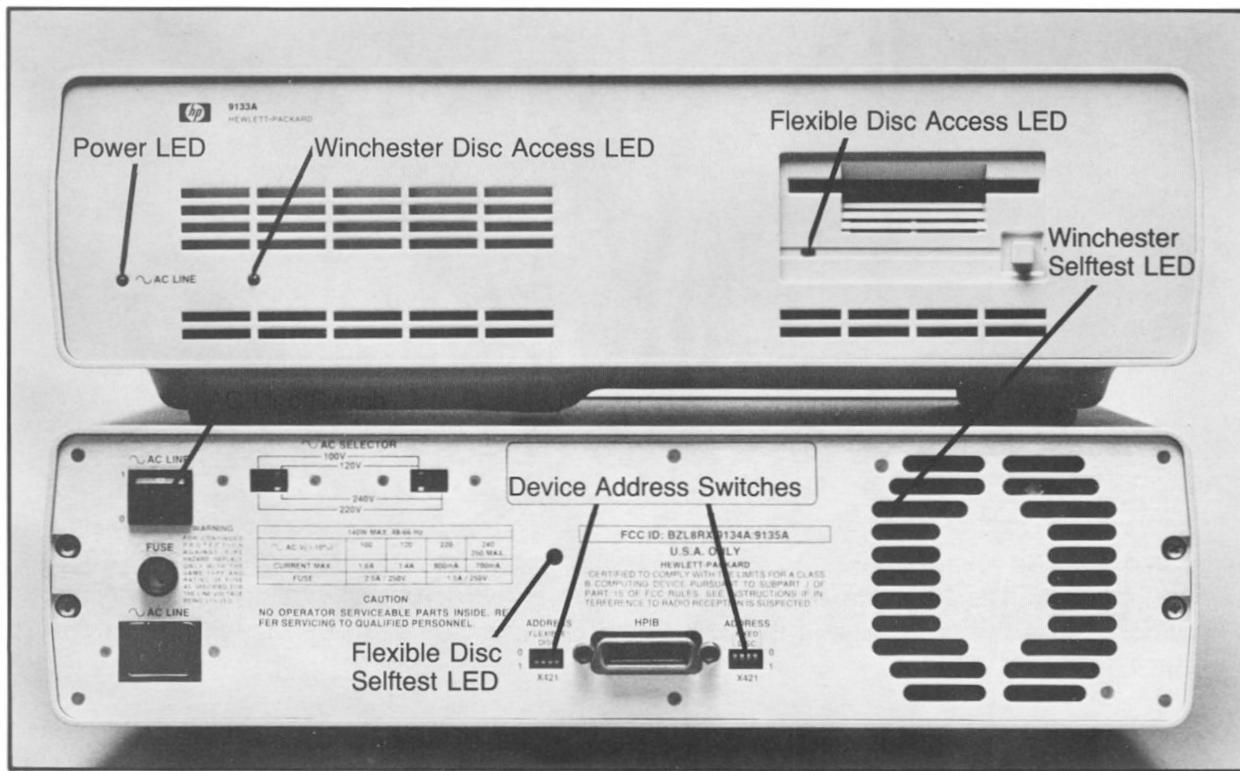


Figure 5-2. Controls and Indicators

CAUTION

THE ACTIVITY LIGHT ON THE FRONT OF THE DRIVE INDICATES USAGE OF THAT DRIVE. DO NOT DEPRESS THE DISC EJECT BUTTON WHEN THE ACTIVITY LIGHT IS ON.

Applying Power

Locate the AC line switch on the rear panel and set it to the "ON" or "1" position. The disc drive requires about 30 seconds after the application of power before it is ready for operation or before you insert your disc. See the section titled "Selftest LED" for the power-on selftest indication in the Appendix.

HP 9134A/B Disc Memory

The HP 9134A/B Disc Memory (Figure 5-3) is a random access data storage device. The disc memory contains a 5 1/4-inch Winchester disc drive. The drive in the 9134A provides either 4.6 Mbytes or 4.8 Mbytes of data storage (option 010). The 9134B provides 10 Mbytes of data storage.

The Winchester drive in the 9134A has been designed to emulate an HP 9895A 8-inch flexible disc drive master with three slaves. Thus, most HP computers that support the 9895A flexible disc drive can operate the HP 9134A Winchester drive.

Refer to the Mass Storage Manual for your computer for programming information for the HP 9895A.

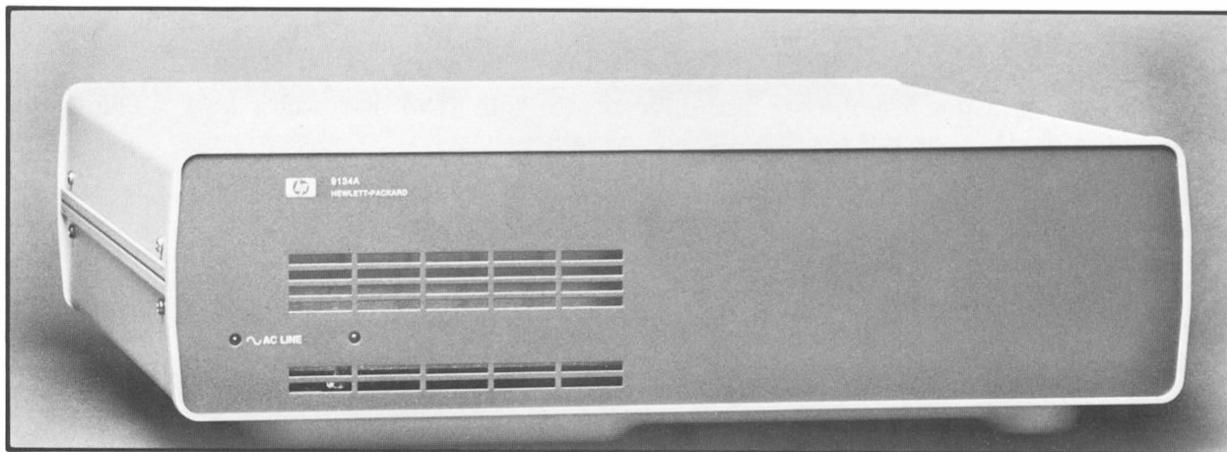


Figure 5-3. HP 9134A/B Disc Memory

Technical Specifications

Listed below are the electrical and physical specifications for the HP 9134A/B disc memory.

Number of drives:	1 Winchester
Net Weight:	13.4 kg (31.5 lbs)
Height:	130 mm (5.125 in)
Depth:	476 mm (18.7 in)
Width:	425 mm (17 in)
Formatted Storage Capacities:	4.6 Mbytes (9134A) 4.8 Mbytes (9134A option 010) 9.68 Mbytes (9134B)

Interface:	HP-IB
System:	System Dependent
Electrical	
Power Source Requirements:	140 Watts
Line Frequency:	48Hz to 66Hz
Environmental Specs:	
Operating Temperature:	10 to 40°C (50 to 104°F)
Operating Humidity:	20 % to 80 %
Max. Wet Bulb Temperature:	25.5°C non-condensing
Operating Altitude:	0 to 4600 m (0 to 15,000 ft)
Storage Humidity:	5 to 95 % non-condensing
Storage Temperature:	-40 to 60°C (-40 to 140°F)
Storage Altitude:	-300 to 15,200m (-1000 to 50000 ft)

Write Protection

There is no write protect capability on the Winchester drive. Caution must be used to avoid erasing or initializing over data you want to keep.

Controls and Indicators

The indicators are located on the front panel. The indicators, as shown in Figure 5-4, are the power-on light, and the Winchester disc drive access light. The disc access light is illuminated whenever the disc is accessed for data storage or retrieval.

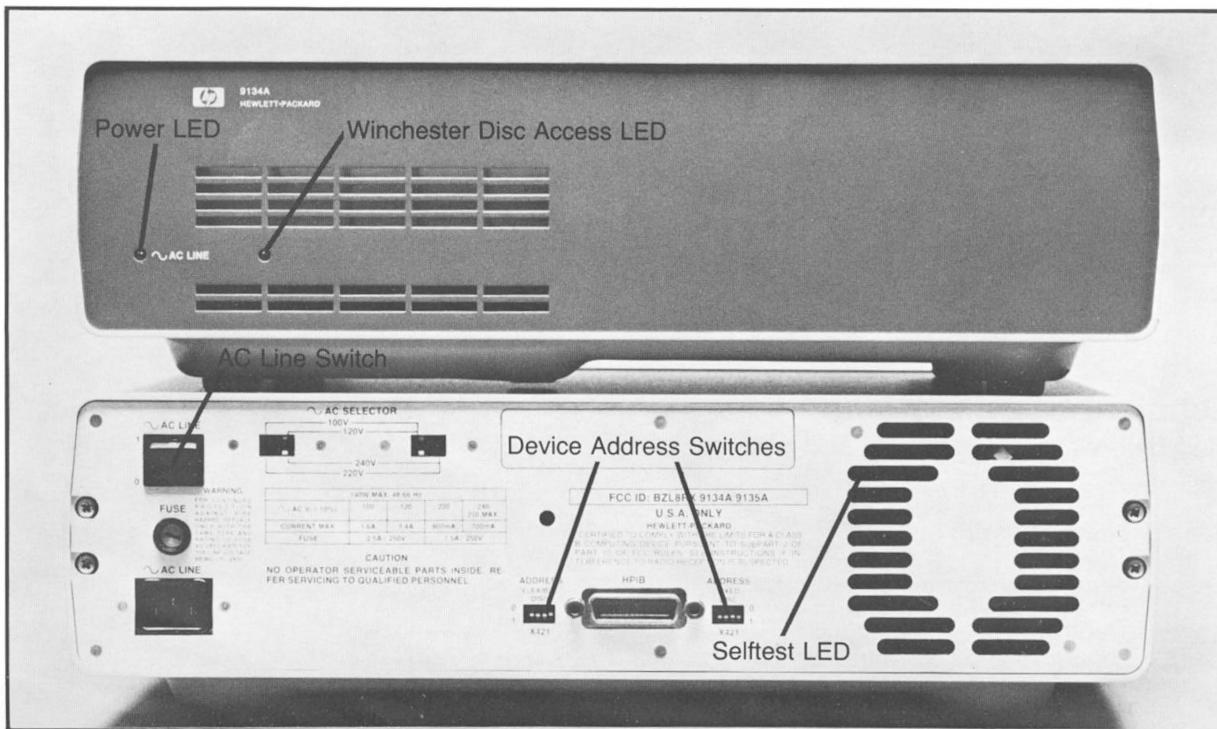


Figure 5-4. Controls and Indicators

Applying Power

Before turning the disc memory on, be sure to perform all the procedures in the installation section Chapter 6 of this Section. Locate the AC line switch on the rear panel and set it to the "ON" or "1" position. The Winchester disc drive requires about 30 seconds after the application of power before it is ready for operation.

HP 9135A Disc Memory

The HP 9135A Disc Memory (Figure 5-5) is a random access data storage device. The disc memory contains both a 5 1/4-inch Winchester disc drive and a 5 1/4-inch flexible disc drive.

The Winchester drive has been designed to emulate an HP 9895A 8-inch flexible disc drive master with three slaves. Thus, most HP computers that support the 9895A flexible disc drive can operate the Winchester drive in the HP 9135A. Only computers that support the HP 9895A and HP 8290X disc drives can fully operate both disc drives in the HP 9135A.

Refer to the Mass Storage Manual for your computer for programming information for either the HP 9895A (used for the Winchester drive), or HP 8290X 5 1/4-inch flexible disc drive (used for the flexible disc drive in the HP 9135A).

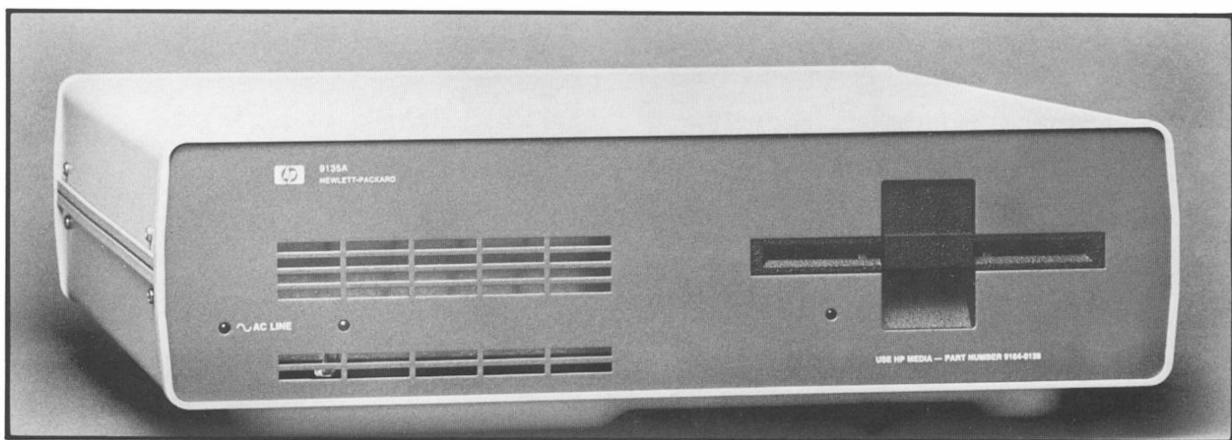


Figure 5-5. HP 9135A Disc Memory

Technical Specifications

Listed below are the electrical and physical specifications for the HP 9135A disc memory.

Number of drives	1 5 1/4-inch Winchester 1 5 1/4-inch flexible disc
Net Weight	18.1 kg (40 lbs)
Height	130 mm (5.125 in)
Depth	476 mm (18.7 in)
Width	425 mm (17 in)
Formatted Storage Capacities:	4.6 Mbytes Winchester or

Interface:	4.8 Mbyte Winchester 270 Kbytes flexible disc
System:	HP-IB System Dependent
Rotational Speed:	3600 RPM \pm 1 % Winchester 300 RPM \pm 1.5 % flexible disc
Electrical	
Power Source Requirements	140 Watts
Line Frequency	48Hz to 66Hz
Environmental Specs:	
Operating Temperature	10 to 40°C (50 to 104°F)
Operating Humidity	20 % to 80 %
Max. Wet Bulb	
Temperature	25.5°C non-condensing
Storage Humidity	5 to 95 % (non-condensing)
Operating Altitude	0 to 4600m (0 ft to 15,000 ft)
Storage Temperature	-40 to 60°C (-40 to 140°F)
Storage Altitude	-300 to 15,200m (-1000 to 50,000ft)

NOTE

The flexible disc in the HP 9135A disc memory is designed for operation in a typical office environment. Use of the equipment in an environment containing corrosive substances will cause the flexible disc drive and media life to be drastically reduced.

Write Protection

There is no write protect capability on the Winchester drive. Caution must be used to avoid erasing or initializing over data you want to keep.

Controls and Indicators

The indicators are located on the front panel. The indicators, as shown in Figure 5-6, are the disc access light for the Winchester drive and the head load indicator for the 5 1/2-inch flexible disc drive. The Winchester drive light is illuminated whenever the disc is accessed for data storage or retrieval and momentarily when the drive is powered-up. The flexible disc drive light lights up whenever the unit is powered-up, the head is loaded or when the drive is selected by your host controller.

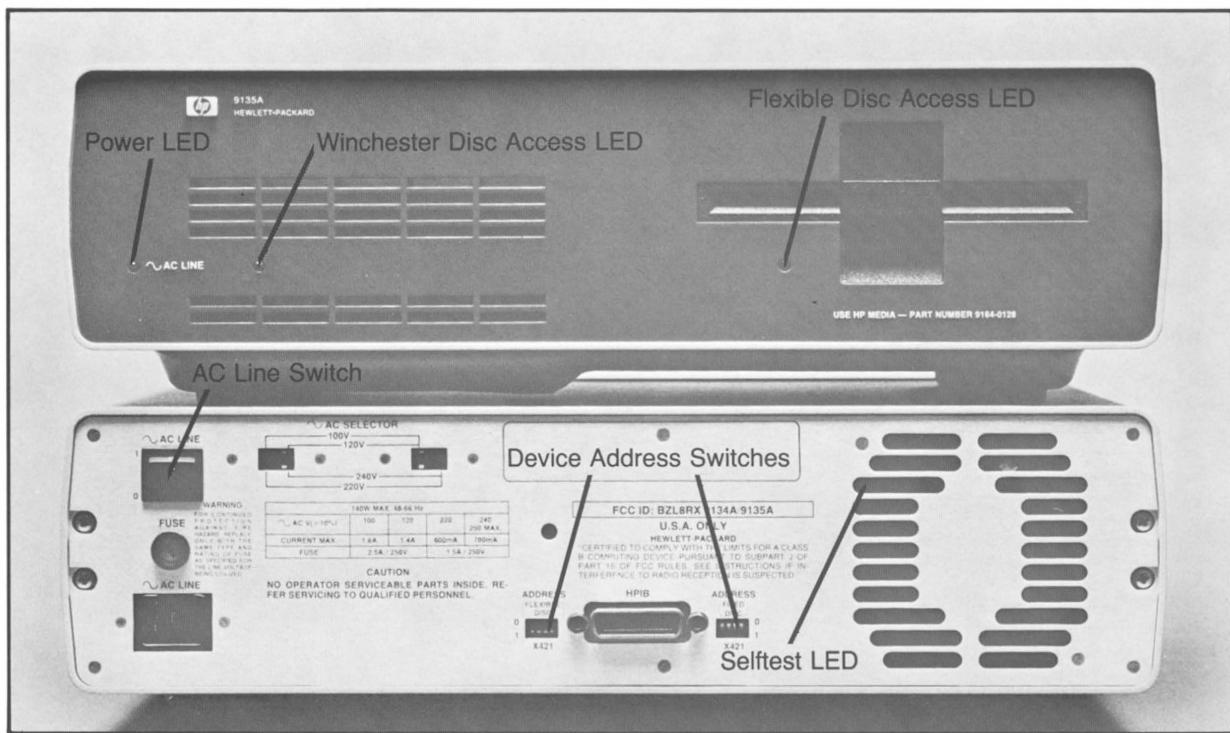


Figure 5-6. Controls and Indicators

CAUTION

THE ACTIVITY LIGHT ON THE FRONT OF THE DRIVE INDICATES USAGE OF THAT DRIVE. DO NOT DEPRESS THE DISC EJECT DUTTON WHEN THE ACTIVITY LIGHT IS ON.

Applying Power

Locate the AC line switch on the rear panel and set it to the "ON" or "1" position. The disc drive requires about 30 seconds after the application of power before it is ready for operation or before you insert the flexible disc.

Chapter 6

Product Installation

- Equipment Supplied
- Unpacking Your Disc Memory
- Configuring Power
- Interfacing the Disc Memories to Your System
- Cleaning The Case

Equipment Supplied

Please check to insure that your customer has received all of the standard equipment. If any items are incorrect or missing, please contact the order processing department at the factory.

Table 6-1 Equipment Supplied

Description	Quantity	HP Part Number	
Power Cable	1	Dependent on location (Refer to Power Cord Section)	
User's Manual	1	09134-90000	
Fuse	1	100 to 120 VAC 2.5 Amp Or 220 to 240 VAC 1.5 Amp	2110-0083
		Dependent on Power Cord	2110-0043

A package of ten 3 1/2-inch flexible discs can be ordered using the 92191A product number.

A package of ten 5 1/4-inch flexible discs can be ordered using the 92190A product number.

Unpacking Your Disc Memory

Your disc memory was carefully inspected before shipment. Remove the unit from the shipping carton and carefully inspect the unit for any physical damage that may have occurred during shipment. If you find any damage, you should immediately notify your dealer and file a claim with any carriers involved.

If the disc memory is moved, be careful when picking it up and setting it down.

**CAREFULLY REPACK THE DISC MEMORY IN THE ORIGINAL SHIPPING CARTON
BEFORE TRANSPORTING IT TO ANOTHER SITE.**

CAUTION

THE DISC MEMORY IS A PRECISION INSTRUMENT. MECHANICAL SHOCK CAN MISALIGN THE READ/WRITE HEADS, RESULTING IN READ ERRORS AND/OR DAMAGED DISCS WHETHER THE DISC IS OPERATING OR NOT.

CAUTION

EVIDENCE OF EXCESSIVE SHOCK WILL VOID THE WARRANTY.

Configuring Power

The following information should be used to configure your disc memory device power for proper operation in your area.

Setting the Line Voltage Select Switches

The voltage select switches on the rear panel must be set to the nominal line voltage for the area in which it is operating. Figure 6-1 shows the setting of the voltage select switches for the various line voltages.

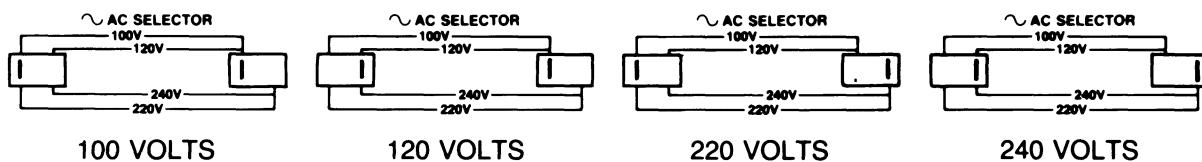


Figure 6-1. Line Voltage Select Switches

Fuses

A different fuse is required for each of the two voltage ranges of 110-120 and 220-240 VAC. Table 6-2 gives the correct fuse ratings and fuse part numbers.

Table 6-2. Fuses

Voltage Range	Fuse Rating	HP Part Number
100 & 120 VAC	2.A 250 VAC Normal Blow	2110-0083
220 & 240 VAC	1.A 250 VAC Normal Blow	2110-0043

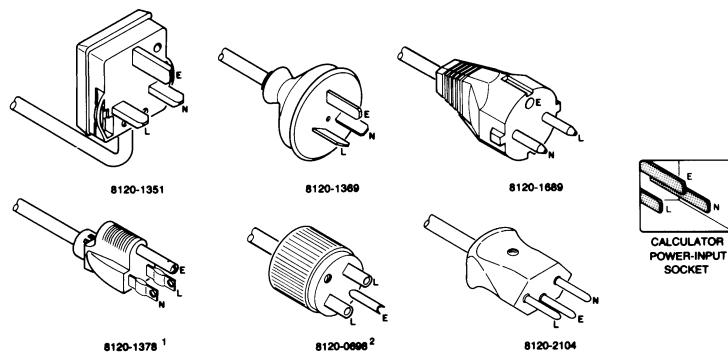
WARNING

ALWAYS DISCONNECT THE DISC MEMORY FROM THE AC SOURCE BEFORE CHANGING FUSES.

Power Cords

Power cords supplied by HP have polarities matched to the power-input socket on the equipment (Figure 6-2).

- * L = Line or active conductor (also called "live" or "hot")
- * N = Neutral or identified conductor
- * E = Earth or safety ground



¹UL and CSA approved for use in the United States of America and Canada with equipment set for either 100 or 120 Vac operation.

²UL and CSA approved for use in the United States of America and Canada with equipment set for either 200 or 240 Vac operation.

Figure 6-2. Available Power Cords

WARNING

IF IT IS NECESSARY TO REPLACE THE POWER CORD, THE REPLACEMENT CORD MUST HAVE THE SAME POLARITY AS THE ORIGINAL. OTHERWISE, A SAFETY HAZARD MIGHT EXIST IF AN INTERNAL FAILURE OCCURS.

Power cords with different plugs are available for equipment; the part number of each cord is shown in Figure 6-2. Each plug has a ground connector. The cord packaged with the equipment depends upon where the equipment is to be delivered.

Interfacing the Disc Memories to Your System

The Disc Memories is connected to the computer via the Hewlett-Packard Interface Bus (HP-IB). The device address switches are set prior to connecting the interface cable.

Selecting the Device Address

Each device in an HP-IB system must be set to a unique device address. The HP 9133A/B or HP 9135A each contain two separate devices in the same the package. A device address switch is provided for each device. See Figure 6-3 for switch locations.

Prior to setting the device address switches, turn the disc memory AC line switches OFF.

The switches can be set to any one of eight device addresses, ranging from decimal 0 through 7. Refer to Figure 6-3 to set these switches to the desired device address.

Address	Switch Segments				
	X	4	2	1	
0	***	UP	UP	UP	(Factory setting for Winchester)
1	***	UP	UP	DOWN	
2	***	UP	DOWN	UP	(Factory setting for flexible disc)
3	***	UP	DOWN	DOWN	
4	***	DOWN	UP	UP	
5	***	DOWN	UP	DOWN	
6	***	DOWN	DOWN	UP	
7	***	DOWN	DOWN	DOWN	

*** = Don't Care

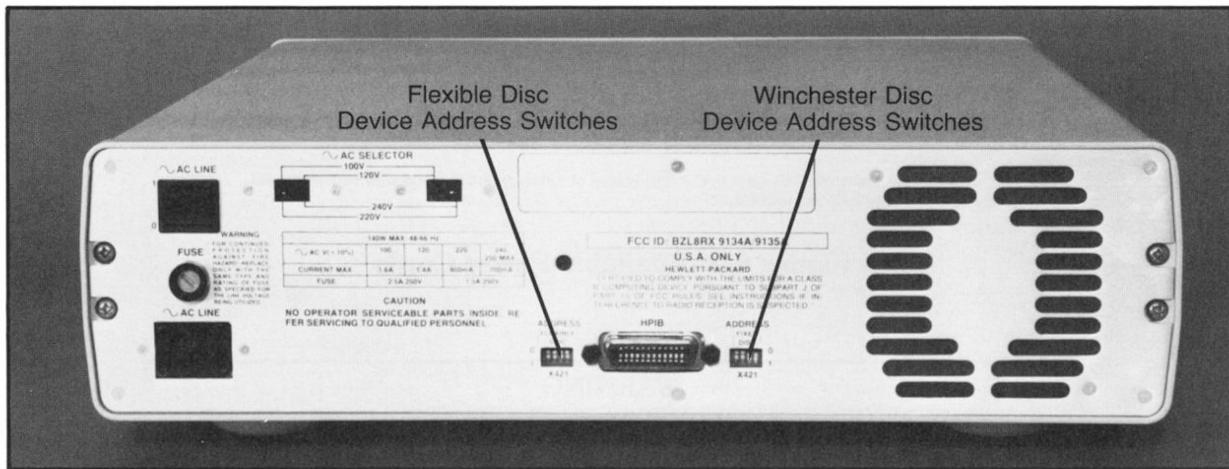


Figure 6-3 . Device Address Switch Setting

Refer to Figure 6-4 for a list of the HP-IB interface cables used with HP computers.

HP-IB Interface Restrictions:

1. All the AC line switches must be turned "OFF" when connecting (and disconnecting) devices to your system.
2. The total length of cable permitted in one bus system must be less than or equal to two metres times the number of devices connected together (the interface card is counted as one device).
3. The total length of the cable must not exceed 20 metres. For example, a system containing six devices can be connected together with cables that have a total length less than or equal to 12 metres (six devices x 2m/device = 12 metres). The individual lengths of cable can be distributed in any manner desired as long as the total length does not exceed the allowed maximum. If more than 10 devices are to be connected together, ca-

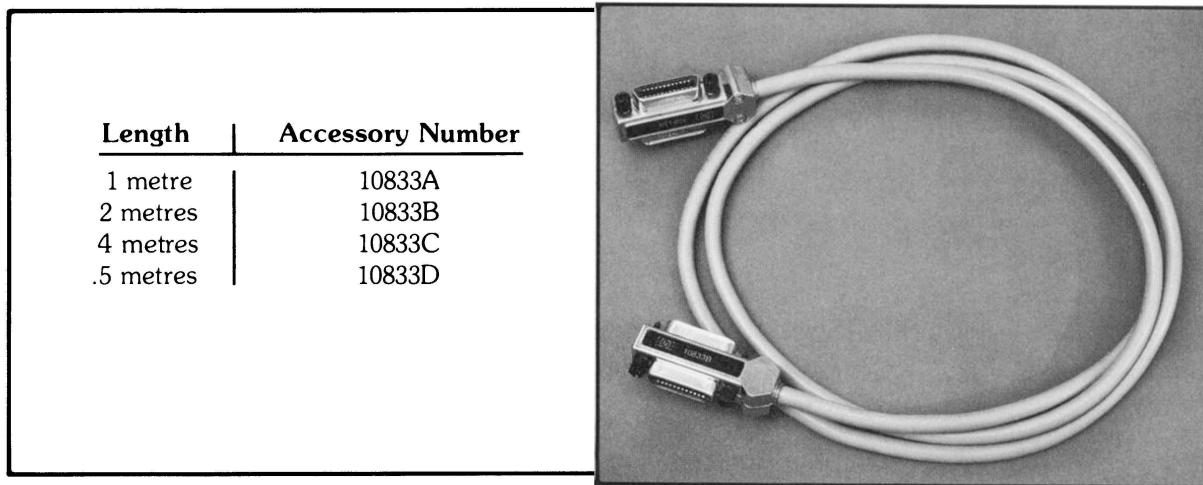


Figure 6-4. HP-IB Interface Cables

bles shorter than two metres must be used between some of the devices to keep the total cable length less than 20 metres.

4. The maximum number of devices that can be connected together in one bus system is 15.

There are no restrictions to the way cables may be connected together; however, it is recommended that no more than four piggyback connectors be stacked together on one device. The resulting structure could exert enough force on the connector mounting to damage it.

Cleaning the Case

The disc memory case has been painted with a durable, long lasting, non-toxic paint. It will preserve the appearance of the disc memory for many years. The following instructions for cleaning below will not harm the quality finish.

CAUTION

CHEMICAL SPRAY-ON CLEANERS USED FOR APPLIANCES AND OTHER HOUSEHOLD AND INDUSTRIAL APPLICATIONS MAY DAMAGE THE CASE FINISH. THESE OR OTHER CHEMICAL CLEANERS SHOULD NOT BE USED. DO NOT USE DETERGENTS THAT CONTAIN AMMONIA, BENZENES, CHLORIDES, OR ABRASIVES.

Before cleaning the disc memory case, disconnect the power cord and any interconnecting cables. Dampen a clean, soft, lint-free cloth in a solution of clean water and mild soap. Wipe the soiled areas of the case, ensuring that no cleaning solution gets inside the unit. For cleaning more heavily soiled areas, a solution of 80 % clean water and 20 % isopropyl alcohol may be used. Wipe the case areas that had cleaning solution applied with a clean, soft, lint free cloth dampened in clean water, then dry the case with a dry, soft, clean cloth. A non-abrasive eraser may be used to remove pen and pencil marks.

Section III HP 9133V, 9133XV, and 9134XV Disc Memory Products

Chapter 1

Controller & Power Supply Theory of Operation

- General Description
- Power Supply Theory of Operation
- Controller Theory of Operation

General Description

This section describes the 5 1/4-inch Winchester disc drive as used in HP 9133V, 9133XV, and 9134XV Disc Memories:

The 9133V/XV and 9134XV Family

	V (5-Mbyte) Winchester	XV (15-Mbyte) Winchester	3 1/2-inch Flexible Disc
HP 9133V	X		X
HP 9133XV		X	X
HP 9134XV		X	

The Winchester drive in these products is available in three configurations. The 9133V can be configured as either a single volume of 4.8-Mbytes or four volumes of 1.15-Mbytes for a total of 4.6-Mbytes. The 9133XV and 9134XV are always configured as a single volume of 14.5-Mbytes capacity.

All three configurations are accomplished by jumper selection on the PCA; the firmware does not change. The user's mainframe must have an operating system designed to support the selected configuration.

Table 1-1 summarizes these configurations.

Table 1-1

Option	Logical Configuration	Formatted Capacity	Jumper Configuration (J3 Pins)
Standard-V	single volume	4.8-Mbyte	C 00 (Removed) B XX (Installed) A XX (Installed)
004-V	four volumes, 1.15-Mbyte each	4.6-Mbyte	C 00 (Removed) B 00 (Removed) A XX (Installed)
Standard-XV	single volume	14.5-Mbyte	C XX (Installed) B 00 (Removed) A XX (Installed)

Figure 1-1 shows the 9133-69508 Controller PCA with the jumper positions listed above visible and called out:

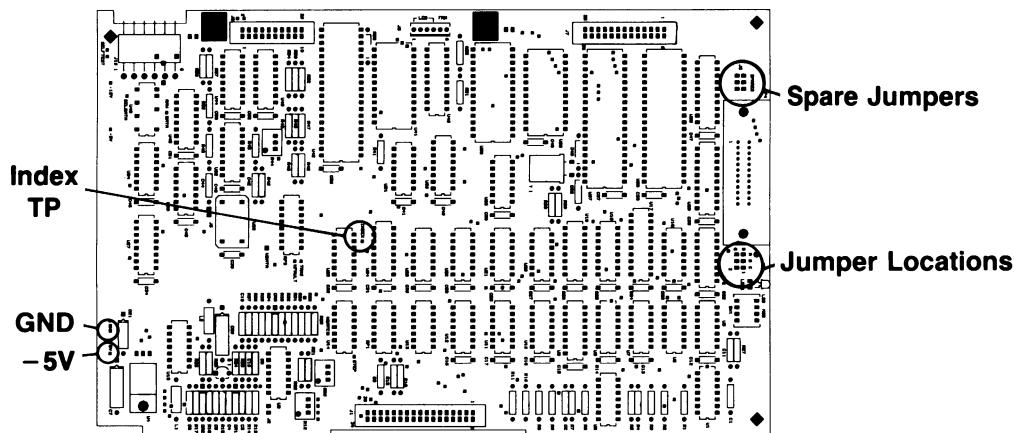


Figure 1-1. The 09133-69508 Controller PCA

Product Hardware Assemblies

Table 1-2 lists by part number the assemblies associated with the Winchester drive.

Table 1-2. Product Hardware Assemblies

Product	Drive Model	Drive Part No.	Drive Electronics	Controller	ROM-IC
HP 9133V	ST406	09133-69100	09133-69103	09133-69508	09133-15520
HP 9133XV	ST419	09133-69104	09133-69105	09133-69508	09133-15520
HP 9134XV	ST419	09133-69104	09133-69105	09133-69508	09133-15520

Winchester drive models used in the 9133V/XV and 9134XV products:

- ST406 - Single-Platter 5-Mbyte (improved track density)
- ST419 - Triple-Platter 15-Mbyte (improved track density)

Power Supply Theory of Operation

Refer to Figure 1-2 while reading the following discussion of the power supply.

Introduction

The same power supply is used for the HP 9133V/XV and 9134XV. All power to the 3 1/2-inch Flexible Disc Drive is routed through the lower board of the 3 1/2-inch controller (09133-69507). The 5V line to the drive is not enabled until the PVAL line from the power supply enables it. The fan is powered by -12V and is connected to the Winchester controller PCA. The power supply brings the +5V and -12V to the Winchester controller and -5V is generated from the -12V line on the controller. The -5V line is used for the phase-lock loop circuitry. The front panel LEDs are connected to 5V on the Winchester disc controller.

This power supply is a 95-watt switching supply that provides outputs of +5V at 5.6 amperes, +12V at .5 amperes, (1.5 amperes maximum surge), +12VP at 2.7 amperes (4.5 amperes maximum surge), and -12V at 0.6 amperes. The +12VP output is a dedicated

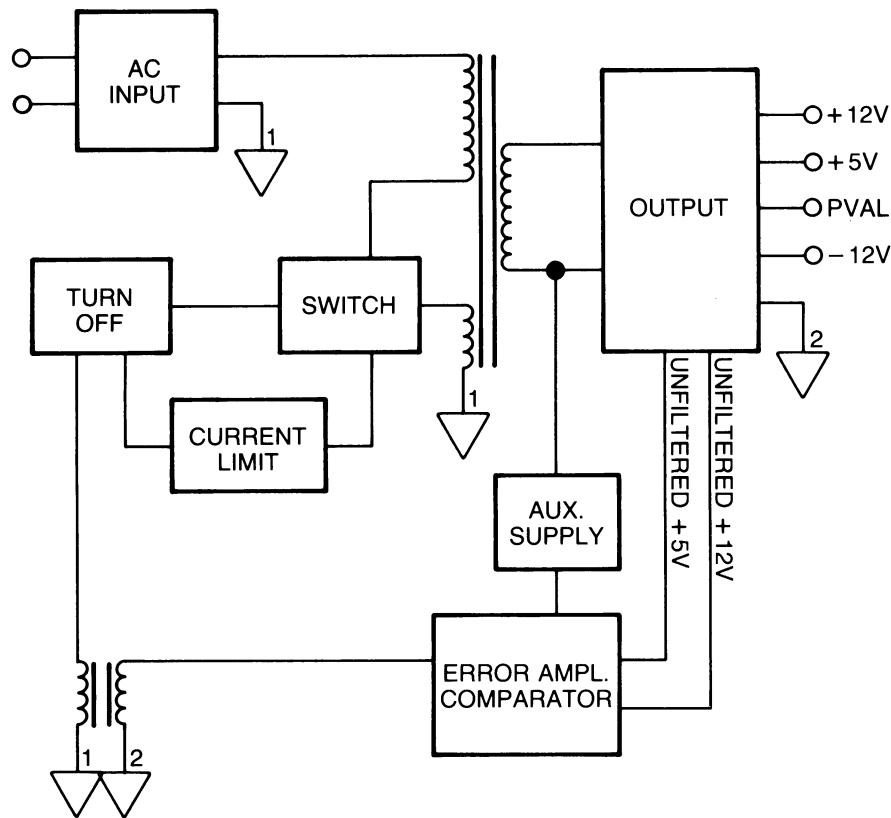


Figure 1-2. Power Supply Block Diagram

+12V supply for the Winchester disc drive. The power-on reset signal is also produced by the power supply. Details of the power supply circuitry are provided in the following paragraphs.

AC Input Circuits

The AC line voltage is connected to the power supply through a printed circuit board (PCB) mounted line cord receptacle. A PCB-mounted power on/off switch controls both sides of the AC line into the power supply. There is a fuse in the hot side of the AC input following the power switch. The fuse value for 115 VAC is 3 amperes and for 230 VAC is 2 amperes. A line filter following the fuse reduces the level of the line transients entering the power supply and the amount of switching noise leaving the power supply.

Also associated with the input circuitry is a line voltage switch that selects nominal voltages of 115 VAC or 230 VAC. When the switch is in the 115 VAC position, a surge voltage protection device protects the power supply from damage if it is inadvertently connected to 230 VAC. A blown line fuse is the only damage that can occur.

A diode array and several capacitors rectify and filter the incoming AC lines. Included in this network are two thermistors that limit the initial power on surge current to approximately 25 amperes peak at 115 VAC and 230 VAC.

Power-on Reset

The power-on reset circuit in the power supply produces the Power-Valid signal, PVAL. This signal can only source current. At power-on, a pull-down resistor on the Winchester controller PCA keeps PVAL low for at least 100 milliseconds after the +5V output exceeds 4.75V. PVAL is then driven HIGH and remains HIGH while the +5 output is in spec. PVAL is turned off, allowing the pull-down resistor to cause a low level at least 500 microseconds before the +5V output falls below 4.75V.

The Winchester controller PCA uses PVAL to generate RESET, which resets all logic on both controllers. In addition, PVAL is used by the flexible disc controller to withhold +5V from the 3 1/2-inch drive during power-on.

Controller Theory of Operation

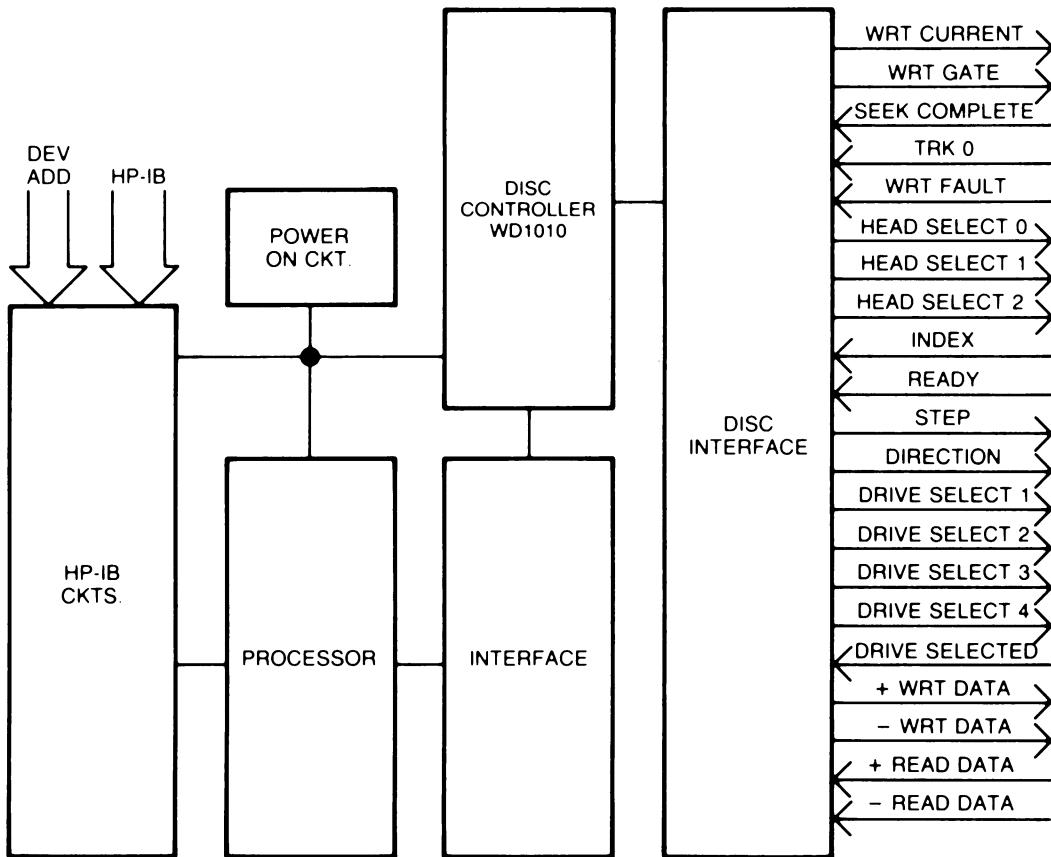


Figure 1-3. Controller Block Diagram

Microprocessor Circuit

The microprocessor is a 68B09 8-bit processor with a 2-MHz bus rate. Timing is provided by an internal oscillator which drives an 8-MHz crystal. The output of the oscillator is divided by four to provide two 2-MHz signals (E and Q). The signals are phase shifted 90 degrees with respect to each other, so that Q leads E. The address present on the address bus is valid whenever either E or Q is high.

Program memory for the microprocessor is stored in an 8-Kbyte ROM. The ROM is selected whenever address line A15 is high and the VMA (valid memory address = E + Q) is high.

Scratch-pad memory for the processor consists of 128 bytes of RAM. The RAM is selected by three of the chip select lines provided on the chip. The condition necessary to select the RAM is A15 low and A07 high and E high.

Disc Controller, HP-IB Chip, Input and Output Ports

The disc controller HP-IB chip (8291A) and input and output ports are selected by strobe lines from a 3-line to 8-line decoder. The decoder is selected when $VMA = Q + E$ and the ROM is not selected (A15 low). When the decoder is selected, one of the 8 output lines is pulled low depending on the sense of address lines A05, A06, and A07. The four outputs that correspond to A07 being 1 are not used since the RAM is addressed when this occurs.

The input port is 8 bits wide. The bit assignments are as follows:

- BIT 7--Not Used
- BIT 6--LED_ON_L (CURRENT STATE OF SELFTEST LED)
- BIT 5--C }
BIT 4--B } (SEE FIGURE 1-1 FOR CONFIGURATIONS SELECTED)
BIT 3--A }
- BIT 2--ADDR2_L (MSB OF HP-IB ADDRESS)
- BIT 1--ADDR1_L
- BIT 0--ADDR0_L (LSB OF HP-IB ADDRESS)

The output port is 8 bits wide. The bit assignments are as follows:

- BIT 7--BUFFER_READY_H
- BIT 6--LED_ON_L
- BIT 5--NOT CONNECTED
- BIT 4--NO ASSIGNMENT
- BIT 3--PRE_COMP_DISABLE_H
- BIT 2--BUFFER_COUNTER_CLEAR_L
- BIT 1--NOT CONNECTED
- BIT 0--WD_RESET_L

The disc controller chip provides most of the control signals needed by the drive. It communicates with the microprocessor through 7 input and output registers and an external RAM buffer. The disc controller chip keeps track of which cylinder the head is positioned over, and when it is necessary to move the head. It controls the direction line and issues the appropriate number of step pulses. It also does the parallel-to-serial conversion, MFM encoding, and generates the precomp control signals necessary for a write operation. On a read operation, the disc controller chip does the MFM decoding, and the serial-to-parallel conversion. The disc controller chip also provides verification of sector headers, control of the phase-lock loop, checking of the error detecting CRC bytes, and automatic initiation of 8 to 16 retries if an error is detected.

The data separator reconstructs the clock from the incoming MFM-encoded bit stream and generates a 5-MHz clock with phase relationship to the incoming data such that nominal data transitions are centered on one level of the read clock and nominal clock transitions are centered on the other level. The read clock is generated by dividing down a 10 MHz clock that is phase locked to a delayed copy of the incoming data. The phase-lock loop uses a digital phase detector whose output is pump-up or pump-down pulses with a pulse width proportional to the phase error. The phaseup line is provided to allow the VC0 (Voltage Controlled Oscillator) to be started up in phase with the incoming data signal to minimize lock-up time.

Chapter2

Assembly Access

- Introduction
- Safety Considerations
- Assembly Access

Introduction

This chapter describes access to 9133V/XV and 9134 XV Disc Memories and the removal of the Winchester disc drive, the printed circuit assemblies (PCAs) controlling it, and the power supply used in all three products.

Safety Considerations

General

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

Safety Symbols



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.



Indicates hazardous voltages.



Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which if not correctly performed, could result in damage to, or destruction of, part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

Safety Earth Ground

This is a safety class I product and is provided with a protective earthing terminal. An uninterrupted safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

Before Applying Power

Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual, and that the correct primary fuse rating is installed.

If this product is to be energized via an auto-transformer (for voltage reduction), make sure the common terminal is connected to the earth terminal of the main power source.

Servicing

Any servicing, adjustment, maintenance or repair of this product must be performed only by service-trained personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when the product is disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow) are to be used for replacement.

Assembly Access

NOTE

Disassembly instructions are written as if viewing the disc device from the front. That is, right = the viewer's right; left = the viewer's left; "front" = the front of the device; and "rear" = the rear of the device.

Assembly Designations

The following assembly numbers are used to designate cable connections:

A1	Winchester Controller PCA (09133-69508)
A2	Winchester Drive
A3	Winchester Drive Electronics PCA
A4	Power Supply
A5	3 1/2-inch Drive
A6	3 1/2-inch Drive Controller, Upper Board (09133-69506)
A7	3 1/2-inch Drive Controller, Lower Board (09133-69507)

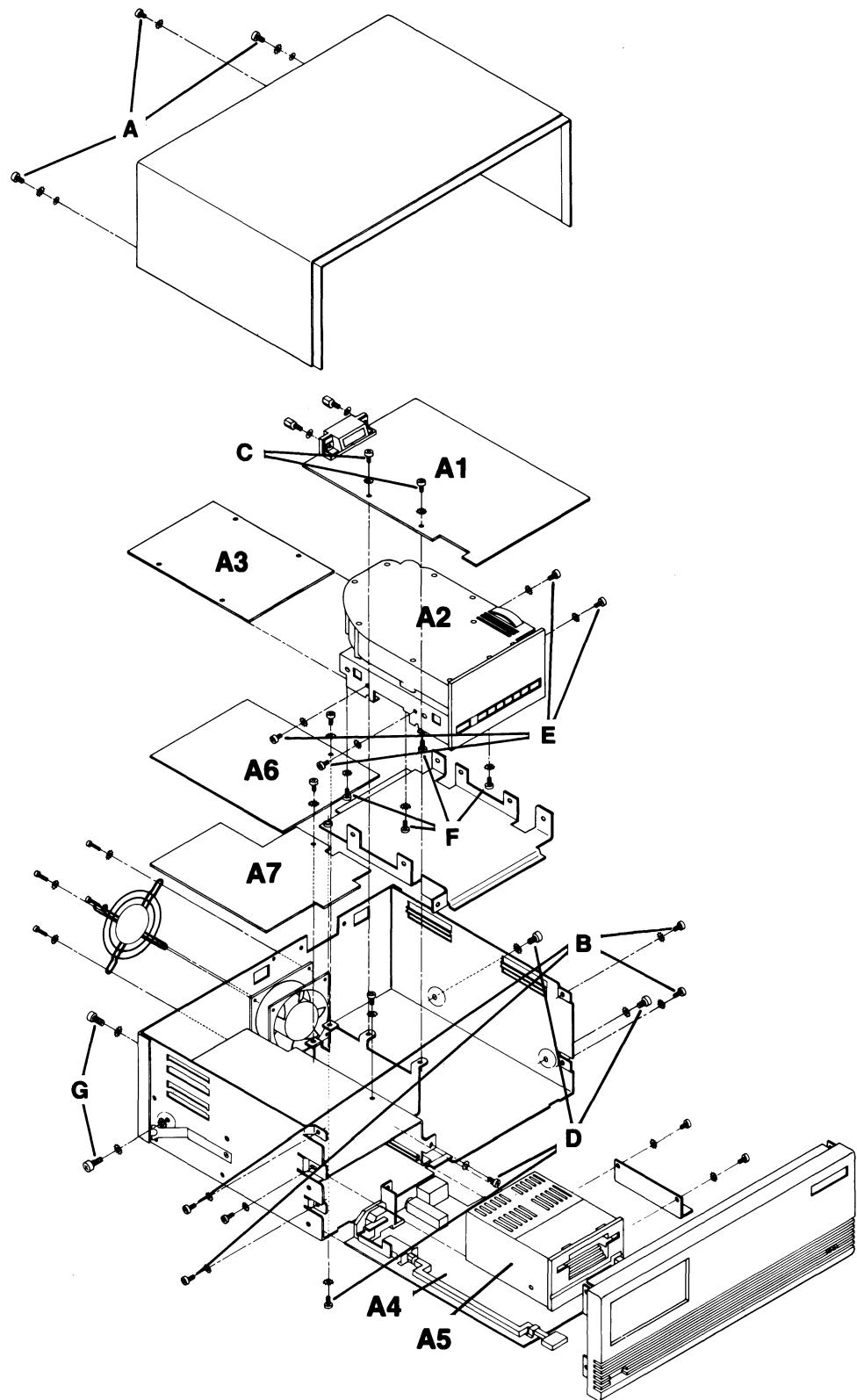


Figure 2-1. The 9133V/XV Exploded View

Top Cover Assembly Removal

The Top Cover Assembly consists of an injection molded plastic shroud and a steel shield shroud. To remove the assembly, remove three screws on the rear of the disc memory (marked "A" in Figure 2-1.)

DO NOT LIFT THE COVER. Instead, slide the cover assembly to the rear until it is clear of the front panel and the HP-IB connector nuts. Then lift the cover assembly from the disc memory. See Figure 2-2.

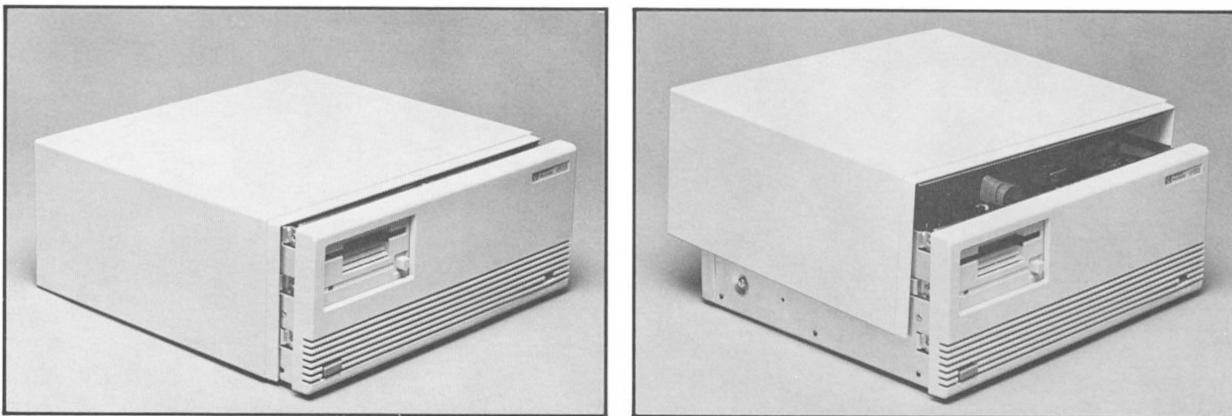


Figure 2-2. Top Cover Assembly Removal

Front Panel Removal

The Front Panel Assembly must be removed for access to the Winchester drive. The controller board (09133-69508) can be removed without removing the Front Panel Assembly.

The Front Panel assembly consists of an injection molded plastic panel and a steel shield.

Remove the assembly as follows:

1. Remove the four-pin LED cable plug from A1J8. See Figure 2-3.
2. Remove four screws marked "B", two on each side of the disc memory.
3. Slide the panel to the front, clear of the disc memory.

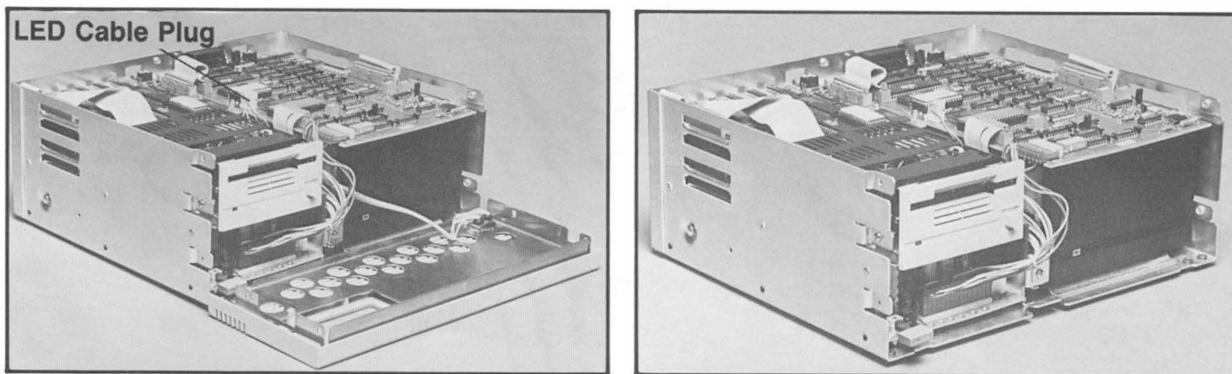


Figure 2-3. Front Panel Removal

Controller PCA Removal

The controller PCA (09133-69508) in the disc memory is located above the Winchester drive. The board can be removed without removing the drive.

To remove the board proceed as follows:

1. Detach cables from A1J1, A1J7, A1J8, A1J9, and A1J10.
2. Remove two mounting screws (labelled "C" in Figure 2-1) from the left side of the board.
3. Remove the HP-IB connector nuts from the rear of the chassis.
4. Lift the board clear of the chassis.

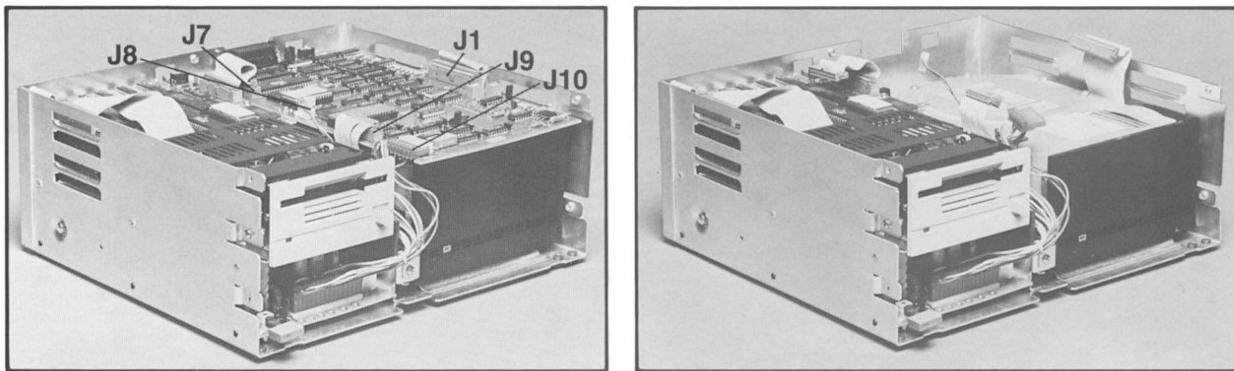


Figure 2-4. Controller PCA Removal

During reassembly, note that the board slides into lanced board guides on the right side of the chassis.

Drive Assembly Removal

The Winchester Drive Assembly consists of the Winchester Drive, the Drive Electronics PCA, and the Winchester Mounting Bracket. To remove the Winchester Drive Assembly, it is necessary first to remove the Top Cover Assembly, the Front Panel Assembly, and the Controller Board PCA.

With this done, proceed as follows:

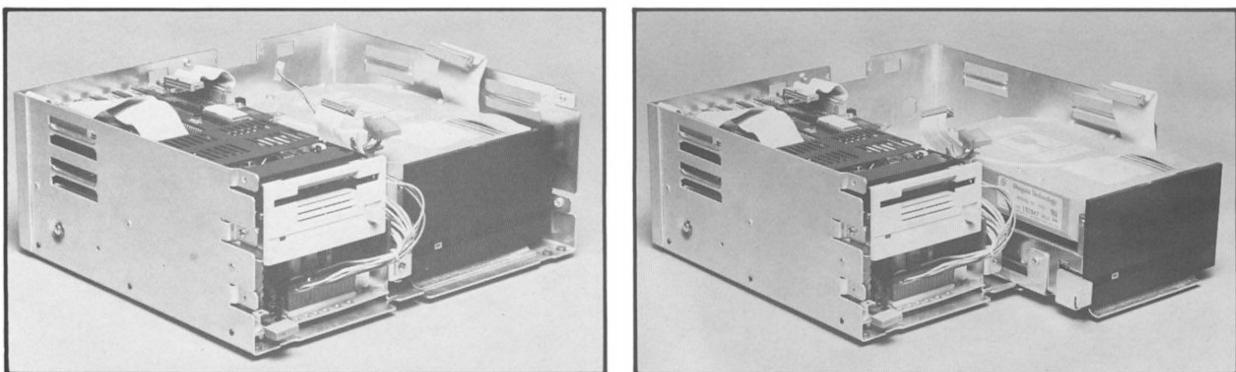


Figure 2-5. Drive Assembly Removal

1. Remove four mounting screws marked "D" on Figure 2-1. Two screws are located on the lower right side of the chassis, an other on the front mounting tab, and the fourth from the bottom.
2. Slide the drive assembly forward and remove the power cable assembly plug from A3J3 (Drive Electronics Board).
3. Slide the Drive Assembly out of the front of the chassis.

Drive Mounting Bracket Removal

1. Remove the Drive Assembly from the chassis as described above.
2. Remove the read/write cable and the disc controller cable from the rear of the Drive Assembly
3. Turn the Drive Assembly upside down. Remove four screws (marked "E" in Figure 2-1) from the sides of the assembly; lift off the mounting bracket.

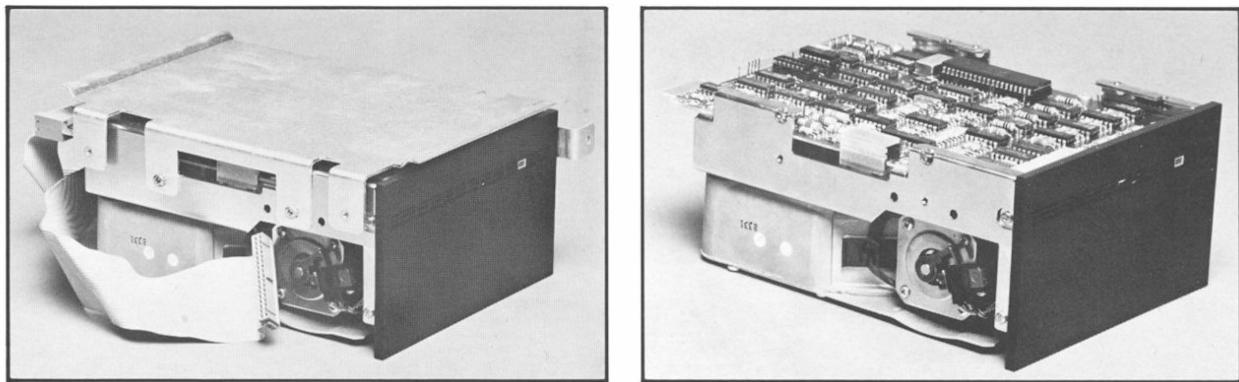


Figure 2-6. Drive Mounting Bracket Removal

Drive Electronics PCA Removal

1. Remove the Drive Assembly and Drive Mounting Bracket as described above.
2. With the Drive still upside down, remove plugs P4, P5, P6, P7, and P8 from A3J4, A3J5, A3J6, A3J7, and A3J8. (Because these plugs are labelled only with stickered labels, notation of the wire codes and pins to which each wire in P6, P7, and P8 is connected is advisable.)

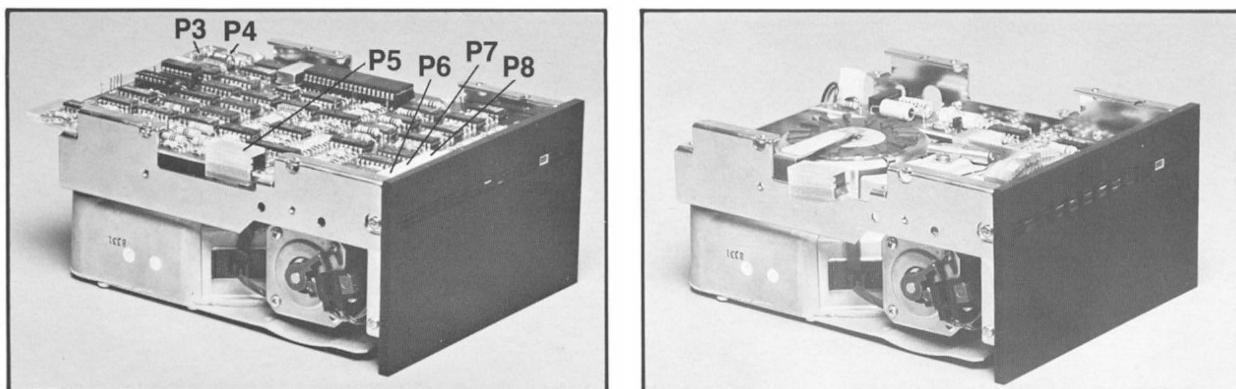


Figure 2-7. Drive Electronics PCA Removal

3. Remove four screws labelled "F" in Figure 2-1. Carefully slide the board to the rear of the box frame and clear of the Drive Assembly. See Figure 2-7.

Replaceable Assemblies

The Winchester Drive and the Drive Electronics PCA are replaceable assemblies. The Mounting Bracket is not a replaceable assembly. If a defective assembly is to be returned for replacement, only the specific defective assembly should be returned. See Figure 2-8.

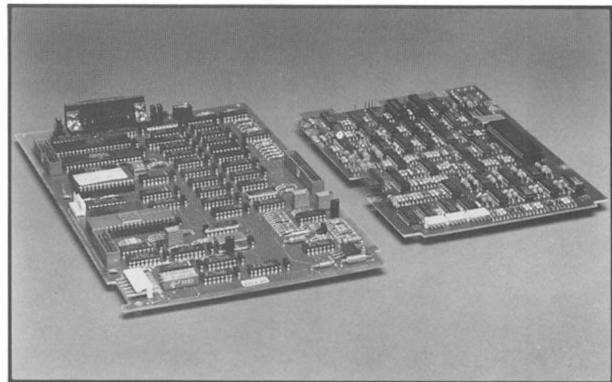
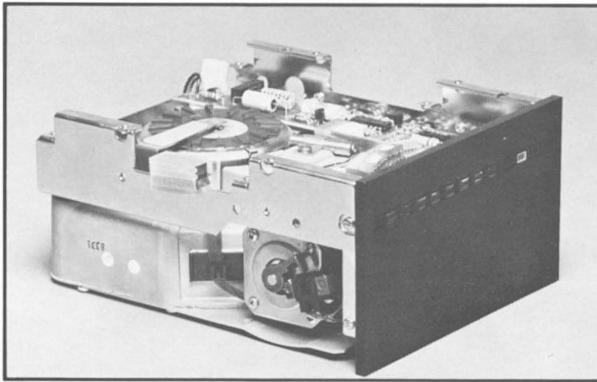


Figure 2-8. Replaceable Assemblies

Power Supply Removal

To remove the Power Supply, it is necessary first to remove the Top Cover Assembly and the Front Panel Assembly. With this done, proceed as follows:

1. Remove two screws marked "G" in Figure 2-1. One is on the left side of the chassis, and the other is on the rear of the chassis.
2. Disconnect the power harness connector from the front of the power supply assembly A4J2. Slide the power supply forward and pull it out of the chassis.
3. The Power Supply Assembly is a replaceable assembly. When replacing a defective assembly, do not return the power guard. See Figure 2-9.

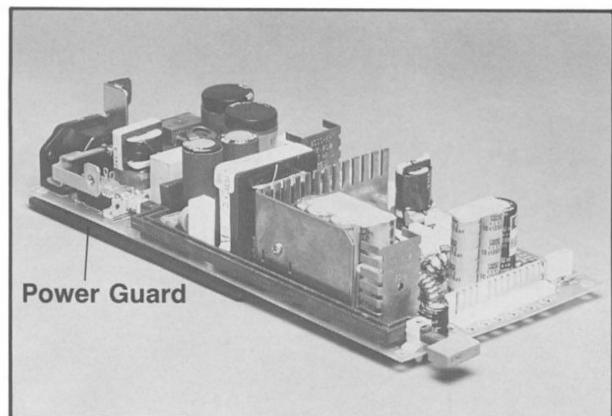
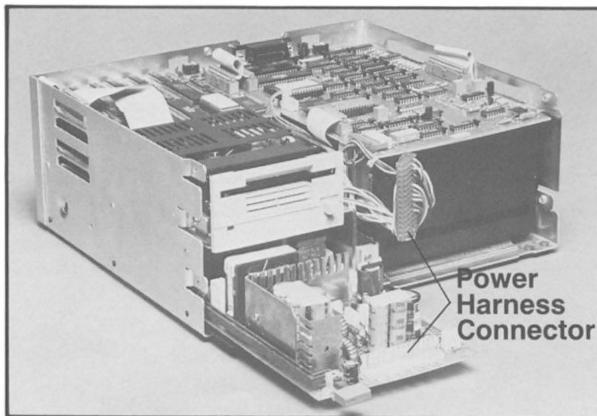


Figure 2-9. Power Supply Removal

Chapter 3

Replaceable Parts

- **Introduction**
- **Replaceable Parts List**

Introduction

This chapter contains the replaceable parts list for the Winchester drive, the power supply, and the case assembly.

The check digit shown in the CD column is required when ordering a part from HP. Please include this number with your order.

The Winchester disc drive, its controller and drive electronics PCAs are "exchange only" assemblies and are not broken down to any lower level.

The various products are listed with a "Usage Code" assigned to each product. The usage code shows how many, and on what product, the parts are used. The parts which do not have a usage code, are used on all of these products.

Replaceable Parts List

Level	Reference Designator	HP Part No.	CD	Description	Usage Code
	9133V			Disc Memory	A
	9133XV			Disc Memory	B
	9134XV			Disc Memory	C
Case Parts					
1		0403-0427	1	BUMPER FOOT	
1		0510-1237	0	FASTNER	
1		07940-00026	7	FAN GUARD	
1		07940-40048	7	FRONT PANEL-9134	C
1		07940-40062	5	SHAFT SWITCH	
1		09121-48301	4	BUTTON, PUSH	
1		09121-48303	6	FOOT-MOLDED	
1		09133-00602	2	FRT SHIELD-33	
1		09133-00604	4	FRT SHIELD-9134	C
1		09133-01202	0	WIN. BRKT	
1		09133-20101	8	CHASSIS - 9133	A,B
1		09133-40201	1	FRT PNL- 9133	A,B
1		09144-45404	9	GUARD, POWER	
Electrical Assemblies					
1		09133-42501	8	LIGHT PIPE	
1		09133-61601	9	POWER HARNESS	
1		09133-61602	0	DISC CTLR CABLE	
1		09133-61603	1	DISC R/W CABLE	
1		09133-61604	2	HPIB CABLE	A,B

Replaceable Parts List

Level	Reference Designator	HP Part No.	CD	Description	Usage Code
1		09133-61606	4	LED/PWR CABLE	
1		09133-68501	2	FAN ASSY	
1		09133-84304	7	FRT PNL LABEL-33	
1		09133-88865	3	SHIELD/SHROUD ASSY	A,B
1	5061-3144		4	POWER SUPPLY	
1		8120-1378	1	CABLE-POWER	
Fuses					
1		2110-0003	0	FUSE-3AMPS NB	
1		2110-0002	9	FUSE 2A 250V	
Exchange Assemblies					
1	A2	09133-69100	9	5 MBYTE DRIVE	A
1	A3	09133-69103	2	5 MBYTE ELEC BD	A
1	A2	09133-69104	3	15 MBYTE DRIVE	B,C
1	A3	09133-69105	4	15 MBYTE ELEC BD	B,C
1	A1	09133-69508	1	HRD DISC CTLR BD	
.2	CR1	0122-0070	4	DIO-VVC IN5456A	
.2	C4,5,8,19	0160-4571	8	C-F .1UF + 80	
.2	C38,48	0160-4788	9	C-F 18PF 5% 100V	
.2	C2,42	0160-4803	9	C-F 68PF 5% 100V	
.2	C1,11	0160-4805	1	C-F 47PF 5% 100V	
.2	C44	0160-4807	3	C-F 33PF 5% 100V	
.2	C3,6,10	0160-4810	8	C-F 330PF 5%	
.2	C9	0160-4832	4	C-F .01UF 10%	
.2	C12-18,22-37,39-41, C43,45-47,49-53	0160-5332	1	C-F .1UF 20% 50V	
.2	C21	0180-0197	8	C-F 21UF 20V	
.2	C7,20	0180-1746	5	C-F 15UF 20V	
.2	Y1	0410-0779	1	CRYSTAL	
.2	R1,2,4-6,8,10,11,38,40 R50-55,58	0683-1025	9	R-F 1K 5% .25W	
.2	R9	0683-2215	1	R-F 220 OHM .05	
.2	R29,35	0698-3132	4	R-F 261 OHM .01	
.2	R23,24	0698-4451	2	R-F 340 OHM .01	
.2	R19	0698-4471	6	R-F 7.15K 1%	
.2	R32,34	0757-0284	7	R-F 150 OHM 1%	
.2	R16,21,22,57	0757-0401	0	R-F 100 OHM .01	
.2	R14,25-27,41,56	0757-0411	2	R-F 332 OHM 1%	
.2	R31,33	0757-0413	4	R-F 392 OHM 1%	
.2	R28,37,42,43,47	0757-0416	7	R-F 511 OHM .01	
.2	R17	0757-0417	8	R-F 562 OHM 1%	
.2	R30,36	0757-0424	7	R-F 1.1K 1%	
.2	R18,45,46	0757-0437	2	R-F 4.75K 1%	
.2	R3,13,39,48,49	0757-0442	9	R-F 10.0K 1/8W	
.2	R7	0757-0444	1	R-F 12.1K .01	
.2	R15	0757-0465	6	R-F 100K .01	
.2	U42	1200-0654	7	SKT-IC 40-CIBT	
.2	U39	1200-0861	8	SKT-IC 28-CONT	
.2	J2,5	1251-5380	3	CONN 2 PIN M	
.2	J10	1251-5533	8	CONN-POST-TP-HDR	
.2	J3,6	1251-6515	8	CONN-POST-TP-HDR	
.2	P4	1251-7651	5	CONN 24-PIN M	
.2	J8	1251-7967	6	CONN-POST-TP-HDR	

Replaceable Parts List

Level	Reference Designator	HP Part No.	CD	Description	Usage Code
.2	J9	1251-8681	3	20 PIN CONNECTOR	
.2	J7	1251-8682	4	CONNECTOR,26 PIN	
.2	J1	1251-8683	5	CONNECTOR,34 PIN	
.2		1258-0141	8	JUMPER-REM	
.2	RP1	1810-0182	9	NTWK-R24XMULTDIP	
.2	RP2,3	1810-0235	3	NTWK-R15X21KDIP	
.2	U26	1813-0067	5	XTAL-CLK-OSC	
.2	U46	1813-0346	3	DLAY LINE 60NSEC	
.2	U41	1818-1178	1	IC MK 4118AN-3	
.2	U38	1818-1751	6	IC MCM68B10P	
.2	U13	1820-0471	0	IC SN7406N	
.2	U2,14,23	1820-0621	2	TTL BUFF 7438N	
.2	U15	1820-0681	4	IC SN74SOON	
.2	U1	1820-0683	6	IC SN74S04N	
.2	U12,33	1820-0693	8	IC SN74S74	
.2	U29	1820-1112	8	IC 74LS74	
.2	U34	1820-1158	2	IC SN74S51N	
.2	U27	1820-1191	3	IC SN74S175	
.2	U30,45	1820-1195	7	IC 74LS175	
.2	U18	1820-1196	8	IC SN74LS174N	
.2	U11,20	1820-1197	9	IC 74LS00	
.2	U16,21	1820-1199	1	IC 74LS04	
.2	U22	1820-1202	7	IC 74LS10N	
.2	U8	1820-1206	1	IC SN74LS27N	
.2	U19,24	1820-1216	3	IC SN74LS138	
.2	U6	1820-1285	6	IC SN74LS54N	
.2	U5	1820-1367	5	IC SN74S08N	
.2	U25	1820-1416	5	TTL TRGR 74LS14N	
.2	U9	1820-1423	4	TTL SN74LS123N	
.2	U7	1820-1425	6	IC SN74LS132N	
.2	U10	1820-1568	8	IC SN74LS125AN	
.2	U32	1820-1782	8	IC 26S02	
.2	U17	1820-2024	3	IC SN74LS244	
.2	U40	1820-2075	4	IC SN74LS245N	
.2	U31	1820-2096	9	IC SN74LS393N	
.2	U44	1820-2203	0	IC AM26LS32PC	
.2	U28	1820-2483	8	IC SN75161N	
.2	U35	1820-2485	0	IC SN75160N	
.2	U36	1820-2549	7	IC 8291AP	
.2	U37	1820-2624	9	IC 68B09	
.2	U43	1820-2749	9	IC AM26LS31PC	
.2	U4	1826-0445	0	IC UA7905UC	
.2	Q1	1854-0215	1	XSTR-2N3904	
.2	U3	1858-0086	2	XSTR ARRAY	
.2	CR2,3	1901-1098	1	DIO-1N4150	
.2	CR4	1990-0450	4	LED-LMP	
.2	R20	2100-3863	5	RES-VAR 200 10%	
.2	R12,44	2100-3874	8	RES-VAR 5K 10%	
.2		2200-0521	8	SCR-MACH 4-40	
.2		2260-0002	6	NUT-HEX 4-40	
.2		2200-0107	6	SCR-MACH 4-40	
.2	SW1	3101-2264	1	SW-RKR 4-1A	
.2	L1,2	9100-3913	3	IDCTR 3.3UH 5%	
.2	U39	09133-15520	4	COYOTE E PROM	
.2	U42	1820-3168	8	IC WD1010	

Chapter 4

Technical Specifications

Controls and Indicators

- HP 9133V/XV Disc Memory
- HP 9134XV Disc Memory

HP 9133V/XV Disc Memories

The HP 9133V and the 9133XV Disc Memories (Figure 4-1) are random access data storage devices; they each contain a 5 1/4-inch Winchester disc and a 3 1/2 inch flexible disc drive.

The 9133V is available with the Winchester disc configured as a single volume with a formatted capacity of 4.8 Mbytes, or as four volumes with a formatted capacity of 1.15 Mbytes per volume as Option 004. The four volume configuration emulates an HP 9895A 8-inch flexible disc drive master with three slave drives, and can be operated by any computer which supports the 9895A.

The 9133XV is available only with the Winchester disc configured as a single volume with a formatted capacity of 14.5Mbytes.

The 3 1/2-inch flexible disc drive in the 9133V and 9133XV emulates an HP 9121S flexible disc drive and can be operated by any computer which supports the 9121S or 82902M flexible disc drives.

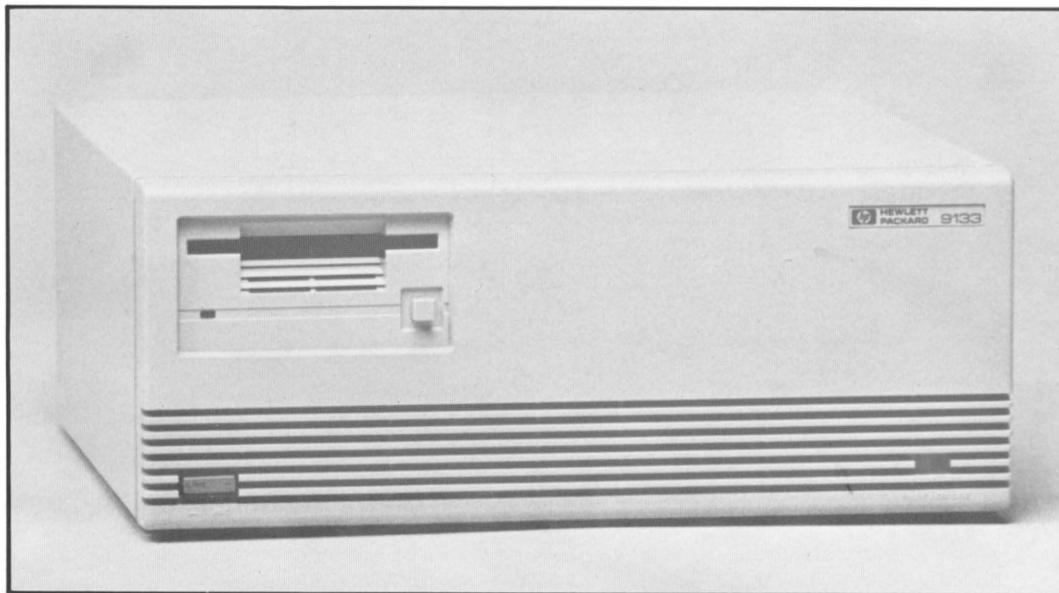


Figure 4-1. HP 9133V/XV Disc Memory

Technical Specifications

Listed below are the physical, electrical, and environmental specifications for the HP 9133V/XV disc memories.

Unit Specifications

Power Requirements:	
Source (selected by rear panel switch)	90 to 125Vac 180 to 250Vac
Line Frequency	48 to 66 Hz
Power Consumption(max)	125W
Environmental Range:	
Operating Temperature	10° to 40° C (50° to 104° F)
Storage Temperature	-40° to 60° C (-40° to 140° F)
Operating Humidity (non-condensing, 25° C max wet bulb temperature)	20% to 80%
Storage Humidity (non-condensing)	5% to 95%
Operating Altitude	0 to 4572m (0 to 15000 ft)
Storage Altitude	-304 to 1524m (-1000 to 50000 ft)
Size/Weight:	
Height	125mm (4.9 in)
Width	325mm (12.8 in)
Depth	285mm (11.2 in)
Net Weight	10kg (22 lb)
Shipping Weight	16.8kg (37 lb)

Drive Specifications

Characteristics	5 Mbyte Winchester 9133V	15 Mbyte Winchester 9133XV
Formatted Capacity:		
Bytes per Unit	4.8M (Opt. 004: 4.6M)	14.5M
Bytes per Sector	256	256
Sectors per Track	31 (Opt. 004: 30)	31
Tracks per Surface	305	305
Surfaces per drive	2	6
Tracks per inch	345	345
Max Sustained Transfer Rate*		
Average Access Time	50kBytes/sec 85msec	50kBytes/sec 85msec
Rotational Speed	3600rpm	3600rpm

*Mainframe dependent

NOTE

There is no write protect capability on the Winchester drive. Caution must be used to avoid writing over data stored on the Winchester disc.

Controls and Indicators

The location of all controls and indicators on the disc memory are shown in Figure 4-2. Front panel controls and indicators are a primary power LINE switch, a FAULT indicator, an ON LINE indicator for the Winchester disc drive, and a disc access indicator for the 3 1/2-inch flexible disc drive. Rear panel controls and indicators are the DISC ADDRESS switches, the VOLTAGE SELECT switch, the TEST switch adjacent to the FLEXIBLE DISC ADDRESS switches, and the selftest indicators for the flexible disc and the Winchester disc.

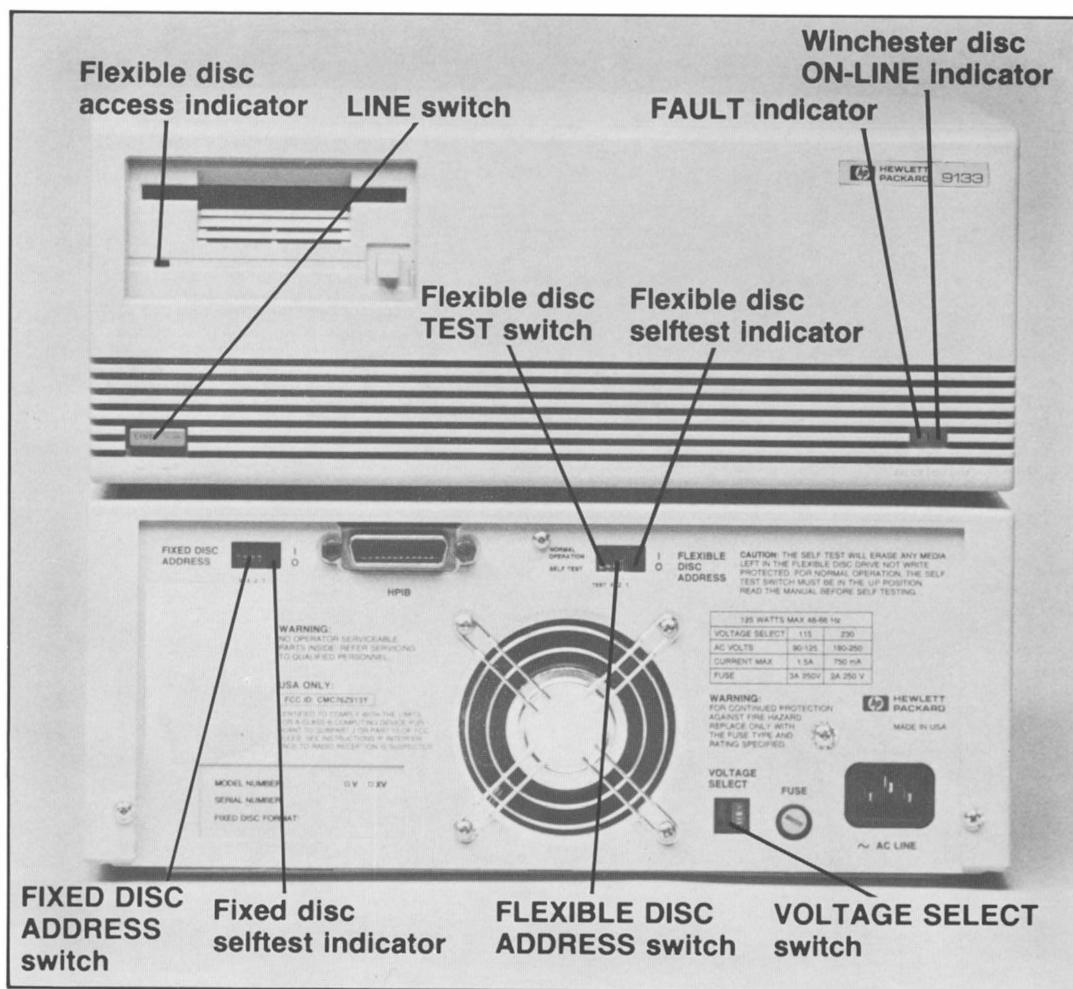


Figure 4-2. Controls and Indicators

The LINE switch controls the application of AC power to the disc memory. It is depressed to apply power, and depressed again to remove power.

The FAULT indicator is on whenever the selftest indicator of either disc drive is on. It is normally on during the power-up selftest, selftest initiated by a command from the computer, or when a fault exists in either disc drive. It also indicates the results of the user-confidence selftest initiated by the TEST switch on the rear panel of the disc memory. If the FAULT indicator remains on or flashing for more than one minute after power-up or initiation of a selftest, a fault has been detected in one of the disc drives. (The fault light indication can be followed up by examining the selftest indicator LEDs on the rear of the instrument and consulting the "Selftest Results" section of the Appendix.)

The ON LINE indicator is on whenever the Winchester disc is accessed for data storage or retrieval, and momentarily when the drive is powered up.

The flexible disc access indicator is on whenever the flexible disc is accessed for data storage or retrieval and momentarily when the drive is powered up.

The selftest indicators for the flexible disc drive and the Winchester disc drive are visible through the DISC ADDRESS cut-outs on the rear panel and can be checked to determine which drive is defective if the FAULT indicator is on or flashing.

HP 9134XV Disc Memory

The HP 9134XV Disc Memory (Figure 4-3) is a random access data storage device. The disc memory contains a 5 1/4-inch Winchester disc drive configured as a single volume with a formatted capacity of 14.5Mbytes.

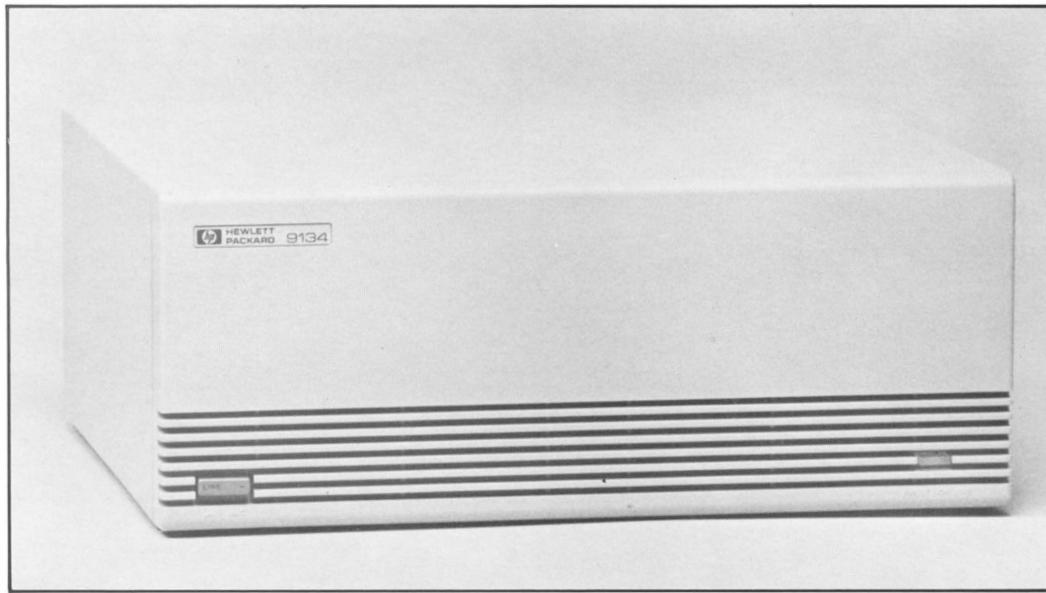


Figure 4-3. HP 9134XV Disc Memory

Technical Specifications

Listed below are the physical, electrical, and environmental specifications for the HP 9134XV disc memory.

Unit Specifications

Power Requirements:	
Source (selected by rear panel switch)	90 to 125Vac 180 to 250Vac
Line Frequency	48 to 66 Hz
Power Consumption(max)	125W
Environmental Range:	
Operating Temperature	10° to 40° C (50° to 104° F)
Storage Temperature	-40° to 60° C (-40° to 140° F)
Operating Humidity (non-condensing, 25° C max wet bulb temperature)	8% to 80%
Storage Humidity (non-condensing)	5% to 95%
Operating Altitude	0 to 4572m (0 to 15000 ft)
Storage Altitude	-304 to 1524m (-1000 to 50000 ft)
Size/Weight:	
Height	125mm (4.9 in)
Width	325mm (12.8 in)
Depth	285mm (11.2 in)
Net Weight	8.64kg (22 lb)
Shipping Weight	15.5kg (37 lb)

Drive Specifications

Characteristics	15 Mbyte Winchester 9134XV
Formatted Capacity:	
Bytes per Unit	14.5M
Bytes per Sector	256
Sectors per Track	31
Tracks per Surface	305
Surfaces per drive	6
Tracks per inch	345
Max Sustained	
Transfer Rate*	50KBytes/sec
Average Access Time	85msec
Rotational Speed	3600rpm

*Mainframe dependent

NOTE

There is no write protect capability on the Winchester drive. Caution must be used to avoid writing over data stored on the Winchester disc.

Controls and Indicators

The location of all controls and indicators on the disc memory are shown in Figure 4-4. Front panel controls and indicators are a primary power LINE switch, a FAULT indicator, and an ON LINE indicator. Rear panel controls and indicators are the FIXED DISC ADDRESS switch, the selftest indicator LED, and the VOLTAGE SELECT switch.

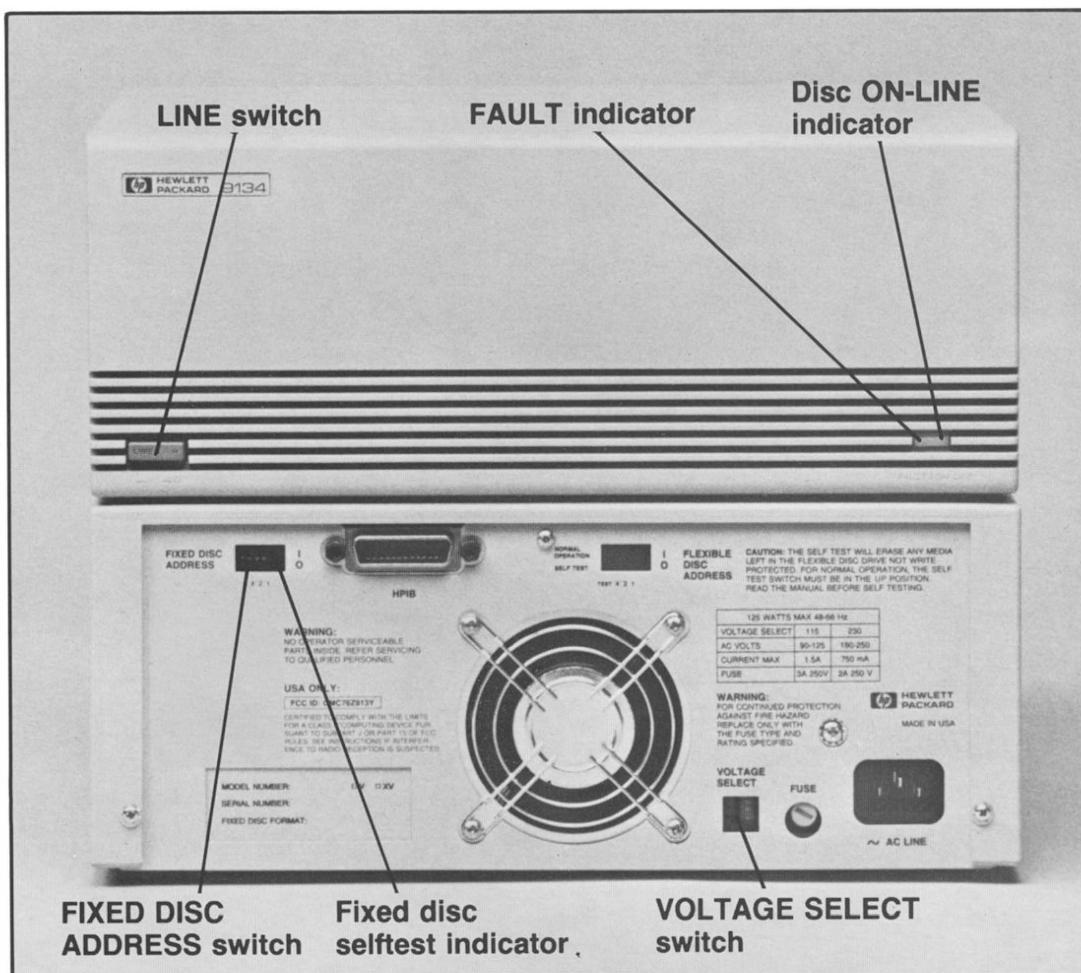


Figure 4-4. Controls and Indicators

The LINE switch controls the application of AC power to the disc memory. It is depressed to apply power, and depressed again to remove power.

The FAULT indicator is on whenever the selftest indicator is on. It is normally on during the power-up selftest, selftest initiated by a command from the computer, or when a fault exists in the Winchester disc drive. If the fault indicator remains on or flashing for more than one minute after power-up or initiation of a selftest, a fault has been detected in the disc drive. (The fault light indication can be followed up by consulting the "Selftest Results" section of the Appendix.)

The ON LINE indicator is on whenever the Winchester disc is accessed for data storage or retrieval, and momentarily when the drive is powered up.

The selftest indicator for the Winchester disc drive is visible through the device address cut-out on the rear panel. Its response is identical to that of the FAULT indicator.

Chapter 5

Installation and Initial Checkout

- Introduction
- Equipment Supplied
- Configuring Power
- Interfacing to Your System
- Winchester Drive Operation

Introduction

This chapter contains procedures for the installation, initial power-on, and initial checkout of the HP 9134XV and initial power-on and checkout procedures for the Winchester drive in the HP 9133V/XV. For information on installation and initial checkout of the 3 1/2-inch drive in the HP 9133V/XV, see HP's 3 1/2-Inch Flexible Disc Drive Service Documentation, Part No. 09121-90030.

Equipment Supplied

Description	Quantity	HP Part Number		
Power Cable	1	Dependent on location		
User's Manual	1	09133-90010		
Spare Fuse	1	90 to 125VAC or 180 to 250VAC	3 Amp 2110-0003	2 Amp 2110-0002

Configuring Power

Setting the VOLTAGE SELECT Switch

The VOLTAGE SELECT switch on the rear panel was set to the line voltage for the original destination when shipped from the factory. Verify that the setting is correct for local line voltage before connecting to the power source.

Figure 5-1 shows the setting of the VOLTAGE SELECT switch for the two ranges of line voltage.

WARNING

ALWAYS TURN OFF THE AC POWER SWITCH BEFORE
CHANGING THE VOLTAGE SELECT SWITCHES.

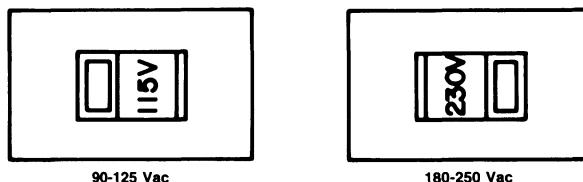


Figure 5-1. Line VOLTAGE SELECT Switch

Fuses

A different fuse is required for each voltage range (90-120VAC and 180-250VAC). The correct fuse for the original destination is installed and a spare fuse for that destination is included before shipment from the factory.

Table 5-1 gives the correct fuse ratings and fuse part numbers for each voltage range.

Table 5-1. Fuses

Switch Setting	Voltage Range	Fuse Rating	HP Part Number
115V	90-125VAC	3A 250 VAC Normal Blow	2110-0003
230V	180-250VAC	2A 250 VAC-Normal Blow	2110-0002

WARNING

ALWAYS DISCONNECT THE DISC MEMORY FROM THE AC SOURCE BEFORE CHANGING FUSES.

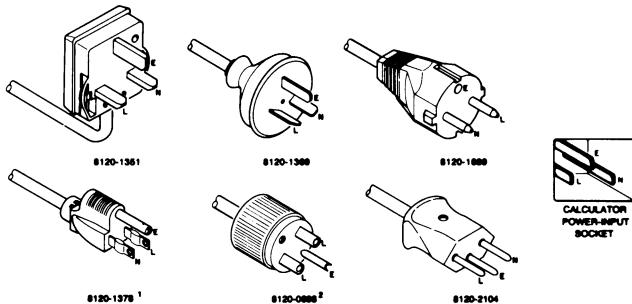
Power Cords

Power cords supplied by HP (See Figure 5-2) have polarities matched to the power input socket on the equipment. They are marked as follows:

L = Line or active conductor (also called "live" or "hot")

N = Neutral or identified conductor

E = Earth or safety ground



¹UL and CSA approved for use in the United States of America and Canada with equipment set for either 100 or 120 Vac operation.

²UL and CSA approved for use in the United States of America and Canada with equipment set for either 200 or 240 Vac operation.

Figure 5-2. Available Power Cords

WARNING

IF IT IS NECESSARY TO REPLACE THE POWER CORD, THE REPLACEMENT CORD MUST HAVE THE SAME POLARITY AS THE ORIGINAL. OTHERWISE, A SAFETY HAZARD MIGHT EXIST SHOULD AN INTERNAL FAILURE OCCUR.

The correct power cord for the original destination is packaged with the equipment.

Interfacing to Your System

Selecting the Device Address

Before connecting the disc memory to the computer, and before powering-up, set the device address.

Each device in an HP-IB system must be set to a unique device address. The two drives in an HP 9133V/XV are, for this purpose, considered separate devices; hence a device address switch is provided for each drive. See Figure 5-3 for switch locations.

A device address switch can be set to any one of eight device addresses ranging from decimal 0 through 7 by proper positioning of the four switch-segments within the device address switch. Table 5-2 lists the switch-segment positions for the eight device addresses.

Prior to setting the device address switches, turn the disc memory AC line switch OFF.

Table 5-2. Switch-Segment Positions

Address	*TEST	4	2	1	
0	**	DOWN	DOWN	DOWN	(Factory setting for Winchester)
1	**	DOWN	DOWN	UP	
2	**	DOWN	UP	DOWN	(Factory setting for flexible disc)
3	**	DOWN	UP	UP	
4	**	UP	DOWN	DOWN	
5	**	UP	DOWN	UP	
6	**	UP	UP	DOWN	
7	**	UP	UP	UP	

* Refer to "Selftest Results" in the Appendix for test information.

** The TEST switch-segment on the flexible disc device address switch must be UP for normal operation. The position of this switch-segment on the fixed disc device address switch does not affect operation.

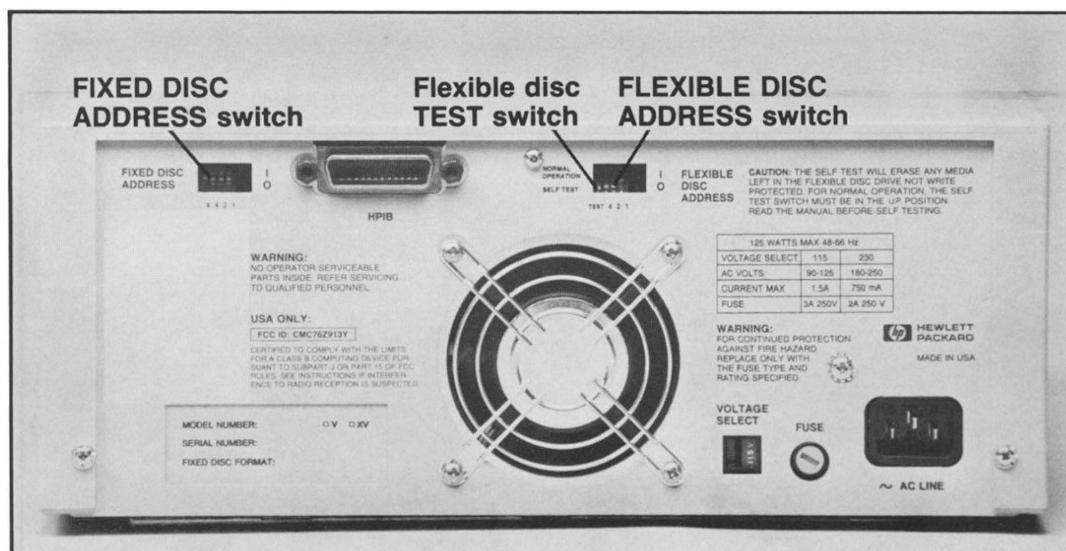


Figure 5-3. Device Address Switches

NOTE

If the TEST switch-segment on the flexible disc device address switch is in the down position, the computer will not be able to communicate with the disc drive and will probably indicate that the disc drive is not present.

HP-IB Cables

Refer to Figure 5-4 for a list of the HP-IB cables used with the computers.

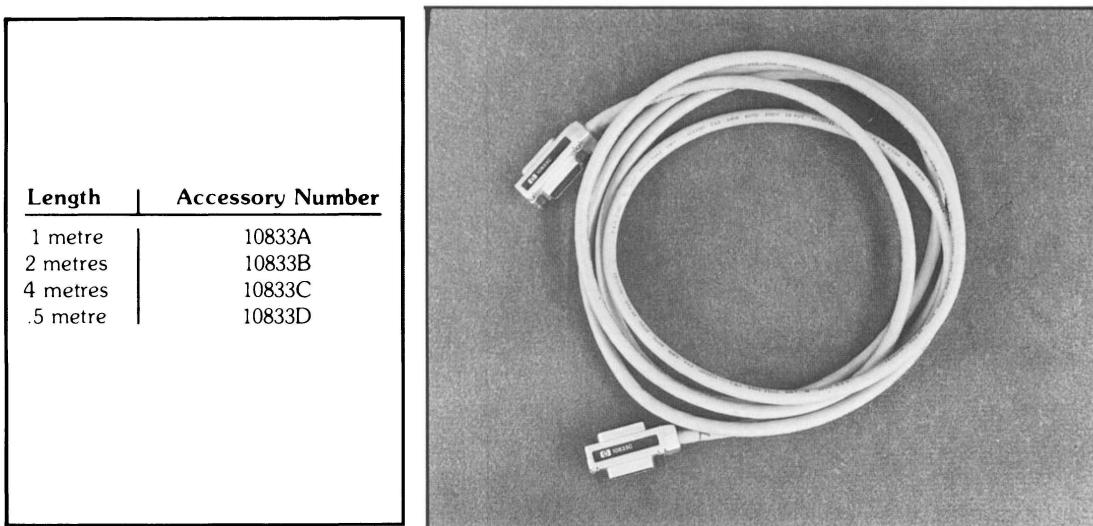


Figure 5-4. HP-IB Interface Cables

CAUTION

ALWAYS SET THE AC LINE SWITCHES TO "OFF" (0) FOR THE COMPUTER AND THE DISC DRIVES WHEN INSERTING OR REMOVING THE INTERFACE CABLES. USE ONLY CABLES DESIGNED BY HEWLETT-PACKARD FOR YOUR EQUIPMENT. FAILURE TO DO SO COULD DAMAGE THE DISC DRIVE OR THE CONTROLLING COMPUTER.

HP-IB Interface Restrictions

1. All the AC line switches must be turned "OFF" when connecting (and disconnecting) devices to your system.
2. The total length of cable permitted in one bus system must be less than or equal to two metres times the number of devices connected together (the interface card counts as one device; the 9133 counts as two devices.)
3. The total length of the cable must not exceed 20 metres. For example, a system containing six devices can be connected together with cables that have a total length less than or equal to 12 metres (six devices x 2m/device = 12 metres). The individual lengths of cable can be distributed in any manner desired as long as the total length does not exceed the allowed maximum.

4. The maximum number of devices that can be connected together in one bus system is 15.

There are no restrictions to the way cables may be connected together; however, it is recommended that no more than four piggyback connectors be stacked together on one device. The resulting structure could exert enough force on the connector mounting to damage it.

Winchester Drive Operation

This section contains information about the initial power-on and initial checkout of the Winchester drive. Controls and indicators for the Winchester drive are discussed in Chapter 4.

NOTE

There is no write protect capability on the Winchester drive. Caution must be used to avoid writing over data stored on the Winchester disc.

Initial Power-on and Checkout

CAUTION

KEEP THE FRONT AND BACK OF THE DISC MEMORY FREE FROM OBSTRUCTIONS TO AVOID RESTRICTING THE AIR FLOW. FAILURE TO DO SO COULD CAUSE THE UNIT TO OVERHEAT AND RESULT IN DAMAGE TO THE DISC MEMORY.

Before turning the disc memory power on, check that the setting of the VOLTAGE SELECT switch on the rear panel (see above) is correct for local line voltage. If this is the first time the drive has been turned on, proceed as follows:

1. Connect the HP-IB cable from your computer to the disc memory.
2. Press the LINE switch on the front panel to the "1" position. The Power-on Selftest will automatically execute when power is applied. The FAULT indicator on the front panel will be continuously on during the test (about 30 seconds). Normally the indicator light will go off after completion of the test. Should it remain on or flashing, a fault has been detected. Refer to the "Selftest Results" section of the Appendix for further information on a selftest failure.
3. Consult computer system documentation for Winchester disc initialization procedure. The first time power is applied to a Winchester disc (or should damage to a disc be suspected), perform that initialization procedure.

The first initialization of the four volume 5 MByte Winchester should immediately initialize all four volumes in the sequence of volume 0,1,2,3. (Later initializations do not require that the complete disc be initialized at the same time or in any particular sequence.)

With the Power-on Selftest successfully completed and the disc properly initialized, the Winchester drive is ready for operation.

Appendix

Introduction

This document contains the firmware description for the 09133-69514 controller. This is the HP-designed controller assembly for the Winchester drives. The 09133-69514 controller is a replacement for several controllers which have been designed by HP OEMs for the 5 Mbyte drives. The new controller appears with the newer 5 Mbyte single drive units. See Table 1-1 "Product Configuration" in Chapter 1 of Section 2.

This description is divided into four major sections. The first describes the various configurations in which the 09133-69514 controller can operate. The 09133-69514 controller has several jumper-selectable configurations which select drives of various capacities (physical configuration), and also select the apparent format of the drive (logical configuration).

The remaining three sections describe various aspects of the command set. The "Status" section describes all of the status information available to the host and includes tables of error codes. The "Command Set" section describes the protocol used in general terms. Finally, the "Command Descriptions" section gives the details about each command individually.

Information on the MSC controllers (88134-69910, 09135-69515, and the 09135-69501) plus selftests is presented at the end of this Appendix.

Information about the 09133-69508 controller which is used in the 9133V/XV and the 9134XV disc memories is on page A-59.

Configurations

The various configurations of the 09133-69514 controller have both a physical and a logical aspect. The physical part of a configuration specifies the type of drive being controlled, and the logical part describes the way that drive is made to appear to the host.

The various logical and physical options are described in the following sections. Next, a chart summarizes the differences between the configurations. When a command description mentions the "maximum physical cylinder," for example, the actual cylinder number depends on the configuration and is defined in the chart. Finally, the address transformations required by some configurations are described.

Logical Configurations: Single and 4-Volume

Each of the logical configurations is either a 4-Volume or an Single-Volume. The two types are very similar, differing primarily in the way logical units are related to physical drives.

The 4-Volume configurations cause a 5 Mbyte drive to appear, to the host, as a four-unit 9895A flexible disc. One physical drive is addressed as if it were four separate (and smaller) drives. The physical cylinder, sector, and head numbering of the drive being used are mapped into the cylinder, sector, and head numbering that the host would expect to see for each 9895A unit. The controller also identifies itself to the host as a 9895A. This logical format allows hosts with existing 9895A drivers to use the Winchester drives without investing any time in writing new drivers. The 4-Volume is applicable only to 5 Mbyte drives since that is the capacity of a four-unit 9895A.

The Single-Volume configuration is similar to the 4-Volume in that they also use the 9895A Amigo protocol. With the Single-Volume, however, a drive does not appear to the host to be identical to the 9895A. One physical drive becomes one logical unit, with cylinder, sector, and head numbering corresponding (usually) to the physical organization of the drive. This logical format allows 9895A drivers to be easily modified to use the Single-Volume configuration, and allows drives of larger capacities to be used.

Physical Configuration: Drives Supported

Two Winchester disc drives are supported by the various 09133-69514 controller configurations. These are the 5 Mbyte Single Platter and the 10 Mbyte Dual Platter.

The major differences between these drives are the capacities and the number of platters. These differences account for most of the complications in supporting the different configurations. Other differences must also be accounted for, including maximum step rate and the cylinder at which write pre-compensation (pre-comp) begins.

The following chart details some of the differences between the drives.

	5 Mbyte Single Platter	10 Mbyte Dual Platter
Capacity (MB)	5	10
Cylinders	306	306
Platters	1	2
Heads	2	4

Only certain combinations of logical format and physical drive are possible. The following chart marks these pairs with an X.

Physical -	5 Mbyte Single Platter	10 Mbyte Dual Platter
Logical – 4-Volume	X	-
Single-Volume	X	-
Single-Volume	-	X

Each of these possible configurations is described in the following sections.

Configuration Summary

The chart on the following page summarizes the differences between the various configurations.

NOTE

“Unit” refers to a logical unit, and “drive” refers to the physical disc drive. “Units per drive” is therefore the number of logically-addressed units on a single-disc drive.

The last physical cylinder is used to perform a write/read selftest, which would destroy any user data on that cylinder. For this reason, commands that read or write are not allowed to access the last physical cylinder (selftest cylinder) so that no user data can be written there. The cylinder range allowed for reads and writes is given in the table as “logical read/write cylinders.” The full range of logical cylinders is available to other commands such as Format and Initialize.

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	5 Mbyte Single Platter	5 Mbyte Single Platter	10 Mbyte Dual Platter
Identify bytes	00H, 81H	01H, 06H	01H, 0AH
Max. number of drives supported	1	1	1
Units per drive	4	1	1
Physical cylinders per drive	0 to 305	0 to 305	0 to 305
Logical cylinders per unit	0 to 76	0 to 152	0 to 305
Logical read/write cylinders per unit	0 to 75	0 to 151	0 to 304
Selftest cylinder, logical (each unit)	76	152	305
Selftest cylinder, physical	305	304 &305	305
Physical heads	2	2	4
Logical heads	2	4	4
Physical sectors per track	32	32	32
Spare sectors per track	2	1	1
Usable sectors per track	30	31	31
Address mapping required?	yes	yes	no

Address Transformations

The host addresses a particular sector with a unit number, a cylinder number, a head number, and a sector number. This logical address for a sector is identical to the physical address only for configurations in which each disc drive corresponds to a single logical unit, and in which the logical and physical ranges for cylinder, head, and sector numbers are the same.

For the three possible configurations, however, the logical and physical appearances are different, and a logical address from the host must be transformed into a physical address before a sector is accessed. These configurations are the 4-Volume, in which a single drive becomes four logical units, and the Single-Volume configuration.

The address transformations for each of these configurations are given on the following pages.

Single Platter Address Transformations

The 5 Mbyte Single Platter hard disc used in the 4-Volume configuration has 306 cylinders, 2 heads, and 32 sectors per track. It is made to appear to be a 9895A which has four units, each having 77 cylinders, 2 heads, and 30 sectors per track. A command to access a unit, cylinder, head, and sector of the (logical) 9895A is mapped into a cylinder, head, and sector of the (physical) 5 Mbyte Single Platter drive.

Note, for each unit, the 9895A cylinder number 76 maps into the last physical cylinder of the drive (305 on the 5 Mbyte Single Platter.) These cylinders are used for the write/read selftest, and the host is prevented from using them for data.

The following formulas map logical 9895A addresses into physical addresses.

Cylinder:

5 Mbyte Single Platter cylinder = $76 * (\text{unit number}) + (9895\text{A cylinder})$.

Head:

5 Mbyte Single Platter head = 9895A head.

Sector:

No transformation is required for sector numbers.

The following table shows this mapping.

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Logical (9895A)			PHYSICAL (5 Mbyte Dual Platter)		PHYSICAL (5 Mbyte Single Platter)	
UNIT	HEAD	CYLINDER	HEAD	CYLINDER	HEAD	CYLINDER
0	0	0	0	0	0	0
0	1	0	1	0	1	0
	0	1	2	0	0	1
0	1	1	3	0	1	1
...
0	0	74	0	37	0	74
0	1	74	1	37	1	74
0	0	75	2	37	0	75
0	1	75	3	37	1	75
0	0	76	0	152	0	305
0	1	76	1	152	1	305
1	0	0	0	38	0	76
1	1	0	1	38	1	76
1	0	1	2	38	0	77
1	1	1	3	38	1	77
...
1	0	74	0	75	0	150
1	1	74	1	75	1	150
1	0	75	2	75	0	151
1	1	75	3	75	1	151
1	0	76	2	152	0	305
1	1	76	3	152	1	305
2	0	0	0	76	0	152
2	1	0	1	76	1	152
2	0	1	2	76	0	153
2	1	1	3	76	1	153
...
2	0	74	0	113	0	226
2	1	74	1	113	1	226
2	0	75	2	113	0	227
2	1	75	3	113	1	227
2	0	76	0	152	0	305
2	1	76	1	152	1	305
3	0	0	0	114	0	228
3	1	0	1	114	1	228
3	0	1	2	114	0	229
3	1	1	3	114	1	229
...
3	0	74	0	151	0	302
3	1	74	1	151	1	302
3	0	75	2	151	0	303
3	1	75	3	151	1	303
3	0	76	2	152	0	305
3	1	76	3	152	1	305

Single-Volume Single Platter Address Transformation

The Single-Volume Single Platter configuration is logically equivalent to the Single-Volume Dual Platter configuration. The Dual Platter configuration uses identical logical and physical addresses. Since the Single Platter must use the same logical addressing scheme as the Dual Platter, but has a different physical configuration, logical addresses must be mapped into physical addresses. The host driver uses the cylinder and head numbers for the 5-Mbyte Dual Platter and

09133-69514 controller maps them into the cylinder and head numbers of the 5 Mbyte Single Platter. The 5 Mbyte Dual Platter has 153 cylinders and 4 heads, and the 5 Mbyte Single Platter has 30 cylinders and 2 heads. The following shows the mapping used:

LOGICAL (5 Mbyte Dual Platter)		PHYSICAL (5 Mbyte Single Platter)	
HEAD	CYLINDER	HEAD	CYLINDER
0	0	0	0
1	0	1	0
2	0	0	1
3	0	1	1
0	1	0	2
1	1	1	2
2	1	0	3
3	1	1	3
0	2	0	4
1	2	1	4
...
0	151	0	302
1	151	1	302
2	151	0	303
3	151	1	303
0	152	0	304
1	152	1	304
2	152	0	305
3	152	1	305

The formulas for this transformation are:

- 5 Mbyte Single Platter cylinder
 - = $2 * (5 \text{ Mbyte Dual Platter cylinder})$
 - if (5 Mbyte Dual Platter) head = 0 or 1
 - = $2 * (5 \text{ Mbyte Dual Platter cylinder}) + 1$
 - if 5 Mbyte Dual Platter head = 2 or 3
- 5 Mbyte Single Platter head
 - = 0 if 5 Mbyte Dual Platter head is 0 or 2
 - = 1 if 5 Mbyte Dual Platter head is 1 or 3.

Status

The status information that the controller can return consists of two status words (Stat 1 and Stat 2), the DSJ byte, the selftest results and the target addresses. Stat 1 contains information about the last operation performed, and Stat 2 gives the status of the unit given as a parameter to the Request Status command. DSJ is an indication of controller status. The selftest results describe the results of the last selftest, contain diagnostic information, or describe the most recent hardware failure. The target addresses are not usually part of error reporting, but are included because they are information available to the host. Each of these is described in the following pages. Also, a "Power-On State" section describes the initialization of status at power-on or after a Initiate Selftest command.

STAT 1

The Stat 1 and Stat 2 words are returned in response to the Request Status and Send Status command sequence. Stat 1 gives information about the last command received, and consists of the following bits.

0	0	D	S	S	S	S	S
0	0	0	0	U	U	U	U

where: D	is set when a D bit is encountered (flags defective sector) - 09133-69514 controller does not use D bits
SSSS	is a completion code for the previous command
UUUU	is the last valid unit number given in a command (the unit to which the SSSSS code applies).

The SSSSS completion code is called S1, and may have the following possible meanings.

S1	Meaning.
00000 (00H)	Normal completion, no errors.
00001 (01H)	Illegal opcode received.
01000 (08H)	Uncorrectable data error. Disc read or verify terminated because of CRC error in data field. Data is still transmitted for the bad sector.
01001 (09H)	Sector compare error. The target sector cannot be found on the current track. Retries were attempted unsuccessfully.
01010 (0AH)	I/O program error. May be caused by an illegal secondary, or wrong number of parameters. This status can only be set if the previous S1 was zero.
10001 (11H)	D bit encountered during a write, read, read verify, or verify.
10011 (13H)	Stat 2 error. Some condition in Stat 2 prevented the drive-related operation from completing normally. These conditions include: <ol style="list-style-type: none"> 1. Drive not connected to controller (SS = 10) 2. Hardware problem detected in drive E = 1) 3. Unformatted or unknown format (TTT = 0101) 4. First status bit set (F = 1).
10111 (17H)	Unit unavailable. A command included a request for a unit number out of range.
11111 (1FH)	Drive attention. The indicated drive is requesting attention because a Seek command completed, whether normally or abnormally. Abnormal completion may be due to drive fault, out-of-bounds target (cylinder, head or sector), or target address not found.

STAT 2

The status information in Stat 2 applies to an individual unit, so these status bits are maintained for all four possible units. The Request Status command has a unit number parameter that selects the unit for which Stat 2 bits are returned.

The Stat 2 word consists of the following bits,

```
* 0 0 T T T T 0
A 0 0 E F C S S
```

with the following meanings:

Bits	Meaning
*	Stat 2 error - E or C or SS bits not zero
TTTT	0101 = Unknown format or unformatted disc 0110 = Formatted disc 0000 = No drive attached
A	Drive attention. Set when a seek completes (successfully or unsuccessfully) - Cleared when status is read
E	Drive fault - Fault condition detected in drive during command - Cleared when status is read
F	First status bit - Set at power-on and selftest completion - Cleared when status is read
C	Seek check - A seek failed because of a hardware failure, or because the target address (cylinder, head, or sector) was out of bounds - The allowed ranges for a target address depend on both the configuration and the command being executed - Cleared when status is read
SS	00=Drive is ready 10=Drive not attached (not ready within 30 sec after power-on).

DSJ

The DSJ byte is returned in response to the DSJ command. It can have the following values and meanings:

0	Last operation completed normally
1	Last operation ended abnormally - status indicates error
2	Power up or selftest completed (holdoff state).

Selftest Results

The selftest results are two bytes that describe the most recently detected hardware error. These bytes are cleared when the Read Selftest command is executed.

The format of the two bytes is:

```
E 0 U U 0 H H H
C C C C C C C C.
```

where:

E	is a bit indicating that an error was detected
UU	gives the current unit when the error was detected
HHH	gives the head selected when the error was detected
CCCCCC	is an error code describing the failure.

If the E bit is zero (no error), then both bytes are zero.

The power-on selftest is not identical to the selftest done in response to the Initiate Selftest command. Some continual selftesting is also done during normal command execution. See the Initiate Selftest command description for details on all of these modes of selftest.

The selftest error codes are described on the following pages. The MSC controllers selftests are described at the end of this section.

Selftest Error Codes

Error Code	Description of Error
HEX DECIMAL	
DCH 220	The jumper on the drive board which gives the address of the drive is set incorrectly. It should be set for 1 for a single drive.
DEH 222	The ERR bit on the 8291A was set. It is set when the 8291A tries to send a byte on the bus but there are no listeners.
DFH 223	What is written to the LED bit on the output port does not compare with what is read on the LED bit of the input port. Either the output port, input port or LED is faulty.
E0H 224	Drive 0 did not come up within 30 seconds of power on. Either no drive is attached, or the drive is faulty or there is some hardware problem with the drive ready or drive select lines.
E1H 225	WD1010 chip must be bad. What is written to the read/write registers on the WD1010 does not compare with what is read back. The chip could also be in a mode where it doesn't respond to bus activity.
E2H 226	TR000 Error. Couldn't find track zero Track zero indicator may be bad. Also check the configuration. The 5 Mbyte Dual Platter can't handle the rapid stepping pulses given the other two drives. If the

		WD1010 chip does not respond to bus activity, this error may also be seen.
E3H	227	Failed selftest. Failed the final normal read of all sectors on the self-test cylinder. At least 3 sectors either had bad CRC's or the data byte read was not 0E5H which had just been written. Could be a problem with the WD1010 chip, WD buffer, write circuitry or related hardware. 3 bad sectors is too high an error rate. You can get this error if the drive was formatted with a different configuration than you are now using.
E4H	228	The "BI" (byte in) bit of the 8291A was set for no apparent reason. This is not an error, but more of a diagnostic aid.
E5H	229	Failed selftest. After writing sequential bytes onto the disc during selftest, they are read back using a long read. The data and CRC bytes are checked. At least 5 sectors were bad. This is too high an error rate and something must be wrong.
E6H	230	The 1K buffer RAM used for data (WD_BUFFER) failed selftest.
E7H	231	There is only 1 spare sector available in the configuration chosen and the next worst sector is too bad to allow the continued use of the drive. In other words, there are two bad sectors and we can only spare one of them.

The following group are errors the WD1010 chip returns when it can't execute a command (E8H through EFH).

E8H	232	Aborted command, Drive not ready, Seek not complete
E9H	233	Aborted command, Drive not ready
EAH	234	Aborted command, Drive not ready, Write fault, and Seek not complete
EBH	235	Aborted command, Drive not ready, Write fault
ECH	236	Aborted command, Seek not complete
EDH	237	Aborted command with no error recorded
EEH	238	Aborted command, Write fault, Seek not complete
EFH	239	Aborted command, Write fault (Could be the wrong configuration jumper setting, controller expects the drive to have more heads.)
F0H	240	Timeout waiting for WD1010 to be "not busy, ready, and seek complete". WD1010 chip, drive or associated hardware must be defective.
F1H	241	This error is set if more than 1 error bit is set in the WD1010 error register or an unidentified error bit was set. For example, if the ID NOT FOUND error bit was set as well as the D BIT, only the former is reported and this selftest error is set to say that more than an ID NOT FOUND error occurred.
F2H	242	The number of hard errors has exceeded the number of spares on the track. Too many errors to format a track.

F3H 243	Failed selftest. During selftest all sectors on the selftest cylinder are written. We were unable to write at least 3 sectors. This is too high an error rate and something must be wrong. You can get this one if you format with D code and switch to L code which has more sectors per track.
F4H 244	Timeout during a read waiting for the byte out (BO) bit to equal 1 on the 8291A chip. Probably a host error; possibly a defective 8291A chip. The timeout is active only on the first byte of each block of 256 bytes transferred.
F5H 245	The "END" bit in the 8291A was set for no apparent reason. This is not an error, but just a diagnostic aid.
F6H 246	Timeout waiting for the Data Request bit in the WD1010 status register to change polarity. Could be a defective WD1010 chip or data bus problem.
F7H 247	Timeout during a write waiting for the byte in (BI) bit to equal 1 on the 8291A chip. Probably a host error, possibly a defective 8291A chip. The timeout is only active on the first byte of each block of 256 bytes transferred.
F8H 248	The long read done prior to error correction resulted in good data. No error correction was required.
F9H 249	Error correction was used and was successful.
FAH 250	Error correction was attempted but did not make a correction. The length of the error must be greater than 2 bits. The data is still bad.
FBH 251	No data was acquired during the Long Read because of a header error, so error correction could not be done.
FCH 252	The configuration jumpers are set for a non-existent configuration.
FDH 253	The head had to be moved in one cylinder (higher cylinder number) and then back out before the sector could be read. The actuator must have a hysteresis problem.
FEH 254	The head had to be moved out one cylinder (lower cylinder number) and then back in before the sector could be read. The actuator must have a hysteresis problem.
FFH 255	The two syndromes calculated from the two long reads did not compare so error correction was not attempted.

Selftest LED

SELFTEST LED BLINKING RAPIDLY

If the selftest LED is blinking rapidly, then the 6809 thinks one of the following is bad: itself, the 128 byte data RAM, the ROM checksum, or the 8291A. The 6809 is not responding to bus activity and can only be reset by cycling power or shorting the reset line.

SELFTEST LED BLINKING SLOWLY

If the selftest LED is blinking slowly, then the 6809 has discovered a problem with the user stack and is not responding to bus activity. The 6809 must be reset by cycling power or shorting the reset line.

SELFTEST LED ON

The selftest LED is on during the power-on selftest or when a selftest command is given and goes off if the selftest is completed successfully. If the selftest fails the LED remains on. If the selftest ever goes on during normal drive operation, then there has been some sort of hardware failure. Reading the selftest results tell what the failure was.

SELFTEST LED OFF

This is the normal operating state and the drive and controller are working correctly.

Target Addresses

Any individual sector on any attached drive can be addressed with a unit number, a cylinder number, a head number and a sector number. Every command which accesses the disc has to derive the address of the sector (or sectors) that are to be written or read. This address is called the target address.

Each attached unit has a current target address consisting of the cylinder, head and sector numbers. The target address may be set for any unit by the Seek command or the Set Address Record command. A clear command clears all target addresses. A "current unit" is also maintained, and is set to the last valid unit number given in any command with a unit number parameter.

These target addresses are used in different ways by different commands. The Request Logical Address command always returns the current target address for the current unit. Most other commands require a unit number parameter, and use the current target address for that unit. All of the read and write commands work this way.

Note that while the Seek and Set Address Record commands are the only ones that allow the host to set an arbitrary target address, the target address may be changed during normal execution of other commands. The read and write commands, for example, increment the target address after reading each sector so that consecutive sectors may be read. If a read or write error occurs, the target address is left pointing to the sector at which it occurred. The verify command also increments the target address, and uses the target address to point to a defective sector if one is found.

Power-On State

When power is first applied to the 09133-69514 controller, the controller will not respond to parallel polls and conducts a selftest of the controller electronics and drive. When the attached drive is ready and has been tested, the controller enables parallel poll. The maximum time from power-on until the parallel poll is enabled is roughly 60 seconds. The actual time should be considerably less if no hardware errors are detected.

Status after a NORMAL powerup will be (for all units):

DSJ = 2

S1 = 0

Selftest results = 0,0

Current unit = 0

Target addresses = 0,0,0 (cylinder,head,sector) for all units.

Stat 2 bits after normal powerup depend on the status of each unit.

	Unit attached and formatted	Unit attached not formatted	Unit not attached	Unit not allowed	
S1	=	0	0	0	17H
*	=	0	0	1	0
TTTT	=	0110	0101	0	0
E	=	0	0	0	0
C	=	0	0	0	0
SS	=	00	00	10	0

If errors are detected during the powerup selftest, the selftest bytes are set non-zero, and other status is set appropriately.

The single red LED on the 09133-69514 controller board goes on at power-on, stay on during selftest, and go off if the selftest was completed successfully. If the selftest failed the red LED remains on or blinks on and off.

Overview of Command Set

The 09133-69514 controller uses the Amigo command set. This section explains the general structure of the Amigo commands. The chart which follows and the sections “Command Order” and “Command Timing” provide additional detail. Each command also has its own explanation of syntax and function in the command descriptions.

Amigo commands can take one of several forms. The simplest is a universal command which is made up of a single primary. The only universal that we recognize is the Universal Clear. See the command description for details.

The Identify command has a syntax that is unique in the command set. The Amigo Clear also has a syntax unlike any other command. These commands are described in their respective command descriptions.

The more standard commands all have the following general structure:

1. controller is addressed to talk (listen) with a Primary talk (Primary listen) to its address
2. controller receives a secondary
3. controller sends (receives) one or more data bytes to (from) the host.

The meaning of the data bytes depends on the particular command. They may be parameters, status information, or data being written or read. The correct number of bytes is also dependent on the command.

The recommended HP-IB sequence for these commands is:

1. Primary talk (or Primary listen)

2. Secondary
3. Data bytes, if any, transferred; last one tagged with EOI
4. Primary untalk (or Primary unlisten).

This is the type of sequence shown in the individual command descriptions. Variations on this sequence are allowed to support existing drivers. These variations are described below.

The Primary listen or Primary talk may be omitted if the controller is still in the correct state (addressed to listen or addressed to talk) from a previous command.

If the 09133-69514 controller is receiving data, then a byte tagged with EOI is the recommended way of terminating the transfer. A number of other termination conditions are recognized, including:

- UNL (unlisten)
- IFC (interface clear)
- any primary
- any secondary
- Universal Clear.

If the 09133-69514 controller is sending data, either the last data byte is tagged with EOI or the controller sends an extra byte of one tagged with EOI. The host may terminate the transfer earlier with:

- UNT (untalk)
- IFC
- any primary
- any secondary
- Universal Clear.

The preferred method is an Untalk.

After sending a byte tagged with EOI, the 09133-69514 controller will not attempt to send any more data until a new command is received.

Command Order

Certain commands must occur in pairs and in the correct order. If the first command in a pair is followed by any command other than the required one, or the second command is given without the first immediately prior to it, an I/O program error results.

The commands which must occur in order are listed next.

First command	Second command
Request status	Send address or status
Request logical address	Send address or status
Request physical address	Send address or status
Buffered read	Send data
Unbuffered read	Send data
Buffered read verify	Send data

Unbuffered read verify	Send data
Buffered write	Receive data
Unbuffered write	Receive data
Initialize	Receive data

Note that Initiate Selftest and Read Selftest form a logical pair of commands, but the ordering restriction does not apply. See the Read Selftest command description for details.

The same applies to Write Loopback and Read Loopback. The results of Read Loopback are meaningless unless a Write Loopback was executed previously, but certain other commands may occur between them. This allows the successful completion of the Write Loopback command to be verified by requesting status. Only the DSJ, Request Status, and Send Status commands are guaranteed to work without destroying the loopback data. The End command also works for 250 compatibility.

For the pairs listed in the columns above, however, no other commands can occur between them.

Command Timing

If hosts ignore the parallel poll status and send commands in rapid succession, the controller accepts the first command and begins its execution normally. The 8291A chip handshakes the next primary while the processor is executing the earlier command, but the secondary will not be taken off the bus until the controller finishes the first command and requests the next. This could cause a bus timeout if the host does not allow enough time for the previous command to finish before expecting a completed handshake.

With some currently implemented drivers for the 9895A, a problem occurs with the commands which must be received in pairs (see "Command Order.") For these we recognize the first command in the pair and immediately look for the second, to be compatible with hosts which do not wait for parallel poll. No long operations such as seeks will be done before the second command is received.

In any future documentation for driver implementers, we will specify that they should always wait for parallel poll to be re-enabled before sending another command.

After accepting the secondary command byte, the 09133-69514 controller disables the parallel poll response. This indicates that the device is busy processing the command sequence. The actual disabling of parallel poll response may occur up to 50 microseconds after the secondary is accepted by the 09133-69514 controller. If the controller has parallel poll enabled, and the host is fast enough to send a command sequence and then conduct a parallel poll before the 09133-69514 controller has disabled the poll, the bus controller would see the wrong parallel poll response. To solve this problem, the host should introduce an intentional delay.

The 9895A and the 09133-69514 controller differ in their response time because they use different HP-IB chips.

Command Set Summary

The following chart summarizes the HP-IB sequences which are recognized as valid commands, grouped by secondaries.

The following commands are not included in the chart because they each have an HP-IB sequence that is unique.

- Amigo Clear
- Selected Device Clear
- Universal Clear
- Identify

See each command description for details.

Several commands supported by the 9895A are not supported by the 09133-69514 controller. If one of these commands is given, an I/O Program Error or Illegal Opcode results. These commands are:

- Cold Load Read
- Set File Mask
- ID Triggered Read
- Download controller.

The command descriptions for these commands show their syntax. They are not included in the chart.

The following abbreviations are used for data bytes listed in the chart.

UNIT	unit number
CYLH,CYLL	cylinder number (high and low bytes)
HEAD	head number
SEC	sector number
SCNTH,SCNTL	sector count (high and low bytes)
F	format override select
DSJ	DSJ value
ST1,ST2	selftest results
X	don't care

Blanks in the opcode column indicate that no opcode is used; the secondary applies to only one command.

Note that only the lower five bits of opcodes are checked. Although the upper three bits are shown as zeros throughout this document, they are actually "don't care" bits.

Command Set Summary

Secondary	Opcode	Command Name	Data Bytes
Commands following Primary Listen:			
	00	Receive Data	<data>
08	02	Seek	UNIT,CYLH,CYLL,HEAD,SEC
	03	Request Status	UNIT
	05	Unbuffered Read	UNIT
	07	Verify	UNIT,SCNTH,SCNTL
	08	Unbuffered Write	UNIT
	0B	Initialize	UNIT
	0C	Set Address Record	UNIT,CYLH,CYLL,HEAD,SEC
	14	Request Logical Address	X
	15	End	X
09	08	Buffered Write	UNIT
0A	03	Request Status	UNIT
	05	Buffered Read	UNIT
	14	Request Logical Address	X
0B	05	Buffered Read Verify	UNIT
0C	05	Unbuffered Read Verify	UNIT
	14	Request Physical Address	X
	18	Format	UNIT,F,X,X
	19	Door Lock	UNIT
	1A	Door Unlock	UNIT
10		Amigo Clear (see description)	
11		HP-IB CRC	X,X, . . .
1E		Write Loopback	<data>
1F		Initiate Selftest	X,X
Commands following primary talk are shown next.			
00		Send Data	<data>
08		Send Address or Status	<four bytes>
10		DSJ	DSJ
11		HP-IB CRC	1
1E		Read Loopback	<data>
1F		Read Selftest	ST1,ST2

Holdoffs

Three holdoffs are defined. If a command is held off the controller sends a byte (01H) tagged with EOI if it was addressed to talk. If the controller was addressed to listen it accepts as many bytes as the host sends. The three holdoffs are listed below, and the following chart details the effect of each.

The DSJ=2 holdoff happens after the controller is powered up, or after a selftest.

The first status holdoff occurs under the same conditions as DSJ=2, that is, after powerup or selftest. First status is set only for units which are attached.

The DSJ=1 and S1 is not I/O program error (S1<10) and S1 is not Illegal Opcode (S1<1) holdoff occurs when an error has occurred, but it is not I/O program error or Illegal Opcode. In other words, a serious error has occurred and the host has apparently not checked status (which would clear S1) to find out about it.

Other conditions may be necessary for execution of a particular command. Correct command syntax is always a requirement. Parameters must also be within allowable ranges. Commands which access the disc require that the selected unit be attached and formatted. The requirements for execution for each command are given in the command descriptions.

Holdoff Table

Command Name	None	DSJ=2	First Status	DSJ=1, S1<>1, S1
Identify	X	-	-	-
DSJ	X	-	-	-
Universal clear	X	-	-	-
Amigo clear	X	-	-	-
Selected device clear	X	-	-	-
Request status	-	X	-	-
Request logical addr	-	X	-	-
Request physical addr	-	X	-	-
Seek	-	X	X	-
Set address record	-	X	X	-
Buffered read verify	-	X	X	X
Unbuffered read verify	-	X	X	X
Buffered read	-	X	X	X
Unbuffered read	-	X	X	X
Buffered write	-	X	X	X
Unbuffered write	-	X	X	X
Verify	-	X	X	-
Initialize	-	X	X	-
Format	-	X	X	-
Initiate self test	X	-	-	-
Read self test	X	-	-	-
Write loopback record	X	-	-	-
Read loopback record	X	-	-	-
End	-	X	-	-
Door lock	-	X	X	X
Door unlock	-	X	X	X
HP-IB CRC	X	-	-	-

X : HOLDOFF APPLIES

- : HOLDOFF DOES NOT APPLY

NOTE

Send Address Or Status, Send Data, and Receive Data are held off if the proper preceding command is held off.

Command Descriptions

Each command is described individually in the following pages. This outline is a guide to the information in each command description.

Name of Command

HP-IB Sequence:

The sequence of events over the HP-IB for a command with good syntax and normal completion. Bytes from the host to the 09133-69514 controller are shown as (X X X X X X X), and bytes from the 09133-69514 controller to the host are shown as -X X X X X X X-.

Description:

The function of the command.

Effect on status:

The status results for a normal completion, along with any special cases which need to be shown. A separate section of this document gives the interpretation of all of the status bits if an error occurs. See the "Status" section.

Requirements for execution:

Status requirements, valid parameter ranges, and other conditions which determine whether or not this command may be executed.

Variation from 9895A:

Usually applies only to D-codes. Any significant differences that exist between the 09133-69514 controller's response to a command and that of a 9895A.

Variations from the HP OEM Controllers:

Usually applies only to D-codes and/or L5-codes. Significant differences from the HP OEM Controller's treatment of a command.

Amigo Clear

HP-IB Sequence:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 1 0 0 0 0)	ATN	Secondary
	PPD	
(X X X X X X X X)	EOI	Control byte
(P 0 0 0 0 1 0 0)	ATN	Selected device clear primary
	Clear done here
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

Description:

The Amigo Clear command has the same effect as the Universal Clear command except that only one device is cleared. This command is also called HP300 Clear.

This command is highly preferred over the standard form for a Selected Device Clear (SDC). The 09133-69514 controller recognizes SDC's only in certain forms. See the Selected Device Clear command.

Effect on Status:

See universal clear.

Requirements for Execution:

None.

Variation from 9895A:

Parity control byte is ignored.

Variation from the HP OEM Controllers:

None.

Buffered Read and Send Data

HP-IB Sequence,

Buffered Read command:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 0 1 0)	ATN	Secondary
	PPD	
(0 0 0 0 0 1 0 1)		Opcode for Buffered Read
(X X X X U U U U)	EOI	Unit number
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

where: UUUU is the unit number.

Send Data command:

(P 1 0 A D D R S)	ATN	Primary talk
(P 1 1 0 0 0 0 0)	ATN	Secondary for Send Data
	PPD	
.	.	Read being performed
- X X X X X X X -		Data is in buffer.
.	.	Data Bytes being sent to host.
- X X X X X X X -		Last data byte.
- 0 0 0 0 0 0 1 -	EOI	Extra byte with EOI
	PPE	Read is done
(P 1 0 1 1 1 1 1)	ATN	Untalk.

Description:

To perform a buffered read of one sector, the Buffered Read command is given, followed by the Send Data command. These commands must occur in this sequence or an I/O program error results.

Data is transferred to a buffer on the 09133-69514 controller board before being sent to the host. The host can then accept the data bytes at any rate within the 09133-69514 controller's capabilities.

The data is transmitted over the HP-IB if it is good or if it has a Data CRC error. The data bytes (256) are sent, followed by one byte of value 1 tagged with EOI. If a D bit was encountered, the ID field couldn't be found, or the Data Mark was bad, then only the single byte of value 1 is transmitted over the HP-IB.

If the data was good, the target address is incremented whether the full sector was transferred to the host or not. If the data was bad, or couldn't be found, the target address points to the bad data.

The target address can be incremented into an address which is not allowed. No error is reported unless an attempt is made to read the out-of-bounds sector.

If more than one sector is to be transferred, then any number of buffered reads can be used in succession. If an error is encountered all following reads are held off due to DSJ=1, so an error in the middle of a long read cannot go unreported.

Effect on status,

No errors, successful read:

S1 - 0

Stat 2 - Unchanged

DSJ - 0.

Requirements for execution:

The correct number of parameter bytes must be received

The unit number selected must be attached and formatted

DSJ not 2

First status bit not be set

If DSJ=1, then S1 must be 0AH (I/O program error) or 01H (Illegal opcode)

The target address (Cylinder, head, and sector) must be valid for the configuration.

Variation from 9895A:

The 9895A can have discs with an IBM format, using 128 bytes per sector. The 09133-69514 controller always uses 256-byte sectors .

The 9895A transfers the data if a D bit is encountered. Because of the way the WD1010 works, the 09133-69514 controller does not get any data and would have to pass dummy bytes. We send one byte tagged with EOI.

Variation from the HP OEM Controllers:

For a read of a target address which is not allowed, the HP OEM Controllers sets the D bit and sets S1 to 11H. We set the C bit,A bit, * bit and S1 = 1FH.

Buffered Read Verify and Send Data

HP-IB Sequence,

Buffered Read Verify command:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 0 1 1)	ATN	Secondary
	PPD	
(0 0 0 0 0 1 0 1)		Opcode for Buffered Read Verify
(X X X X U U U U)	EOI	Unit number
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

where: UUUU is the unit number.

Send Data command:

(P 1 0 A D D R S)	ATN	Primary talk
(P 1 1 0 0 0 0 0)	ATN	Secondary for Send Data
	PPD	
	...	Read verify being performed
- X X X X X X X -		Data is in buffer
		Data bytes being set to host
...		...
- X X X X X X X -		Last data byte
- 0 0 0 0 0 0 1 -	EOI	Extra byte with EOI
	PPE	Buffered Read Verify is done
(P 1 0 1 1 1 1 1)	ATN	Untalk.

Description:

This command is identical to Buffered Read and Send Data.

Buffered Write and Receive Data

HP-IB Sequence,

Buffered Write command:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 0 0 1)	ATN	Secondary
	PPD	
(0 0 0 0 1 0 0 0)		Opcode for Buffered Write
(X X X X U U U U)	EOI	Unit number
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

where: UUUU is the unit number.

Receive data command:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 0 0 0 0)	ATN	Secondary
	PPD	
(X X X X X X X X X)		Data bytes
(X X X X X X X X X)	EOI	Last data byte
	PPE	
	...	Writing onto disc
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

Description:

The Buffered Write and Receive Data commands are used to write one sector of data. This sequence must be followed or an I/O program error results.

The disc controller takes data transmitted on the HP-IB and stores it in an internal buffer before writing it on the disc. This buffering allows the host to transmit the bytes at any rate allowed by the 09133-69514 controller.

The 09133-69514 controller accepts the data bytes over the HP-IB until it has accepted 256 bytes, receives a byte tagged with EOI, or has been terminated by the host in some other manner. If less than 256 bytes are received, the remaining bytes are filled with zeros.

If more than one sector is to be written, any number of Buffered Write and Receive Data commands can be used in succession. The 09133-69514 controller increments the address automatically after each successful write. A write will fail if it follows another write which failed, so an error will not go unreported.

Effect on status,

No errors:
S1 - 0
Stat 2 - Unchanged
DSJ - 2.

Requirements for execution:

The requirements for execution are the same as those for a Buffered Read; see the Buffered Read and Send Data command.

Variation from 9895A:

No IBM format with sectors of 128 bytes is possible.

Variation from the HP OEM Controllers:

None.

Cold Load Read

HP-IB Sequence:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 0 0 0)	ATN	Secondary
	PPD	
(0 0 0 0 0 0 0 0)		Opcode
(X X X X X X X X)	EOI	Head and sector
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

where: X is a don't care.

Description:

The Cold Load Read command is not supported by the 09133-69514 controller.

Effect on status:

S1 - Illegal opcode
 Stat 2 - Unchanged
 DSJ - 1.

Requirements for execution:

None.

Variation from 9895A:

The 09133-69514 controller does not support the Cold Load Read command

Variation from the HP OEM Controllers:

None.

Door Lock

HP-IB Sequence:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 1 0 0)	ATN	Secondary
	PPD	
(0 0 0 1 1 0 0 1)		Opcode
(X X X X U U U U)	EOI	Unit
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

where: UUUU is the unit number.

Description:

No action is taken (no doors are locked), but status is updated to match 9895A operation.

The requirements for execution are checked, and if these are met, the current unit number is updated and status is cleared as described below.

Effect on status:

S1 - 0
Stat 2 - unchanged
DSJ - 0.

Requirements for execution:

DSJ not 2,
Not first status.
Variation from 9895A:
No doors.

Variation from the HP OEM Controllers:

None.

Door Unlock

HP-IB Sequence:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 1 0 0)	ATN	Secondary
	PPD	
(0 0 0 1 1 0 1 0)		Opcode
(X X X X U U U U)	EOI	Unit
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

where: UUUU is the unit number.

Description:

This command is accepted, but no action is taken; treatment is identical to Door Lock; see the Door Lock command.

Download

HP-IB Sequence:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 1 1 1)	ATN	Secondary
	PPD	
(X X X X X X X X)		1 to 256 bytes for 9895A
.	.	.
(X X X X X X X X)	EOI	
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

Description:

This command is unrecognized.

Effect on status:

Unrecognized secondary causes I/O program error.

Requirements for execution:

None.

Variation from 9895A:

The 09133-69514 controller does not support the Download command.

Variation from the HP OEM Controllers:

None.

Device Specified Jump (DSJ)

HP-IB Sequence:

(P 1 0 A D D R S)	ATN	Primary talk
(P 1 1 1 0 0 0)	ATN	Secondary
	PPD	
- DSJ -	EOI	DSJ byte
(P 1 0 1 1 1 1)	ATN	Untalk.

where: DSJ is 0, 1 or 2.

Description:

The controller returns a byte indicating that the last operation completed normally or abnormally, or that the controller has just completed a power up or selftest. This command also provides a way to disable the parallel poll response. After accepting the DSJ secondary, the 09133-69514 controller disables parallel poll response (within 50 microseconds.) The DSJ values are as follows:

DSJ = 0	The last operation completed normally
DSJ = 1	The last operation ended abnormally; status indicates the current error
DSJ = 2	A power-up or selftest sequence completed DSJ = 2 is a holdoff state.

Effect on status:

S1 - unchanged
Stat 2 - unchanged

DSJ - If DSJ = 2 before this command, then DSJ0; else, unchanged.

Requirements for execution:

None.

Variation from 9895A:

No DSJ = 3 is possible.

Variation from the HP OEM Controllers:

None.

END

HP-IB Sequence:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 0 0 0)	ATN	Secondary
	PPD	
(0 0 0 1 0 1 0 1)		Opcode
(X X X X X X X X)	EOI	Data Byte
(P 0 1 1 1 1 1)	ATN	Unlisten.

Description:

If a First Status bit (F) is set for any unit (searching from unit 3 to unit 0), then do the following,

1. Set current unit to unit with First Status set
2. Set the A bit (Attention) for that unit
3. Set DSJ=1, S1=1FH
4. Enable parallel poll

Otherwise, do the following instead:

1. Set S1 and DSJ to zero
2. Do not enable parallel poll.

This command is used on the 9895A flexible disc controller to notify the bus controller that a flexible disc has been removed or inserted.

Effect on status:

None.

Requirements for execution:

DSJ not 2.

Variation from 9895A:

None.

Variation from the HP OEM Controllers:

The HP OEM controller doesn't check DSJ holdoff.

Format

HP-IB Sequence:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 1 0 0)	ATN	Secondary
	PPD	
(0 0 0 1 1 0 0 0)		Opcode for Format
(X X X X U U U U)		Unit Number
(F X X X X X X X)		Override select bit
(X X X X X X X X)		Interleave
(X X X X X X X X)	EOI	Data Byte
	.	Format is in progress
	PPE	Format is done
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

where: UU is the unit number

F is the override old format bit

F=1 means to override the old format; the 09133-69514 controller formats the unit, sparing the worst sectors on each track

F=0 means to not override the old format; the 09133-69514 controller will not do any writing on the disc

The interleave can be any value and is not used by the 09133-69514 controller; on the 09133-69514 controller the interleave is always 9

The data byte can be any value and is not used by the 09133-69514 controller; the data pattern is always FFH.

Description:

The Format command is a part of the sequence of commands which changes a disc which is unformatted or has the wrong format into a disc with a usable format.

Formatting writes headers and data into all sectors of all tracks on a unit. The 0FFH data pattern is used.

If the F bit = 0, no formatting or writing on the disc is done.

If the F bit = 1, the 09133-69514 controller formats each track, reads back all sectors of the track, and repeats this process, keeping track of which sectors were bad and which took the most retries to recover the data. The track is then re-formatted sparing the 1 or 2 worst sectors. The number spared depends on the configuration.

The target address is set to 0,0,0 after the command is complete, whether the F bit was 0 or 1.

Effect on status,

No errors:

S1 - 0
Stat 2 - Unchanged
DSJ - 0.

Requirements for execution:

The correct number of parameter bytes must be received

The selected unit must be attached

DSJ not 2

First status bit not set for selected unit.

Variation from 9895A:

The 09133-69514 controller does not support variable interleave

The 9895A formats with a spiral offset; the 09133-69514 controller does not

The 9895A spares tracks and the 09133-69514 controller spares sectors

The 09133-69514 controller does nothing if F = 0

Because the 9895A has HP and IBM formats, it uses the Override Old Format Bit (F) differently than the 09133-69514 controller

Variation from the HP OEM Controllers

The 09133-69514 controller attempts to use the best sectors available by doing some sparing during the Format command.

HP-IB CRC

HP-IB Sequence (Talked version):

(P 1 0 A D D R S)	ATN	Primary talk
(P 1 1 1 0 0 0 1)	ATN	Secondary
	PPD	
- 0 0 0 0 0 0 1 -	EOI	
	PPE.	

HP-IB Sequence (Listened version):

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 1 0 0 0 1)	ATN	Secondary
	PPD	
(X X X X X X X X)		
	...	
(X X X X X X X X)	EOI	Any number of data bytes
	PPE.	may be sent

Description:

This command is accepted without setting any error, but no action is taken.

Effect on status:

S1 - unchanged
 Stat 2 - unchanged
 DSJ - unchanged.

Requirements for execution:

None.

Variation from 9895A:

The 9895A sets I/O program error if any data bytes are sent in the listened version; this is not as described by 9895A documentation.

Variation from the HP OEM Controllers:

The HP OEM controllers source multiple bytes of 1 with EOI for the talk version.

Identify**HP-IB Sequence:**

(P 1 0 1 1 1 1)	ATN	Primary UNTALK
(P 1 1 A D D R S)	ATN	My secondary
- ID1 -		First ID byte
- ID2 -	EOI	Second ID byte.

Description:

Note the non-standard sequence using a untalk followed by a secondary. The ADDRS in the secondary is the address normally recognized in primaries.

The controller will return the two identify bytes repeatedly as long as the host accepts them.

A listen address to any other address but the controller's can be sent after "my secondary" and is ignored. (This is for compatibility with the 250).

The Identify bytes are dependent on the configuration selected. See the configuration descriptions for specific values.

Effect on status:

None.

Requirements for execution:

None.

Variation from 9895A:

None.

Variation from the HP OEM Controllers:

None.

ID Triggered Read

HP-IB Sequence:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 0 1 1)	ATN	Secondary
	PPD	
(0 0 0 0 0 1 1 0)		Opcode
(X X X X X X X X)	EOI	
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

where: X is a don't care.

Description:

This command is not supported.

Effect on status:

S1 - Illegal opcode
Stat 2 - Unchanged
DSJ - 1

Requirements for execution:

None.

Variation from 9895A:

The 09133-69514 controller does not support the ID Triggered Read command.

Variation from the HP OEM Controllers:

None.

Initialize and Receive Data

HP-IB Sequence,

Initialize command:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 0 0 0)	ATN	Secondary
	PPD	
(0 0 D 0 1 0 1 1)		Opcode for Initialize
(X X X X U U U U)	EOI	Unit number
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

where: D is the D bit
 UUUU is the unit number.

Receive Data command:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 0 0 0 0)	ATN	Secondary for Receive Data
	PPD	
(X X X X X X X X)		Data bytes
		.
(X X X X X X X X)	EOI	Last data byte
		.
	PPE	Performing the Initialization
		.
(P 0 1 1 1 1 1 1)	ATN	PPE after Initialize is done.
		Unlisten.

Description:

The Initialize command must be followed by a Receive Data command. Any other command following the Initialize command result in an I/O program error.

If D = 1, the 09133-69514 controller will:

1. Format the track using the data byte 0E5H
2. Verify the track noting the worst sectors
3. Repeat steps one and two 25 times getting more data on which sectors contain the most hard errors or require the most number of retries to recover the data
4. Re-format the track replacing the worst sectors with spares, again using the data byte OFFH.

The target address is not changed in this case.

If D = 0, the 09133-69514 controller does nothing except increment the target address.

The Initialize command does sparing of bad sectors. The interleave is always 9.
 Effect on status,

No errors:
 S1 - 0
 Stat 2 - Unchanged
 DSJ - 0

Requirements for execution:

The correct number of parameter bytes must be received

The selected unit must be attached and formatted

DSJ not 2

First status bit not set for selected unit

The target address (cylinder, head, and sector) must all be valid for the configuration.

Variation from 9895A:

The 9895A is quite different in that it spares tracks, not sectors. See the 9895A manual for an explanation of its Initialize command.

The 9895A writes out the data to the target address; we always write the byte 0FFH.

Variation from the HP OEM Controllers:

The 09133-69514 controller handles sparing during Initialize in a manner much like that of the HP OEM controllers except for D=1, where the HP OEM controller increments the target address whereas the 09133-69514 controller and the 9895A do not.

Initiate Selftest

HP-IB Sequence:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 1 1 1 1)	ATN	Secondary
	PPD	
(X X X X X X X X)		Cylinder (ignored)
(X X X X X X X X)	EOI	Control (ignored)
...		Self tests are done here
	PPE	
(P 0 1 1 1 1 1)	ATN	Unlisten.

where: X is a don't care.

Description:

In this description, the general selftest strategy is described first, followed by additional detail on how this particular command fits into the strategy.

Selftests are performed under three conditions: at power-on (or processor reset), in response to the Initiate Selftest command, and during normal execution. Of these three modes of selftest, the power-on test is the most complete, followed by the selftest initiated in response to the command. The continual selftesting during normal command execution means that if a hardware error is detected during the execution of any command, a selftest error is set, along with appropriate status.

The power-on selftest begins by testing the processor, ROM, RAM, and the 8291A chip. A failure during any of these tests results in the processor attempting to stop execution altogether. In this case the processor hangs in a routine which blinks the selftest LED. An 8291 error means communication with the host is impossible, so continued execution is useless at best. A processor, RAM, or ROM error means that continued execution is dangerous. For example, a stuck bit in RAM or in a processor register could cause writes to be done to the wrong cylinder.

If this first part of the power-on selftest completes without error, the Initiate Selftest command is executed to complete the selftest and to initialize the system to its power-on state. The Initiate Selftest command causes the following to be done:

Test the WD1010 buffer

Test the WD1010 chip itself

Test the attached drive (restore, seek, scanid, write/read)

Check to see if the attached drive is consistent with the configuration setting

Set the TTTT, SS, and F bits for each unit to show its status (attached/not attached, formatted/not formatted)

Test the input and output ports

Reset the WD 1010 chip

Reset and initialize the 8291A chip

Update the HP-IB address from the switches

Set the current unit to zero

Clear all Stat 2 bits for all units (except TTTT, SS, and F which were set previously)

Clear all target addresses

Set S1 to zero

Set DSJ to 2.

If any of the tests fail, the selftest results show that failure and no other tests are tried.

The cylinder number and the control byte are ignored. A write/read test is done using all heads on the maximum cylinder of the disc (configuration dependent) if the drive is formatted.

The single red LED on the 09133-69514 controller is turned on during the selftest. If the self-test completes without error, the red LED is turned off. If the selftest fails, the red LED is left on or blinks depending on the error. The LED is turned off when the selftest results are read by the host.

Effect on status,

No errors:

S1 - 0

Stat 2 - Cleared; F,SS, and TTTT reset as appropriate

DSJ - 2.

Errors during test (Selftest failed):

S1 - Cleared

S2 - F,SS,TTTT reset as appropriate

*E,C bits set to show error, if appropriate

DSJ - 2.

Requirements for execution:

None.

Variation from 9895A:

The 09133-69514 controller ignores cylinder number and write/read test selection.

Variation from the HP OEM Controllers:

A great deal; see the MSC Selftest explanation at the end of this section.

Read Loopback Record

HP-IB Sequence:

(P 1 0 A D D R S)	ATN	Primary talk
(P 1 1 1 1 1 0)	ATN	Secondary
	PPD	
- X X X X X X X X -		
.		
- X X X X X X X X -	EOI	9 bytes
(P 1 0 1 1 1 1 1)	ATN	Untalk.

Description:

The controller sends up to 9 bytes of loopback data over the HP-IB bus. This is used by diagnostics to test the HP-IB data path. The bytes are sent back in the same order in which they were received (see the Write Loopback Record command.) The 9th byte is tagged with EOI.

Effect on status:

S1 - 0
Stat 2 - unchanged
DSJ - unchanged

Requirements for execution:

None.

Variation from 9895A:

The number of bytes stored is not 256, as in the 9895A.

Variation from the HP OEM Controllers:

The HP OEM controllers allowed up to 12 bytes to be stored. It also assumes that the number of bytes written is the number of bytes that will be read, and tags EOI accordingly. The 9895A and the 09133-69514 controllers, however, tag EOI only for the Nth byte (N=256 for 9895A).

Read Selftest Results

HP-IB Sequence:

(P 1 0 A D D R S)	ATN	Primary talk
(P 1 1 1 1 1 1 1)	ATN	Secondary
	PPD	
- E 0 U U 0 H H H -		Selftest results
- ERROR CODE -	EOI	Selftest results
	PPE	
(P 1 0 1 1 1 1 1)	ATN	Untalk.

where: E = 1 means error has occurred

U U = unit on which error occurred

H H H = head number for which error occurred

ERROR CODE is the selftest results byte.

NOTE

If there are no errors, both returned bytes are zero.

Description:

The selftest is performed after an Initiate Selftest command, and is automatically performed at power up. The selftest results are also updated if an error occurs during normal operation or if something occurs which has diagnostic information, such as error correction being used. If you do a selftest and then read the selftest results, you get the selftest results. If you read selftest results long after the selftest was done, you either get the results of the last selftest, the results of the most recent hardware failure, or some diagnostic information.

Effect on status:

- S1 - 0
- Stat 2 - unchanged
- DSJ - unchanged

Requirements for execution:

None.

Variation from 9895A:

The 09133-69514 controller defines the two bytes differently.

Variation from the HP OEM Controllers:

The 09133-69514 controller defines the two bytes differently.

Receive Data

HP-IB Sequence:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 0 0 0 0)	ATN	Secondary
	PPD	
(X X X X X X X X)		Data bytes
(X X X X X X X X)		...
...		...
...		...
(X X X X X X X X)	EOI	Last data byte
	PPE	PPE after writing completed.
(P 0 1 1 1 1 1)	ATN	Unlisten.

Description:

The Receive data command must follow a Buffered Write, Unbuffered Write or Initialize command. If the preceding command was not one of these, an I/O program error results and the command is not executed.

For more information about this command see the following commands:

Buffered Write and Receive Data
 Unbuffered Write and Receive Data
 Initialize and Receive Data.

Request Logical Address and Send Address

HP-IB Sequence:

Request Logical Address command:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 0 X 0)	ATN	Secondary (two possible)
	PPD	
(0 0 0 1 0 1 0 0)		Opcode
(X X X X X X X X)	EOI	Don't care
	PPE	
(P 0 1 1 1 1 1)	ATN	Unlisten.

Send Address or Status command:

(P 1 0 A D D R S)	ATN	Primary Talk
(P 1 1 0 1 0 0 0)	ATN	Secondary
	PPD	
- C C C C C C C C -		Cylinder - high
- C C C C C C C C -		Cylinder - low
- H H H H H H H H -		Head
- S S S S S S S S -		Sector
- 0 0 0 0 0 0 0 1 -	EOI	Extra byte with EOI
	PPE	
(P 1 0 1 1 1 1 1)	ATN	Untalk.

Description:

In response to this command pair, the 09133-69514 controller sends the four-byte current target address. The two possible secondaries (because of the Don't Care bit) have identical results.

Effect on status:

S1 - 0
 Stat 2 - Unchanged
 DSJ - 0.

Requirements for execution:

DSJ not 2.

Variation from 9895A:

None.

Variation from the HP OEM Controllers:

None.

Request Physical Address and Send Address

HP-IB Sequence,**Request Physical Address command:**

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 1 0 0)	ATN	Secondary
	PPD	
(0 0 0 1 0 1 0 0)		Opcode
(X X X X X X X X)	EOI	Don't care
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

Send Address or Status command:

(P 1 0 A D D R S)	ATN	Primary Talk
(P 1 1 0 1 0 0 0)	ATN	Secondary
	PPD	
- C C C C C C C C -		Cylinder--high
- C C C C C C C C -		Cylinder--low
- H H H H H H H H -		Head
- 0 0 0 0 0 0 0 0 -		Zeroes
- 0 0 0 0 0 0 0 1 -	EOI	Extra byte tagged with EOI
	PPE	
(P 1 0 1 1 1 1 1)		ATN Untalk.

Description:

The controller sends the four-byte physical address. The physical address is the same as the logical address, except that the sector number byte is replaced with zeros.

Effect on status:

S1 - 0
Stat 2 - Unchanged
DSJ - 0.

Requirements for execution:

DSJ not 2.

Variation from 9895A:

The 09133-69514 controller physical and logical addresses are always the same.

Variation from the HP OEM Controllers:

None.

Request Status and Send Status

HP-IB Sequence,

Request Status command:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 0 X 0)	ATN	Secondary (two possible)
	PPD	
(X X X 0 0 0 1 1)		Opcode
(X X X X U U U U U)	EOI	Unit
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

where: X is a don't care

UUUU is the unit number.

Send Address or Status command:

(P 1 0 A D D R S)	ATN	Primary Talk
(P 1 1 0 1 0 0 0)	ATN	Secondary
	PPD	
- 0 0 D S S S S S -		
- 0 0 0 0 0 0 U U -		
- * 0 0 T T T T X -		
- A 0 0 E F C S S -		
- 0 0 0 0 0 0 0 1 -	EOI	Extra byte tagged with EOI.
	PPE	
(P 1 0 1 1 1 1 1)	ATN	Untalk.

Description:

In response to this command pair, the 09133-69514 controller sends four bytes of status.

If the unit number is out of range, then the four bytes returned are:

17H	(S1 - unit unavailable)
bad unit number	
0	
0.	

Although an S1 value of 17H is returned, S1 is set to zero upon completion of this command. Any previous S1 error is forgotten. DSJ is also set to 0. The logical address stays the same, with the unit being the last valid unit accessed.

Note that if a valid unit number is given as a parameter, the unit given becomes the next current unit. Stat 1 (first two bytes) is returned for the last valid unit accessed, but Stat 2 represents status for the unit given as a parameter.

Effect on status,

No errors:	
S1 - 0	
Stat 2 - Bits A,E,F,C are cleared for unit given as parameter.	
DSJ - 0.	

Requirements for execution:

DSJ not 2

Unit number within allowed range for configuration.

Variation from 9895A:

None.

Variation from the HP OEM Controllers:

None.

SEEK**HP-IB Sequence:**

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 0 0 0)	ATN	Secondary
	PPD	
(0 0 0 0 0 0 1 0)		Opcode
(X X X X U U U U)		Unit number
(C C C C C C C C)		Cylinder High
(C C C C C C C C)		Cylinder Low
(0 0 0 0 0 H H)		Head
(S S S S S S S S)	EOI	Sector
(P 0 1 1 1 1 1 1)	ATN	Unlisten
	...	Seek in progress
	PPE	On seek completion.

where: UUUU is the unit number
CCCCCCCC is the cylinder number (two bytes)
HH is the head number
SSSSSSSS is the sector number.

Description:

The seek command updates a unit's target address and moves the head actuator to the new target cylinder. A seek usually precedes a data transfer operation or a series of consecutive data transfers.

The target address will only be set if it is valid for the configuration.

The 09133-69514 controller does not support overlapped seek operations. The seek is completed before parallel poll is re-enabled and another command may be executed.

Effect on status,

No errors:

S1 - 1FH

Stat 2 - A bit set

DSJ - 0.

Requirements for execution:

The correct number of parameter bytes must be received

The selected unit must be attached and formatted

DSJ not 2

First status bit not set

The target address (cylinder,head,sector) must be valid for the configuration.

Variation from 9895A:

Because the 9895A has a removable media, some of the conditions for setting the S1 Drive Attention are different.

Variation from the HP OEM Controllers:

None.

Selected Device Clear

HP-IB Sequence:

(P 1 0 A D D R S)	ATN	Primary listen
(0 0 0 0 0 1 0 0)	ATN	Selected device clear
	PPD	
	...	Clear done here
	PPE.	

Description:

The 09133-69514 controller supports this command in a limited fashion for compatibility with existing host drivers. Special hardware has been added to allow the previous syntax to be recognized. The syntax for an Amigo Clear, which includes a Selected Device Clear primary, can be recognized by the 09133-69514 controller without the additional hardware. For this reason, in all documentation and in interaction with people writing host drivers, we highly discourage the use of SDC commands except in the Amigo Clear syntax.

Future versions of the 09133-69514 controller may not include the hardware required to support SDC's.

Note also that other legal forms of the SDC command are possible that are not supported at all; now or ever.

See the universal clear command for a list of the operations done by the 09133-69514 controller during the Clear.

Send Address or Status**HP-IB Sequence:**

(P 1 0 A D D R S)	ATN	Primary talk
(P 1 1 0 1 0 0 0)	ATN	Secondary
	PPD	
- X X X X X X X X -		Byte 1
- X X X X X X X X -		Byte 2
- X X X X X X X X -		Byte 3
- X X X X X X X X -		Byte 4
- 0 0 0 0 0 0 1 -	EOI	Terminating byte
	PPE	
(P 1 0 1 1 1 1 1)	ATN	Untalk.

Description:

This command results in an I/O Program error unless it immediately follows one of the following commands: Request Status, Request Logical Address, or Request Physical Address. For a description of the four bytes sent in response to each of these commands, see the particular command description.

A fifth byte of one tagged with EOI is always sent as shown previously.

Send Data**HP-IB Sequence:**

(P 1 0 A D D R S)	ATN	Primary talk
(P 1 1 0 0 0 0 0)	ATN	Secondary
	PPD	
- X X X X X X X X -		Data Bytes
.	.	.
- X X X X X X X X -	EOI	Last data byte
	PPE	
(P 1 0 1 1 1 1 1)	ATN	Untalk.

Description:

The Send Data command follows a buffered or unbuffered Read Request or a buffered or unbuffered Read Verify. These commands must precede the Send Data command or an I/O program error is set.

For further information, see the following commands:

Buffered Read and Send Data
Buffered Read Verify and Send Data
Unbuffered Read and Send Data
Unbuffered Read Verify and Send Data.

Set Address Record

HP-IB Sequence:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 0 1 0 0 0)	ATN	Secondary
PPD		
(0 0 0 0 1 1 0 0)		Opcode
(X X X X U U U U)		Unit number
(C C C C C C C C)		Cylinder High
(C C C C C C C C)		Cylinder Low
(0 0 0 0 0 0 H H)		Head
(S S S S S S S S)	EOI	Sector
(P 0 1 1 1 1 1 1)	ATN	Unlisten
	PPE.	

where: UUUU is the unit number

CCCCCCCC is the cylinder number (two bytes)

HH is the head number

SSSSSSSS is the Sector number.

Description:

The Set Address Record command is identical to the Seek command except that the actual seek is not done. The target address and status are set just as if a Seek command had been executed instead; the physical position of the heads remains unchanged.

See the Seek command description for details.

Set File Mask

HP-IB Sequence:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 0 1 0 0 0)	ATN	Secondary
PPD		
(0 0 0 0 1 1 1 1)		Opcode
(X X X X X X X X)	EOI	
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

where: X is a don't care.

Description:

This command was added by the HP OEM Controllers as a result of incorrect information about a particular host computer. It is useless, and is ignored.

Effect on status:

S1 - Illegal opcode
 Stat 2 - Unchanged
 DSJ - 1.

Requirements for execution:

None.

Variation from 9895A:

None.

Variation from the HP OEM Controllers:

Not supported.

Unbuffered Read and Send Data

Unbuffered Read command:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 0 0 0)	ATN	Secondary
	PPD	
(X X X 0 0 1 0 1)		Opcode for Unbuffered Read
(X X X X U U U U U)	EOI	Unit number
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

where: UUUU is the unit number.

Send Data command:

(P 1 0 A D D R S)	ATN	Primary talk
(P 1 1 0 0 0 0 0)	ATN	Secondary for Send Data
	PPD	
	...	
- X X X X X X X X -		First sector being read
		First sector data is in buffer
		Data bytes being sent to host
	...	
- X X X X X X X X -		The 256th data byte
		Next sector being read
		Data is in buffer

The process of reading and sending data continues until the host terminates the transfer or the end of the unit is reached

- X X X X X X X X - - X X X X X X X X - (P 1 0 1 1 1 1)	Data bytes being sent to host ATN PPE.
--	---

Description:

The unbuffered read allows more than one sector to be transferred from the disc to the bus controller using a single command.

To perform an unbuffered read, the Unbuffered Read command is given, followed by the Send Data command. The commands must be given in this order or an I/O program error results.

If the data is good, it continues to be transferred over the HP-IB bus in bursts of length 256 until the host terminates the transfer. If a hard data CRC error is encountered, the bad data is transferred, followed by a single byte of value 1 tagged with EOI. If a D bit is encountered, the ID field couldn't be found, the ID field was bad, or the Data Mark was bad, a single byte of value 1 tagged with EOI is transmitted to the host.

The target address is incremented for each good sector whether the host accepted the entire sector or not. If the data was bad, or couldn't be found, the target address points to the bad data and no more reads are performed.

If the target address is incremented into an invalid address, the command execution stops and a byte of value 1 tagged with EOI will be transmitted to the host. No error bits are set. This method is valid for terminating an Unbuffered Read.

The unbuffered read actually uses the internal buffer to store the data. The protocol is unbuffered in that the parallel poll response is not used to indicate when data is available. There is a pause in data flow to the HP-IB each time the buffer is refilled from the disc. This pause occurs at the beginning of the read and after every sector has been transferred. Depending on when the read is started and the sector interleaving, this pause may be up to 30 milliseconds.

Effect on status,

No errors:

S1 - 0
Stat 2 - Unchanged
DSJ - 0.

Requirements for execution:

The requirements for execution are identical to those of the Buffered Read command. See Buffered Read command.

Variation from 9895A:

The 09133-69514 controller always uses sectors with 256 bytes; the 9895A in IBM format can have sectors with 128 bytes.

The 9895A transfers the data if a D bit is encountered. Because of the way the WD1010 works, the 09133-69514 controller does not get any data and would have to pass dummy bytes. We send one byte tagged with EOI.

Variation from the HP OEM Controllers:

For a read of a target address which is not allowed, the HP OEM Controllers sets the D bit and sets S1 to 11H. We set the C,A,* bits and set S1=1FH.

Unbuffered Read Verify and Send Data

HP-IB Sequence,

Unbuffered Read Verify command:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 1 0 0)	ATN	Secondary
	PPD	
(0 0 0 0 0 1 0 1)		Opcode for Unbuffered Read Verify.
(X X X X U U U U)	EOI	Unit number
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

where: UUUU is the unit number.

Send Data command:

(P 1 0 A D D R S)	ATN	Primary talk
(P 1 1 0 0 0 0 0)	ATN	Secondary for Send Data
	PPD	
...		First read being performed
- X X X X X X X X -		Data is in buffer
		Data bytes being sent to host
- X X X X X X X X -		...
		The 256th byte
	...	Next read being performed
		Data is in buffer

this process continues

- X X X X X X X X -		Data bytes being sent to host
- X X X X X X X X -	EOI	...
	PPE	Last data byte
(P 1 0 1 1 1 1 1)	ATN	Unbuffered Read Verify is done
		Untalk.

Description:

This command is identical to Unbuffered Read and Send Data.

Unbuffered Write and Receive Data

HP-IB Sequence,

Unbuffered Write command:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 0 0 0)	ATN	Secondary
	PPD	
(0 0 0 0 1 0 0 0)		Opcode for Unbuffered Write
(X X X X U U U U)	EOI	Unit Number
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

where: UU is the Unit Number.

Receive Data command:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 0 0 0 0)	ATN	Secondary
	PPD	
(X X X X X X X X)		Data bytes
	.	.
(X X X X X X X X)		256th Data Byte
	.	Writing the first sector
	.	Write complete
(X X X X X X X X)		More data bytes
	.	.

The process of receiving data and writing to the disc continues

(X X X X X X X X)	EOI	Last data byte
	.	Last sector is written to disc
	.	.
	PPE	PPE after all writing completed
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

Description:

The Unbuffered Write allows more than one sector to be transferred from the bus controller to the disc using a single HP-IB command sequence.

To perform an Unbuffered Write requires that the Unbuffered Write Command be given, followed by the Receive Data command. This sequence must be followed or an I/O program error results. After the Unbuffered Write command, only a Receive Data command will be accepted.

The 09133-69514 controller accepts bytes over the bus. When it has received 256 bytes, it writes these to the disc, increments the target address, and accepts some more from the host. This is continued until one of the following happens:

1. The 09133-69514 controller receives a byte tagged with an EOI (or other termination condition)

2. The write can't be performed because the ID field couldn't be found or there was some other error making it impossible to do the write; the target address will remain pointing to the defective sector; status is set appropriately and the remaining data is accepted from the host but not written to the disc.
3. The target address points to a non-existent cylinder; Status is set to show an error and the remaining data is accepted from the host but not written to the disc.

If only a partial sector is received when the host terminates the transfer, the remaining bytes in the sector are filled with zeros.

As in the Unbuffered Read, Unbuffered Write actually uses the internal buffer of the controller. The protocol is unbuffered in that the parallel poll is not used to indicate when data may be sent to the 09133-69514 controller. There is a pause in the data flow to the 09133-69514 controller each time the buffer is written to the disc. The pause occurs after each sector is transferred. Depending on when the write starts and the interleave, this pause may be up to 30 milliseconds long.

Effect on status,

No errors:

S1 - 0

Stat 2 - Unchanged

DSJ - 0.

Requirements for execution:

The requirements for execution are identical to those of a Buffered Read; see the Buffered Read and Send Data command.

Variation from 9895A:

No IBM format with 128 byte sectors is possible with the 09133-69514 controller.

Variation from the HP OEM Controllers:

None.

Universal Clear

HP-IB Sequence:

(P 0 0 1 0 1 0 0)	ATN	Universal clear
	PPD	
...		Clear operations done here
	PPE.	

Description:

The Universal Clear places the controller into a known state; the following operations are performed -

HP-IB address is updated from the switches

The 8291A chip is reset and initialized

All drives are recalibrated to physical track zero

The target address is set to cylinder 0, head 0, sector 0 for all units
Status is updated as described below

The First Status bits are cleared; this is done for compatibility with Colorado Springs drivers

The current unit is set to zero.

Effect on status:

S1 - 0

Stat 2 - Clear A,C,E,F for all units

DSJ - 0.

Requirements for execution:

None.

Variation from 9895A:

9895A does not clear first status.

Variation from the HP OEM controllers:

The 9134A does not update the HP-IB address switches during a Clear command; the only way to update them is to cycle the power.

Verify

HP-IB Sequence:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 0 1 0 0 0)	ATN	Secondary
	PPD	
(0 0 0 0 0 1 1 1)		Opcode for Verify
(X X X X U U U U)		Unit Number
(X X X X X X X X)		MSB sector count
(X X X X X X X X)	EOI	LSB sector count
	.	Doing verify during this time
	PPE	Verify completed
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

where: UUUU is the unit number.

Description:

The Verify command is a read which does not transfer data to the HP-IB. This is useful for performing a surface analysis of the disc or checking the integrity of the data of the disc.

Starting with the target sector, consecutive sectors are read until any of the following occurs:

Sector count given in command expires

A seek or read error occurs

A sector marked “defective” is detected

The end of the unit is reached.

Parallel poll response is re-enabled upon completion of the verify. If an error was detected , the target address points to the sector in which the error occurred. Otherwise, the target address points to the sector following the last sector read.

The sector count is a 16-bit unsigned binary number. It can be any value and is not checked for bounds. If it is too large the verify stops when we reach the maximum target address. If the count is zero, the entire disc is verified.

Auto-incrementing into an out-of-bounds cylinder does not result in an error.

Effect on status,

No errors:

S1 - 0

Stat 2 - Unchanged

DSJ - 0.

Requirements for execution:

The correct number of parameter bytes must be received

The selected unit must be attached and formatted

DSJ not 2

First status bit not set for selected unit

The target address (Cylinder, head, and sector) must be valid for the configuration.

Variation from 9895A:

The 9895A does the reads with reduced margin which is not possible with the WD1010. To simulate reduced margin, the 09133-69514 controller reports a hard CRC error on a sector if it takes too many retries to get the data.

Variation from the HP OEM Controllers:

The HP OEM Controllers simulates reduced margin by doing the verify and allowing only errors of burst length 6 bits or less to be corrected. Normally the HP OEM controller can correct single burst errors of up to 11 bits.

Write Loopback record

HP-IB Sequence:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 1 1 1 1 0)	ATN	Secondary
	PPD	
(X X X X X X X X X)		
	.	.
(X X X X X X X X X)	EOI	1 to 9 bytes
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

Description:

The controller stores up to 9 bytes in its RAM. The last byte must be tagged with EOI. If more than 9 bytes are sent, the extra bytes are not stored.

Effect on status:

S1 - unchanged
Stat 2 - unchanged
DSJ - unchanged.

Requirements for execution:

None.

Variation from 9895A:

The number of bytes stored is not 256, as in the 9895A.

Variation from the HP OEM Controllers:

The HP OEM controllers allowed up to 12 bytes to be stored.

The 88134-69910, 09135-69515, and the 09135-69501 Controllers

This section completes the firmware description for the Microcomputer Systems Corporation (MSC) designed controllers (88134-69910, 09135-6915, and the 09135-69501). These controllers were used with the earlier 5 Mbyte Dual Platter Drives (09135-69600).

The logical configuration of this 5 Mbyte Dual drive can be either the D-code (4-Volume) or the L-Code (Single-Volume). The two types are very similar, differing primarily in the way logical units are related to the physical drive.

The D-code configurations cause a 5 Mbyte drive to appear, to the host, as a four-unit 9895A flexible disc. One physical drive is addressed as if it were four separate (and smaller) drives. The physical cylinder, sector, and head numbering of the drive being used are mapped into the cylinder, sector, and head numbering that the host would expect to see for each 9895A unit.

The controller also identifies itself to the host as a 9895A. This logical format allows hosts with existing 9895A drivers to use the Winchester drives without investing any time in writing new drivers.

The L-codes are similar to D-codes in that they also use the 9895A Amigo protocol. With L-code, however, a drive does not appear to the host to be identical to the 9895A. One physical drive becomes one logical unit, with cylinder, sector, and head numbering corresponding (usually) to the physical organization of the drive. This logical format allows 9895A drivers to be easily modified to use an L-code configuration, and allows drives of larger capacities to be used.

The following chart summarizes the differences between the various configurations.

NOTE

"Unit" refers to a logical unit, and "drive" refers to the physical disc drive. "Units per drive" is therefore the number of logically-addressed units on a single-disc drive.

The last physical cylinder is used to perform a write/read selftest, which would destroy any user data on that cylinder. For this reason, commands that read or write are not allowed to access the last physical cylinder (selftest cylinder) so that no user data can be written there. The cylinder range allowed for reads and writes is given in the table as "logical read/write cylinders." The full range of logical cylinders is available to other commands such as Format and Initialize.

	D-Code 5 Mbyte Dual Platter	L-Code 5 Mbyte Dual Platter
Identify bytes	00H, 81H	01H, 06H
Max. number of drives supported	1	1
Units per drive	4	1
Physical cylinders per drive	0 to 152	0 to 152
Logical cylinders per unit	0 to 76	0 to 152
Logical read/write cylinders per unit	0 to 75	0 to 151
Selftest cylinder, logical (each unit)	76	152
Selftest cylinder, physical	152	152
Physical heads	4	4
Logical heads	2	4
Physical sectors per track	32	32
Spare sectors per track	2	1
Usable sectors per track	30	31
Address mapping required?	yes	no

Address Transformations

The host addresses a particular sector with a unit number, a cylinder number, a head number, and a sector number. This logical address for a sector is identical to the physical address only for configurations in which each disc drive corresponds to a single logical unit, and in which the logical and physical ranges for cylinder, head, and sector numbers are the same.

D-Code Dual Platter Transformations

The 5 Mbyte Dual Platter hard disc used in the D-Code configuration has 153 cylinders, 4 heads, and 32 sectors per track. It is made to appear to be a 9895A which has four units, each having 77 cylinders, 2 heads, and 30 sectors per track. A command to access a unit, cylinder, head, and sector of the (logical) 9895A is mapped into a cylinder, head, and sector of the (physical) 5 Mbyte Dual Platter drive.

Note, for each unit, the 9895A cylinder number 76 maps into the last physical cylinder of the drive (152 on the 5 Mbyte Dual Platter). These cylinders are used for the write/read selftest, and the host is prevented from using them for data.

The following formulas map logical 9895A addresses into physical address.

Cylinder:

5 Mbyte Dual Platter cylinder = $38 * (\text{unit number}) + (9895\text{A cylinder})/2$
 if 9895A cylinder is even,
 OR $38 * (\text{unit number}) + (9895\text{A cylinder}-1)/2$
 if 9895A cylinder is odd

Head:

5 Mbyte Dual Platter head = 0 if 9895A head = 0 and unit number is even
 = 1 if 9895A head = 1 and unit number is even
 = 2 if 9895A head = 0 and unit number is odd
 = 3 if 9895A head = 1 and unit number is odd

Sector:

No transformation is required for sector numbers.

The following table shows this mapping.

Logical (9895A)			PHYSICAL (5 Mbyte Dual Platter)	
UNIT	HEAD	CYLINDER	HEAD	CYLINDER
0	0	0	0	0
0	1	0	1	0
		0	2	0
0	1	1	3	0
...
0	0	74	0	37
0	1	74	1	37
0	0	75	2	37
0	1	75	3	37
0	0	76	0	152
0	1	76	1	152
1	0	0	0	38
1	1	0	1	38
1	0	1	2	38
1	1	1	3	38
...
1	0	74	0	75
1	1	74	1	75
1	0	75	2	75
1	1	75	3	75
1	0	76	2	152
1	1	76	3	152
2	0	0	0	76
2	1	0	1	76
2	0	1	2	76
2	1	1	3	76
...
2	0	74	0	113
2	1	74	1	113
2	0	75	2	113
2	1	75	3	113
2	0	76	0	152
2	1	76	1	152
3	0	0	0	114
3	1	0	1	114
3	0	1	2	114
3	1	1	3	114
...
3	0	74	0	151
3	1	74	1	151
3	0	75	2	151
3	1	75	3	151
3	0	76	2	152
3	1	76	3	152

L-Code Dual Platter Address Transformation

The Dual Platter configuration uses identical logical and physical addresses. The 5 Mbyte Dual Platter has 153 cylinders and 4 heads. The following shows the mapping used:

LOGICAL (5 Mbyte Dual Platter)	
HEAD	CYLINDER
0	0
1	0
2	0
3	0
0	1
1	1
2	1
3	1
0	2
1	2
...	...
0	151
1	151
2	151
3	151
0	152
1	152
2	152
3	152

Initiate Selftest

HP-IB Sequence:

(P 0 1 A D D R S)	ATN	Primary listen
(P 1 1 1 1 1 1 1)	ATN	Secondary
	PPD	
(C C C C C C C C)		Cylinder
(X X X X W X X X)	EOI	Control
	PPE	
(P 0 1 1 1 1 1 1)	ATN	Unlisten.

Description:

This command gives the user the capability to remotely initiate the selftest. The selftest results may be read back using the Read Selftest Results command. Selftest takes approximately 7 seconds to complete.

Two bytes are sent following the selftest secondary and contain the following information:

The first byte contains the cylinder to be tested and is only pertinent if the W bit is set in the second byte of the command; the W bit is interpreted as follows:

- 0- No write/read test performed,
- 1- The write/read test is performed on the designated cylinder.

If the write/read test is selected, all data on the selected cylinder is lost; if the write/read test is not selected, the controller verifies cylinder 0, sector 0 of all units.

After the execution of the selftest, the controller is in the same state as a power-on condition would leave it. Selftest clears the Stat 1 bytes for all units. Also, the first status bits are set for all units. If, during the verify, the controller determines that the drive is unformatted, it sets the appropriate Stat 2 bytes for unformatted status. This status only changes if a Format command is issued to that particular unit. If the verify determines that the drive is formatted, but at some later time detects an unformatted drive (assuming that the controller isn't powered down or reset), the controller sets the E-bit in stat 2, but does not set the TTTT bits to "unformatted status". The only command that resets this status is the Format command. Other commands can be executed if this bit is set, but they will not reset the E-bit upon completion.

The selftest write test reformats the selected test cylinder. This reformatting destroys data and alternate sector assignments on the selected cylinder. After the write test is performed, the user should seek back to the test cylinder, and use the Initialize command with the D-bit set; repeating for all heads. This restores any alternate sector assignment. The Power Up Selftest and Initialize Selftest are the only commands which can return the Unknown Format status.

Effect on status,

No errors:

S1 - 0

Stat 2 - Cleared, the bits E, F, C, and * set, if appropriate

DSJ - 2.

Errors during test:

S1 - Cleared

S2 - Cleared, the bits E, F, C, and * set, if appropriate.

Error during write/read test:

Target address left pointing at sector in which error occurred; the drive is then recalibrated.

Illegal cylinder number:

S1 - Drive attention

Stat 2 - Bit C and A are set

DSJ - 1.

The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

Read Selftest Results

HP-IB Sequence:

(P 1 0 A D D R S)	ATN	Primary Talk
(P 1 1 1 1 1 1)	ATN	Secondary
	PPD	
(E H U U F 0 0 0)		Selftest Results
(M O D - S T A T)	EOI	Module Status
	PPE	
(P 1 0 1 1 1 1 1)		Untalk.

where:
 E - Error bit - If on, then an error has occurred
 H - Head number - Indicates which head the read or write test failed on
 UU - Unit number - Indicates which unit was selected when the error occurred
 F - Format of operation - Indicates HP (1) operation at the time of failure.

Description:

The controller returns the results of the last selftest it has performed. This is useful after the Initiate Selftest command or after the controller has been powered on (it performs a selftest at power-on). After receiving the selftest secondary, the controller makes two bytes of the selftest results available. The second byte is tagged with an EOI. The first byte is only valid if the preceding command was the Initiate Selftest command or if the controller was just powered up. The module status byte is always available by reading selftest results without preceding the command with an Initiate Selftest command, and module status contains the status of the last disc-oriented command executed.

Module Status (MOD-STAT)

Hexadecimal Code	Meaning
00	No error
01	Invalid command from controller processor
02	Drive not ready
03	Seek timeout (2 seconds)
04	Invalid track 00 indication from disc drive
05	All ID fields bad on track
06	Target sector not found
07	No sector found and ID ECC error on target sector
08	Position error (seek error)
09	Defective module or support signals
0A	Drive fault active
0B	Index/Sector timeout
0C	Command parameter error from controller processor
0D	Uncorrectable ECC error
** 1X	Correctable ECC error
20	Write alternate error
21	Invalid alternate sector assignment
22	Alternate already assigned
23	Direct access to alternate sector
24	Defective processor
25	Defective buffer memory
26	Defective ECC circuitry
27	Defective program memory
28	Illegal sector pulse during diagnostic
29	Illegal interleave table parameter
30	Module timeout (during selftest)

** X is the length of the burst error which can be 1 to B
 to note if the correction span was 1 to 11 bits.

The 09133-69508 Controller

The information in this appendix which applies to the 09133-69514 controller also applies to the 09133-69508 controller with the following exceptions:

Configurations:

The configurations which are currently supported in the 9133V/XV and 9134XV products are as follows:

Physical:	5-Mbyte Single Platter	15-Mbyte Triple Platter
Logical:		
Single volume (5)	X	
Four volume (5)	X	
Single volume (15)		X

The chart on page A-4 applies to the 5-Mbyte single and four volume configurations directly. The 15-Mbyte configuration is identical to the 10-Mbyte column for the 09133-69514 controller except that the Identify Bytes are 01H,0FH, and the physical and logical number of heads are both 6.