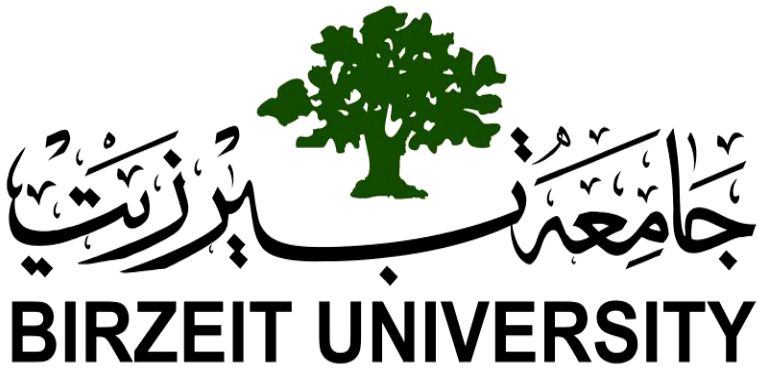

Faculty of Engineering & Technology
Electrical & Computer Engineering Department

Digital Electronics and Computer Organization Lab
ENCS 2110

Report #5

Sequential Logic Circuits

Prepared by:

Maha Maher Mali 1200746

Partners:

Lana Thabit 1200071

Jana Herzallah 1201139

Instructor: Dr. Anjad Badran
Assistant: Eng. Mohammed Bassam

Section: 6

Date: 18/5/2022

Abstract

The aim of this experiment is to understand the differences between combinational and sequential logic circuits, and the applications of various memory units. Also, to study the operating principles and applications of various flip-flops. Moreover, to understand the operating principles of counters and how to construct with JK flip-flops. Finally, to study the synchronous and asynchronous counters.

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2.Theory

2.1 combinational and sequential circuit

Digital circuits can be classified as either a combinational or a sequential circuit.

Combinational logic circuits output depends only on the input. The block diagram of a Combinational circuit is shown in Figure 1. Whereas sequential circuit Output depends on both present and past value of the input. The block diagram of a sequential circuit is shown in Figure 2.

Figure1: combinational circuit 1

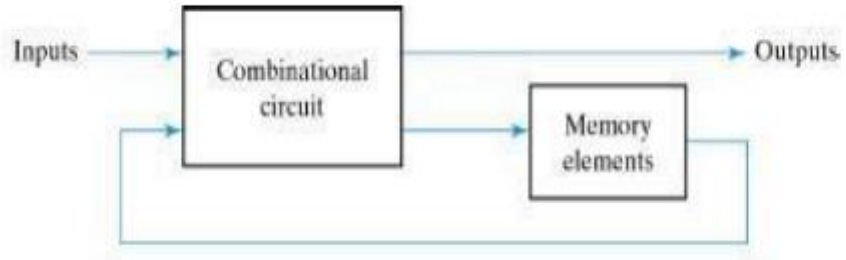


Figure2: sequential circuit 1

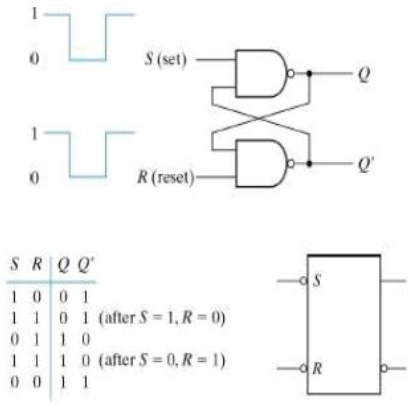
2

2.2 latches

The latch is the basic storage element of sequential logic circuits. Latches operate with signal levels and commonly used in asynchronous sequential circuits but they are not practical for synchronous sequential circuits. Latches are used to construct Flip-Flops.

A. The SR (Set-Rest) Latch

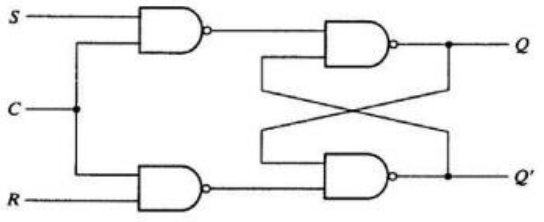
The SR latch is a circuit that is constructed using 2 cross-coupled NAND or NOR gates. It has two input the rest(R) and set(S) and two outputs (Q) and (Q') as shown in Figure 3.



S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	

Figure3: SR latch with NAND gate 3

A control input (C) can be added to the SR Latch. If C=0 the output Q will not be changed for any values of R and S but if C=1 the circuit will work normally as shown in Figure4

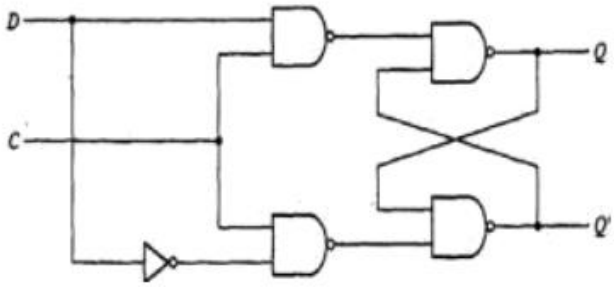


C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

Figure4: SR latch with control input 4

B. The D -Latch

The D-Latch was designed to eliminate the undefined condition of the SR Latch by eliminating one of its inputs as shown in Figure 5.



C	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state

Figure5: D -Latch 5

2.3 Flip-Flops

The Flip-Flops are used for storing binary information as Latches. But the difference is that the output change in the Flip-Flop happens only at the clock edge while in the Latch it happens at the clock level. Flip-Flops can be constructed using two separated Latches.

Figure 6 shows a D Flip-Flops implemented using two D Latches.

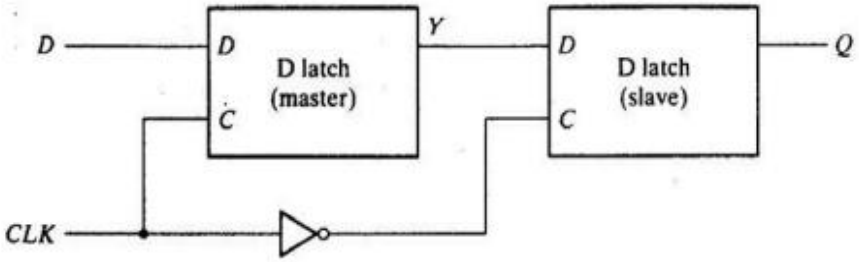


Figure6: Flip-Flop 6

The common types of Flip-Flops are D, JK and T Flip-Flops as shown in Figure 7

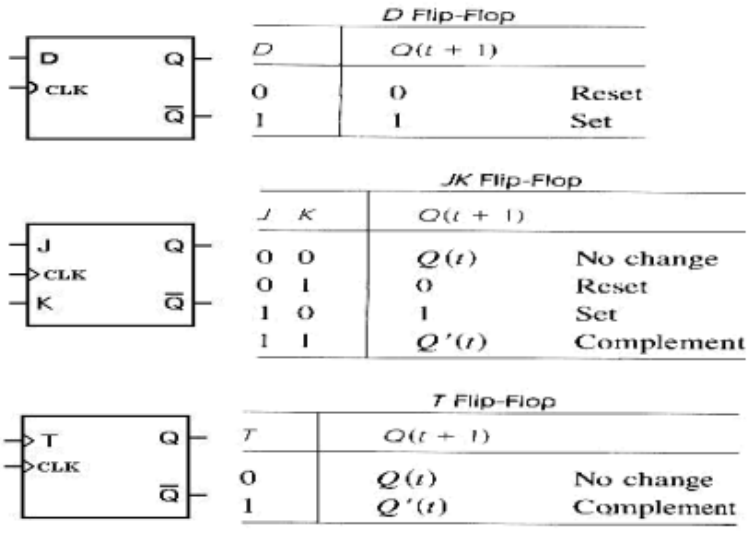


Figure7: D, JK, and T Flip-Flops 7

2.4 Registers

Registers are used to hold binary data. The register is a collection of Flip-Flops. N-bit register consists of N Flip-Flops.in registers all Flip-Flops share a common clock and they all rest together-bit register require N Flip-Flop. Figure 8

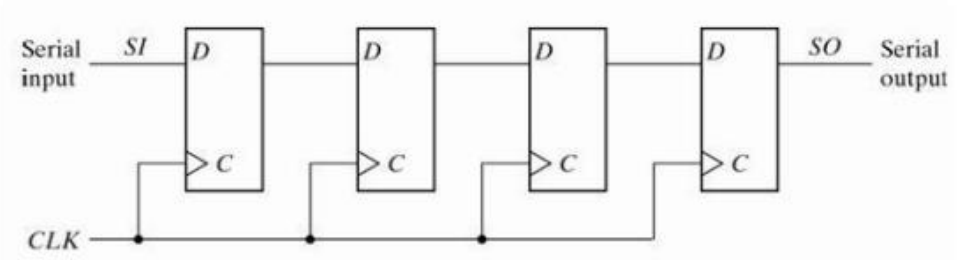


Figure8: 4-bit Register 8

Shift register is a group of cascaded Flip-Flops where the output of one Flip-Flop become the input of the next Flip-Flop ,as shown in figure 9 .

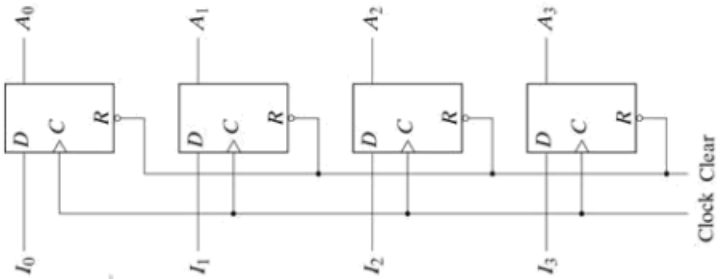


Figure9: 4-bit shift- right register 9

2.5 Counters

The counter is a special type of the registers that goes through certain sequence of states. They are mainly used to count the number of times an event happens. Counters can count up or down according to the way that Flip -Flops are connected. There are two types of counters, Asynchronous (Ripple) and synchronous counters. In ripple counters the Flip-Flops doesn't share the same clock, one Flip-Flop clock is connected to an external clock pulse and other Flips-Flops clock are triggered by the output of the previous Flip-Flop. In synchronous counters, all Flip-Flops share the same clock.

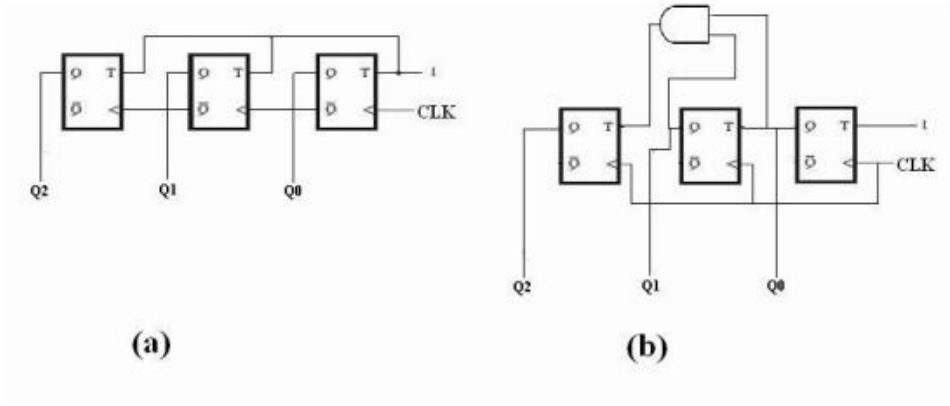


Figure10: (a) 3-bit ripple counter, (b) 3-bit synchronous counter 10

3.Procedure

3.1 Latches and Flip-Flop

A. Constructing RS latch with Basic Logic Gates

The RS latch circuit as shown in Figure 11 was connected.

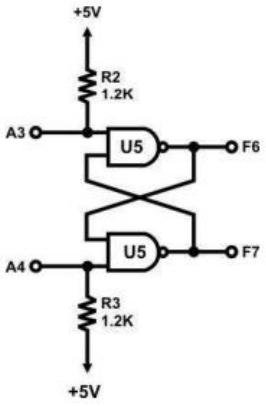


Figure11: RS latch with Basic Logic Gat 11

The inputs A3, A4 were connected to Pulser Switches SW A (TTL), SW B(TTL) respectively. And the Outputs F6, F7 were connected to logic indicators L1, L2, respectively.

The input sequences in Table 1 for A3, A4 were followed and the output

states were recorded and measured.

Table 1 RS latch with Basic Logic Gates

Input		output	
A3	A4	F6	F7
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0	1

B. Constructing RS latch with control input

The RS latch with control input circuit as shown in Figure 12 was connected.

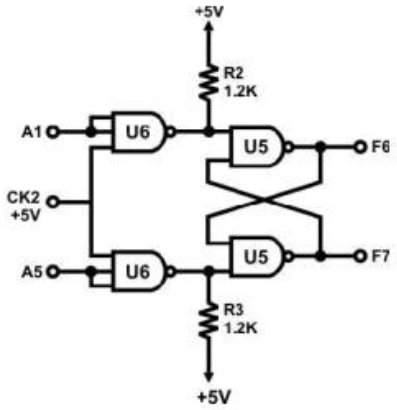


Figure12: RS latch with control input 12

The inputs A1, A5 were connected to Pulser Switches SW A (TTL), SW B(TTL) respectively. And the Outputs F6, F7 were connected to logic indicators L1, L2 respectively.

The input sequences in Table 2 for A1, A2 were followed and the output

states were recorded and measured.

Table 2 RS latch with control input

Input		output	
A1	A5	F6	F7
0	0	1	1
0	1	0	1
1	0	1	0
1	1	1	1

C. Constructing D latch with RS latch

The circuit shown in Figure 13 was connected.

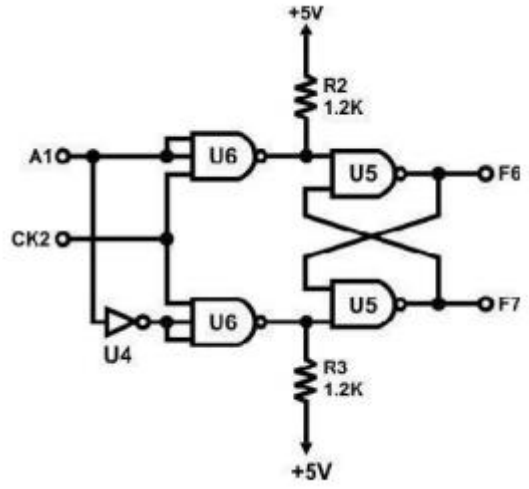


Figure13: D latch with RS latch 13

CK2 was connected to SW B. And the input A1, A5 were connected to the SW0and SW1 respectively. The output F6 was connected to the L1.

The input sequences in Table 3 for the inputs A1, A5 were followed and the output

state was recorded and measured.

Table 3 D latch with RS latch

Input		output
CK2	A1	F6
0	0	0
0	1	0
⎍	0	0
⎍	1	1

D. Constructing JK latch with RS latch

The circuit in Figure 14 shown below was connected

.

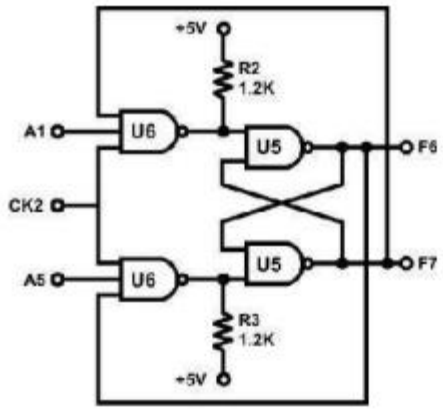


Figure14: JK latch with RS latch 14

CK2 was connected to SW B. And the input A1, A5 were connected to the SW0and SW1 respectively. The output F6 was connected to the L1.

The input sequences in Table 4 for the inputs A1, A5 were followed and the output

state was recorded and measured.

Table 4 JK latch with RS latch

input			output
CK	A1	A5	F6
⎍	0	0	0
⎍	0	1	0
⎍	1	0	1
⎍	1	1	1

E. Constructing JK Flip-flop with master- slave RS latches

The circuit in Figure 15 shown below was connected

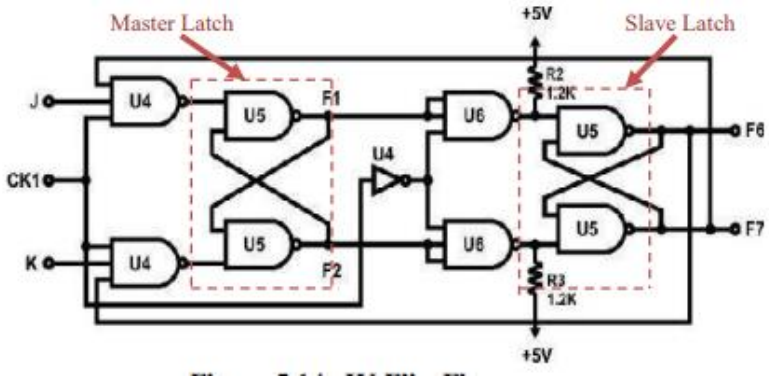


Figure15: JK Flip-flop with master- slave RS latch 15

The CK2 was connected to Pulser switch. Also, the CK1 was connected to SW A output, and J to SW1, K to SW0. The output F1, F2, F6, F7 were connected to L3, L2, L1 and L0 respectively

The input sequences in Table 5 for the inputs A1, A5 were followed and the output state was recorded and measured.

Table 5 JK Flip-flop with master- slave RS latches

input			output				states
CK	k	j	F1	F2	F6	F7	
⎍	0	0	1	0	1	0	No change
⎍	0	1	1	0	1	0	set
⎍	1	0	0	1	0	1	rest
⎍	1	1	1	0	1	0	complement
⎍	1	1	0	1	0	1	complement

3.2 Registers

A. Constructing Shift Register with D Flip-Flops

The circuit in Figure 16 shown below was connected

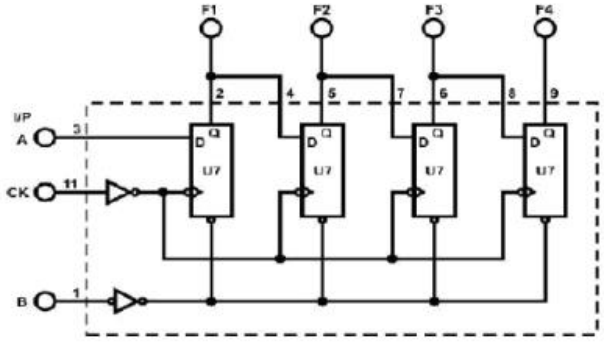


Figure16: shift register 16

Connected B (clear) to SW0, and A to SW1, CK to SW A output, F1, F2, F3, F4 to L1, L2, L3, L4 respectively. 2.

Set SW0 to "0" to clear B and then set SW0 to "1".

At A= "1", when sending a clock signal to the CLK input of Flip-Flops all outputs(F1-F4) will become 1 sequentially. F1 will become 1 first when the clock is at the high state, and F2 will become 1 at the next high state of the clock and the same happens for F3 and F4.

At A= "0", when sending a clock signal to the CLK input of Flip-Flops all outputs(F1-F4) will become 0 sequentially. F1 will become 0 first when the clock is at the low state, and F2 will become 0 at the next high state of the clock and the same happens for F3 and F4.

At A= "0", when sending a clock signal to the CLK input again all outputs will stay zero and nothing will change.

At A= "1", again and after sending a clock signal all outputs will become 1 sequentially the same way as the first time.

B. 4-Bit Shift Register with serial and parallel load

The 4-Bit Shift Register with serial and parallel synchronous operating modes, it has serial input data input (B1) and four parallel (A-D) Data inputs, and four Parallel Data outputs (QA–QD) as shown in in figure 17

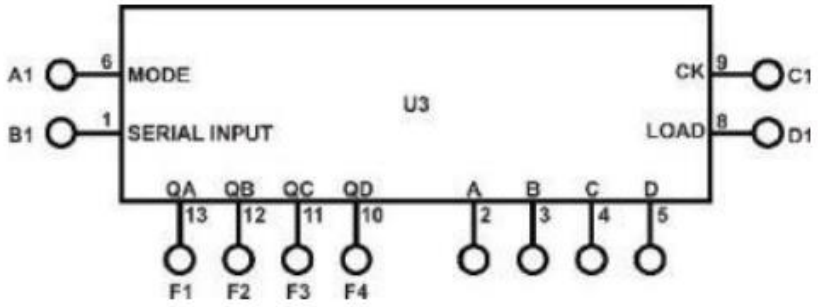


Figure17: 4-bit shift register 17

Inputs A, B, C, D were connected to logic states and outputs F1, F2, F3, F4 were connected to L3, L2, L1 and L0 respectively.

B1 (I/P) was connected to DIP2.0, and A1 (MODE) was connected to o DIP2.1

CK and load inputs were connected to 1HZ clock generator.

B1 was put to 1 state and the values of A1 in Table were followed and the outputs were recorded.

B1 was put to 0 state and the state of A1 was changed to 1 for every input in Table and the outputs were recorded and listed.

We noticed that the parallel load was enabled when A1 set to 1. And the serial load was enabled when B1 is set to 1.

3.3 counters

A) 2-bit Synchronous Counter

The IT-74147 module used to implement the 2-bit synchronous counter as shown in Figure 18. Connected CLK input to pulser switch. Also connected counter outputs Q1 and Q0 to indication lamps.

Applied clock pulses to CLK input. Then observed and recorded the output as shown in table 6.

After that we applied counter output Q1 and Q0 to seven segment display and observed and recorded the output as shown in table 7.

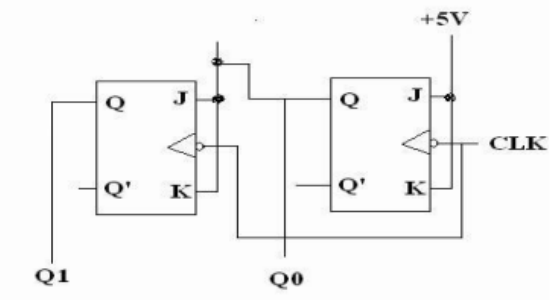


Figure18: 2-bit Synchronous Counter 18

Table 6 2-bit Synchronous Counter

CLK	Q1	Q0
⎍	0	0
⎍	0	1
⎍	1	0
⎍	1	1
⎍	0	0
⎍	0	1
⎍	1	0

	1	1

Table 7

CLK	D1
	0
	1
	2
	3
	0
	1
	2
	3

This counter counts from 0 to 3 then reset to zero then start counting again.

This counter is synchronous because the same clock is connected to all flip flops. The next value is set to the counter only when a clock is applied.

B) 3-bit (divide-by-eight) Ripple Counter

The IT-3001 module was used to implement the 3-bit (divide by eight) Ripple counter as shown in Figure 19. Connected CLK input to pulser switch. Also connected counter outputs Q2, Q1, Q0 to indication lamps.

Applied clock pulses to CLK input. Then observed and recorded the output as shown in table 8.

After that we applied counter output Q1 and Q0 to seven segment display and observed and recorded the output as shown in table 9.

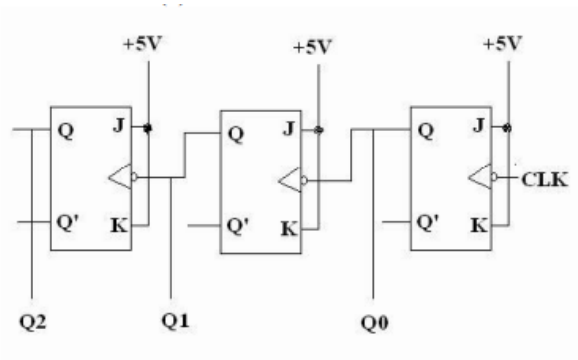


Figure19: 3-bit (divide-by-eight) Ripple Counter 19

Table 8 : 3-bit (divide-by-eight) Ripple Counter

CLK	Q2	Q1	Q0
⎍	0	0	0
⎍	0	0	1
⎍	0	1	0
⎍	0	1	1
⎍	1	0	0
⎍	1	0	1
⎍	1	1	0

	1	1	1
	0	0	0
	0	0	1

Table 9

CLK	D1
	0
	1
	2
	3
	4
	5
	6
	7
	0
	1

This counter counts from 0 to 7then reset to zero then start counting again.

This counter is asynchronous because not the same clock is connected to all flip flops. The next value is set to Q0 of the counter only when a clock is applied and other digits vary depending on the varying of previous digit.

C) BCD Counter

BCD counter was used which locate (IC 7490) on IT-3008 module.

connected C3, C4 to SW0 and SW1, D1, D2 to SW2 and SW3, F1~F4 to L1~L4, A2 to SWA A output, B2 to SWB B output.

connected F1 to B2, set C3, C4, D1 and D2 to ground and A2 to SWA A pulse as shown in Figure 20.

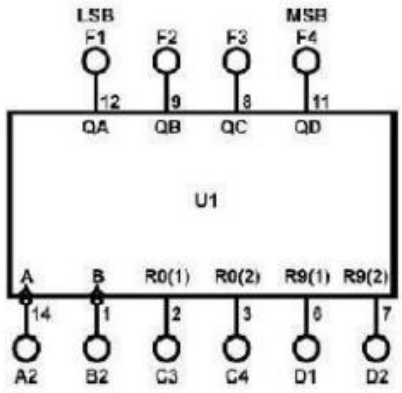


Figure20: BCD Counter 20

This counter counts from 0000 to 1001 when a clock is provided.

Discussion

1) Although latches are useful for storing binary information, they are rarely used in sequential circuit design, why?

   Ans:

   - Latches may get glitched and that's why we use Flip-flops are preferred.
   - Latches will cause race condition which leads to error in the results.
   - Latches are level triggered which means the change will happen at any change of the enable signal.

2) What is the disadvantage of the RS flip flop?

Ans:

The main disadvantage of the RS(Rest-Set) latch when the Rest and Set inputs are equal to 1 the latch makes a set and a rest at the same time which means Q=Q'=1 and this is a indetermined state because Q and Q' are always not equal.

3) What is the difference between "synchronous" and "ripple" counters?

   Ans:

   The main difference between synchronous and ripple counters is that synchronous counters are triggered with the same clock at the same time while ripple counters are triggered with different clocks and that makes synchronous counters faster than ripple counters.

Conclusion

In conclusion, we understood the sequential circuit which is the digital logic circuit in which the output depends in the input and previous output. Also, we became able to deal with different types of latches (SR and D Latches) and flip-flops (D, JK, T flip flops). And we got to know how to implement some types using other types. Also, the we knew the main difference between latches and flip-flops, which is triggering, flip-flops are edge triggering chips, while latches are level triggering chips. In addition to that, counters are an application of flip-flops, were implemented using flip-flops and ICs.

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