Faculty of Engineering & Technology Electrical & Computer Engineering Department

Digital Integrated Circuits– ENCS3330

Assignment #1

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Section: 1

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Device Sizes for All Gates

Table 1 :Device Size

Gate Name	PMOS Size	NMOS Size
Invertor	10 (Base Size)	10 (Base Size)
NAND Gate	10	30(number of NMOS x Base Size) because the NMOS in parallel connection.
NOR Gate	30(number of PMOS x Base Size) because the PMOS in parallel connection.	10
One Bit Pass Gate	10	10

Inverter

Schematic

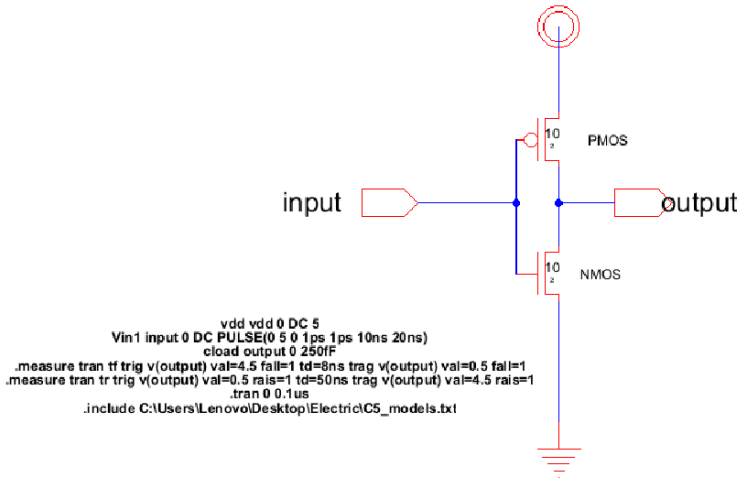

Figure 1: Invertor Schematic

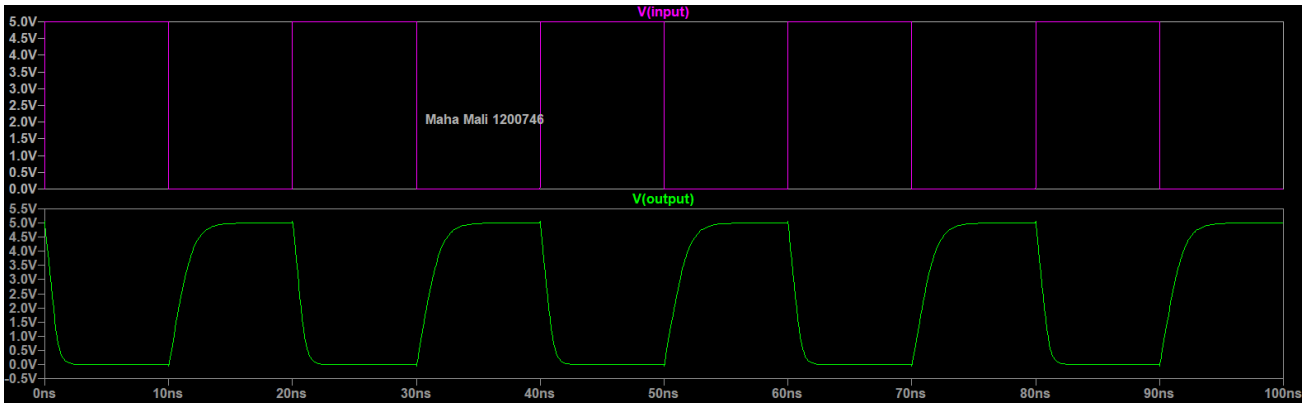

Figure 2:Invertor Schematic Simulation

Layout

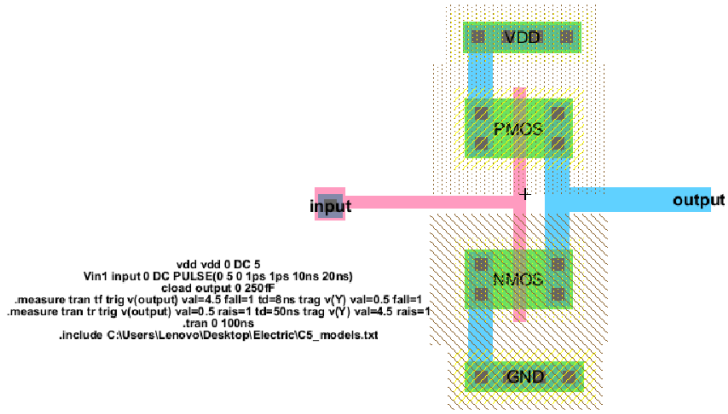

Figure 3:Invertor Layout

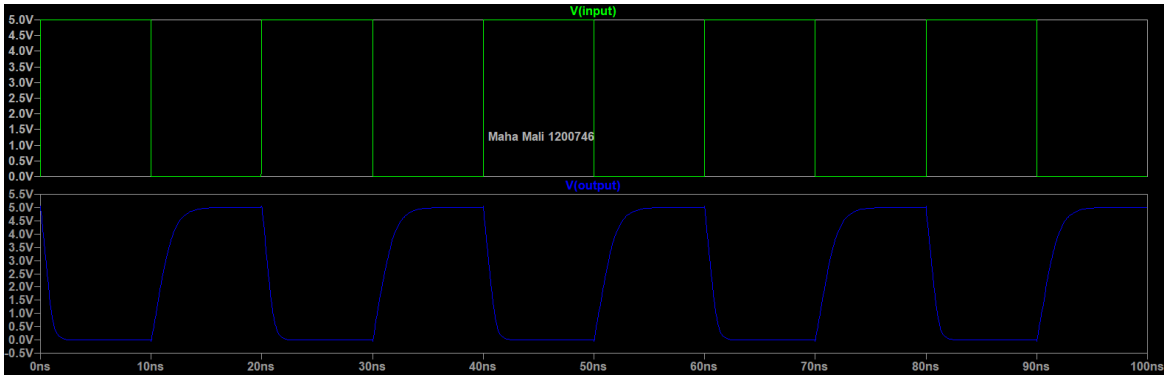

Figure 4: Invertor Layout Simulation

Discussion

From the simulation of schematic and layout, the invertor work corrects, when **the input is 0 the output is 1, also when input is 1 the output is 0**

3 Input NAND Gate
Schematic

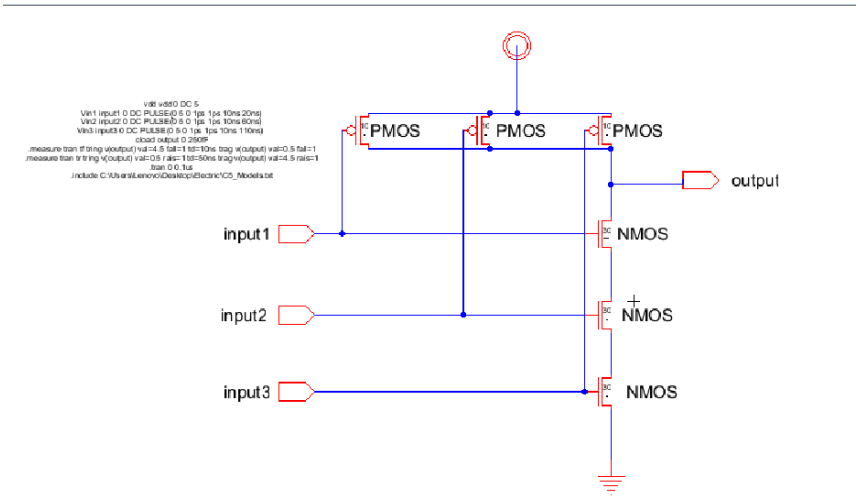

Figure 5:3- input NAND Gate Schematic

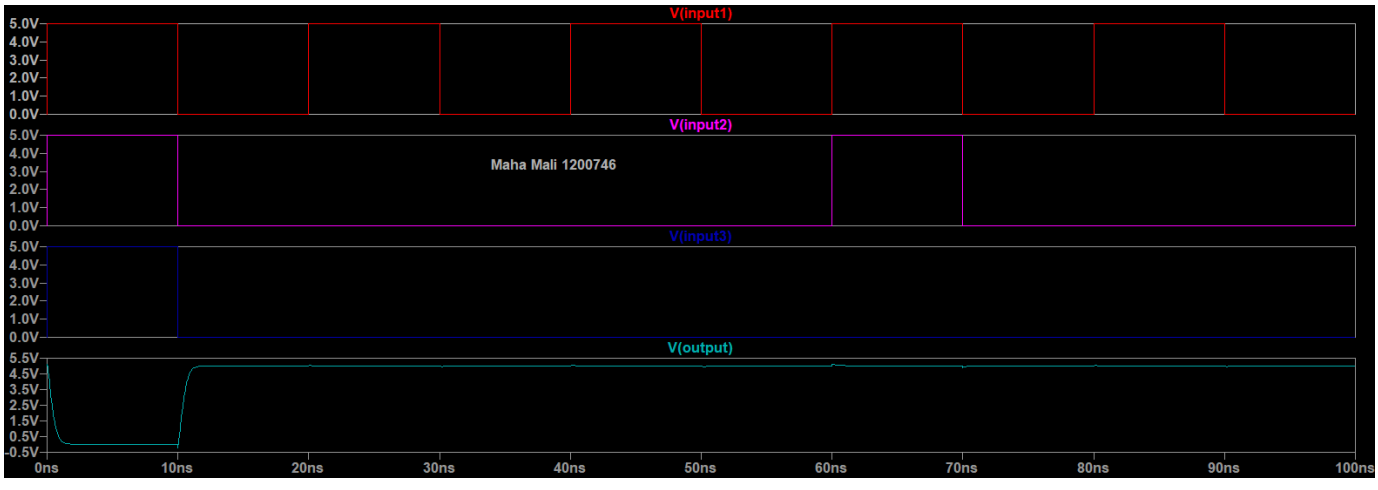

Figure 6: 3- input NAND Gate Schematic Simulation

Layout

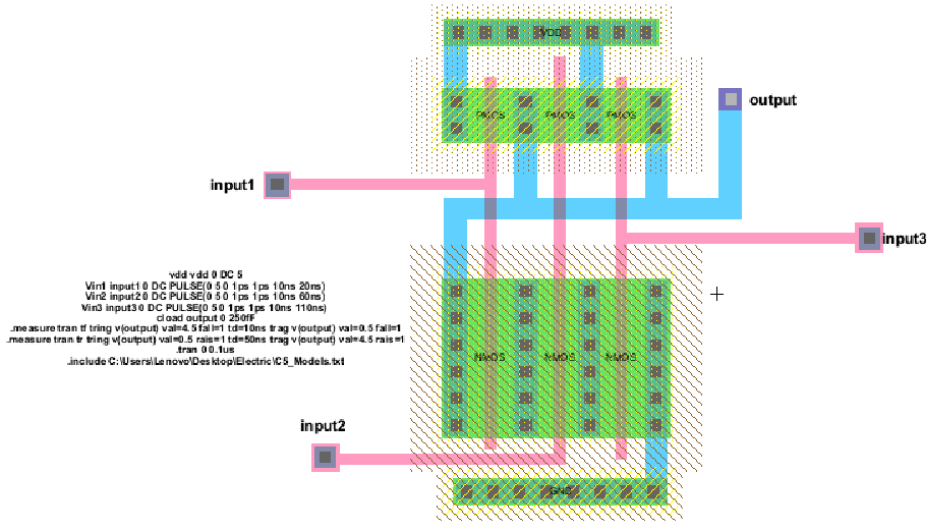

Figure 7: 3- input NAND Gate Layout

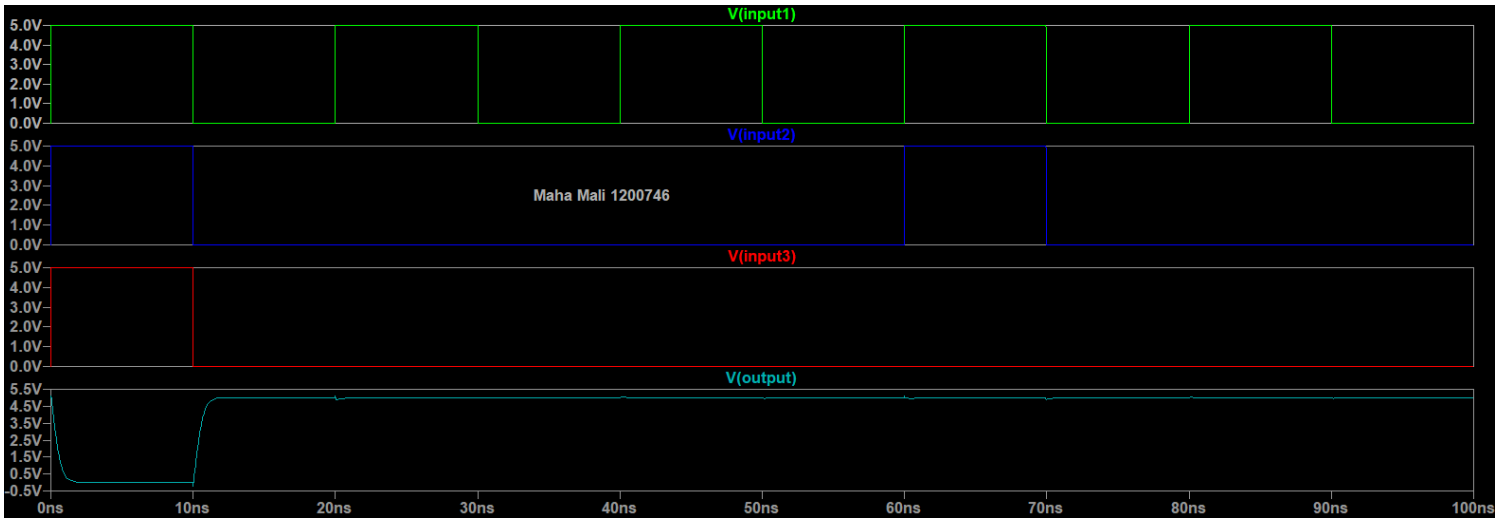

Figure 8: 3- input NAND Gate Layout Simulation

Discussion

From the simulation of schematic and layout, the 3 input NAND gate work corrects, because in NAND gate the output will be 0 in one case only when three input 111.In other input the output still be 1.

3 Input NOR Gate

Schematic

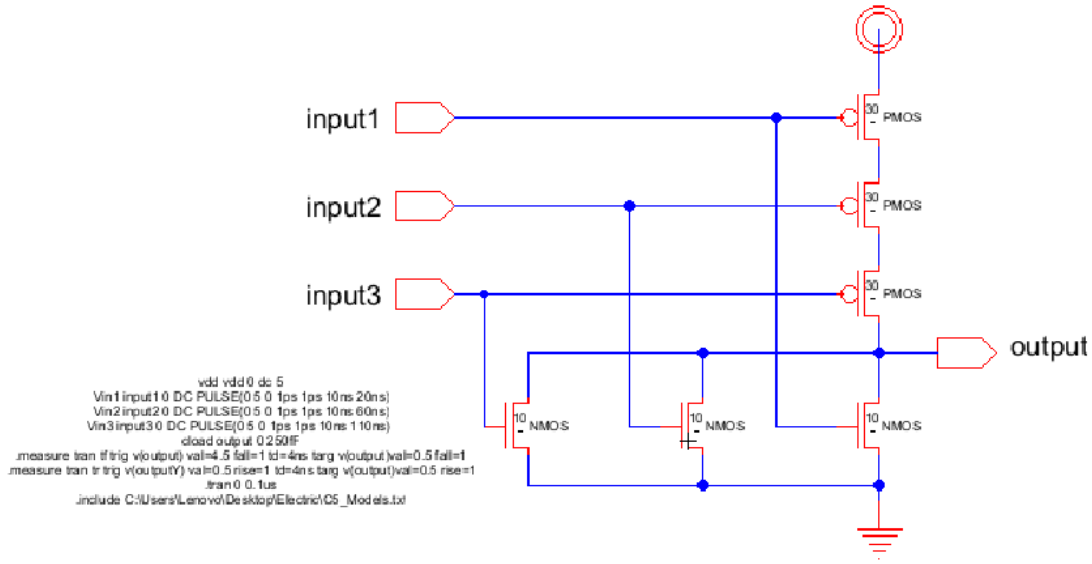

Figure 9: 3- input NOR Gate Schematic

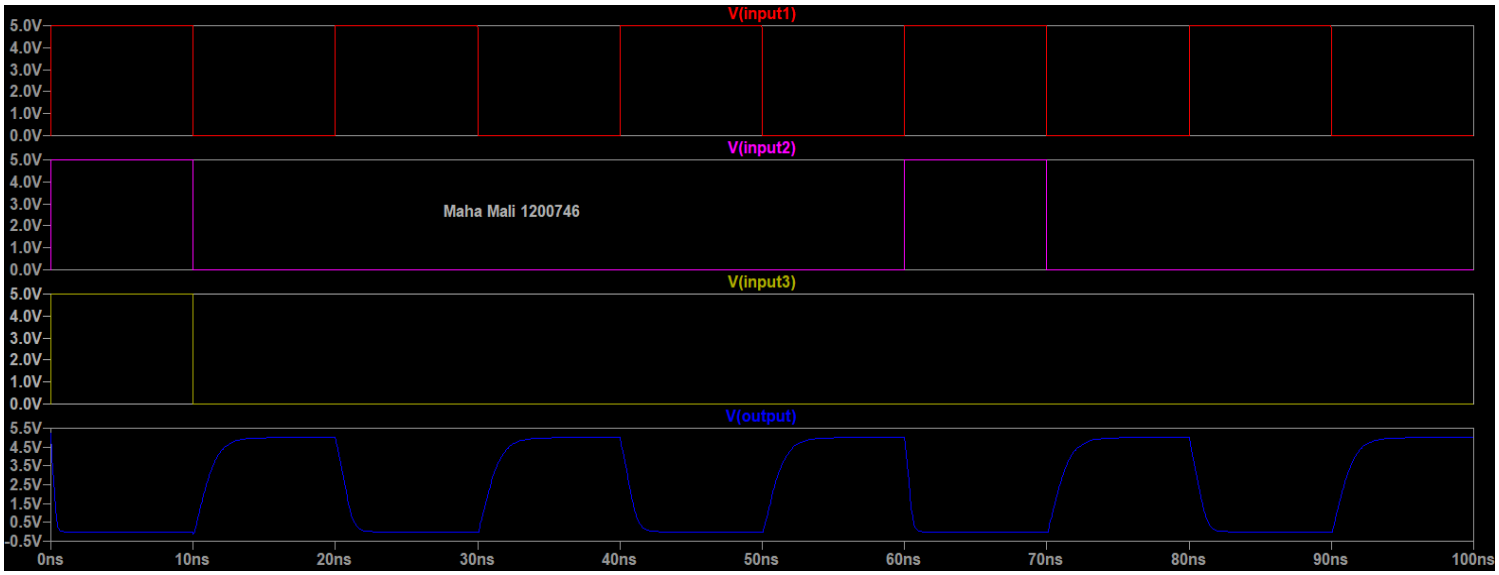

Figure 10: 3- input NOR Gate Schematic Simulation

Layout

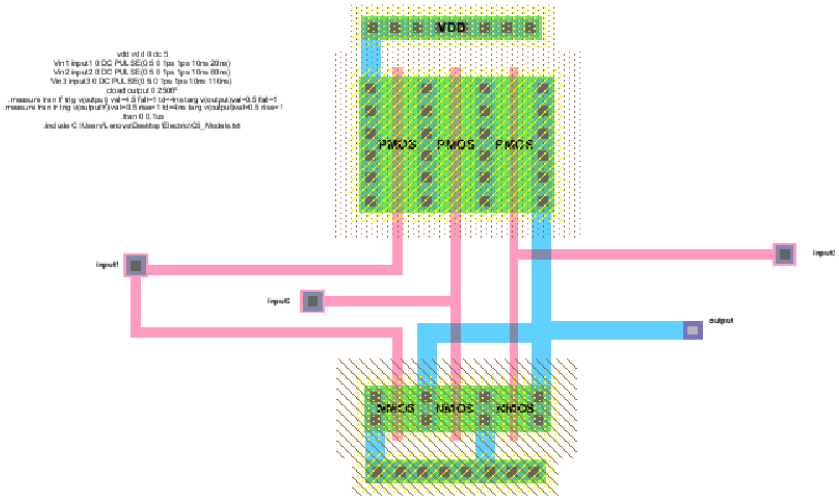

Figure 11: 3- input NOR Gate Layout

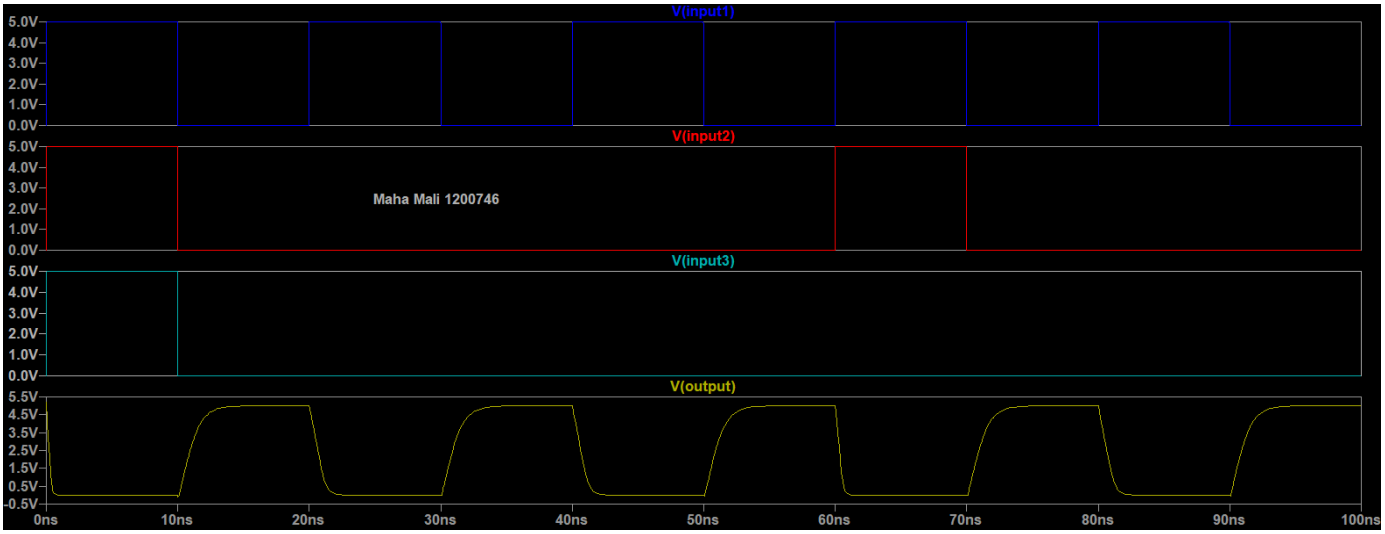

Figure 12: 3- input NOR Gate Layout Simulation

Discussion

From the simulation of schematic and layout, the NOR gate work corrects because in NOR gate the output will be 1 in one case only when three input 000.In other input the output still be 1.

One Bit PASS Gate

Schematic

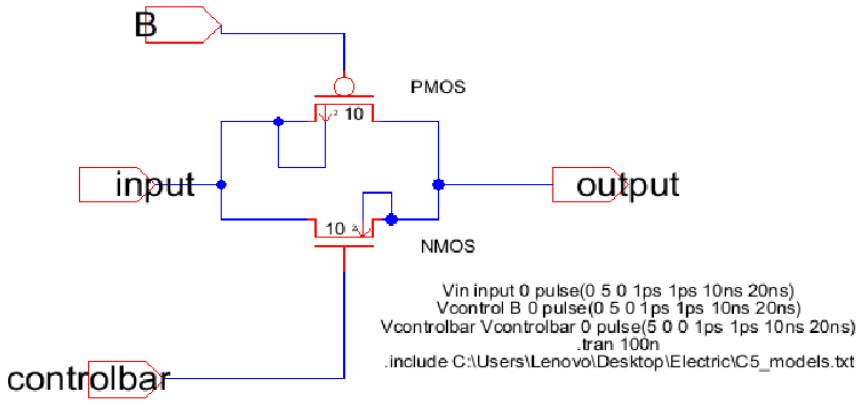

Figure 13: One bit PASS gate schematic

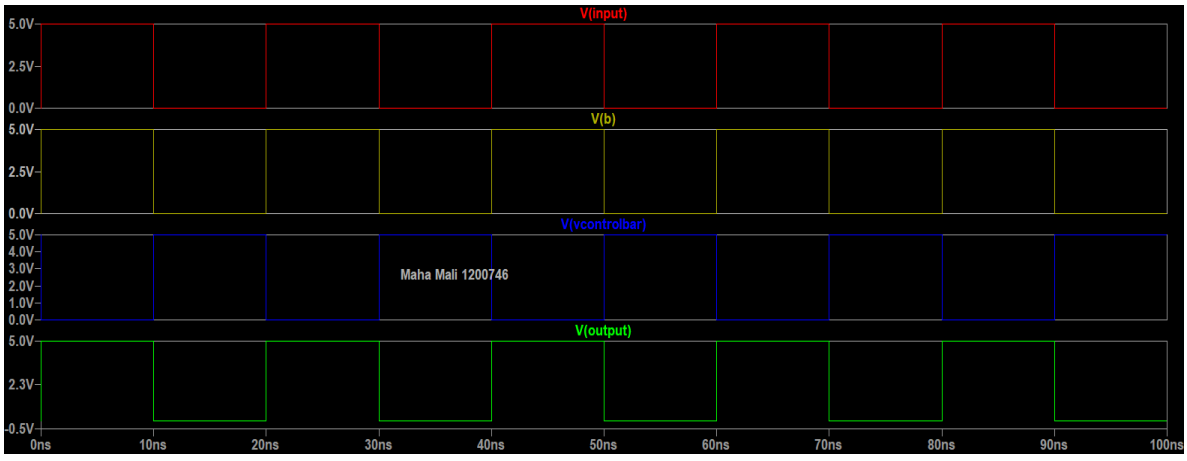

Figure 14: One bit PASS gate schematic simulation

Layout

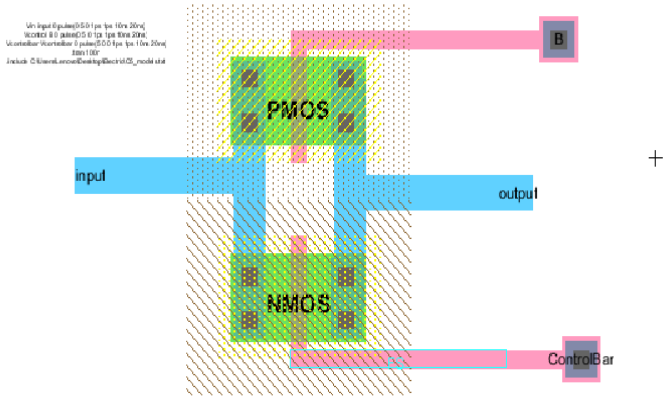

Figure 15: One bit PASS gate Layout

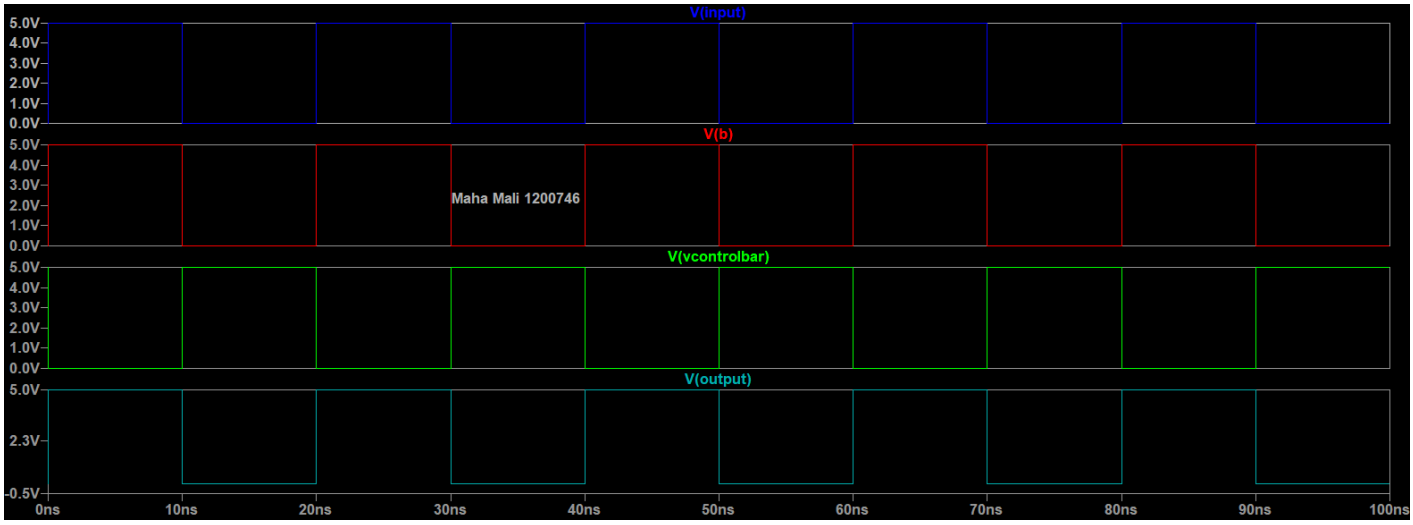

Figure 16: One bit PASS gate Layout Simulation

Discussion

From the simulation of schematic and layout, the one-bit pass gate work as buffer, which mean the output as the same of the input, so if the input is 1 the output also the 1, also if the input is 0 so the output also 0.

Report Rise and fall time

By choosing the correct size of the gates I manage to get the same rise and fall time for all gates as shown in below figure.

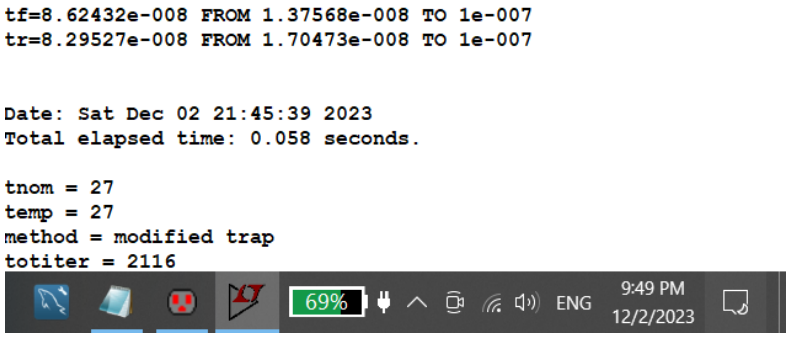

Figure 17: Rise and Fall time

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The aim when we designed the four gate is to get the equal rise and fall time for all gate.so I change the width of the transistors used specified to a certain value. In the invertor gate the width of the transistor (NMOS width = 10, PMOS width = 10) were taken as the base size for the rest of the gates. For the 3 input NAND gate, the width of the PMOS devices were the same as the base widths they are connected in **parallel**. However, the NMOS devices were set to the base width multiplied with their number which means (10*3=30) since they are connected on **series**. In the NOR gate since NMOS devices are connected in parallel (NMOS width =10) and PMOS devices are connected on series (PMOS width =3*10=30). The one-bit pass gate followed the base measurements as the inverter.