



**Faculty of Engineering & Technology Electrical & Computer
Engineering Department**

Digital Integrated Circuits– ENCS3330

Assignment #2

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Section: 1

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N-Latch

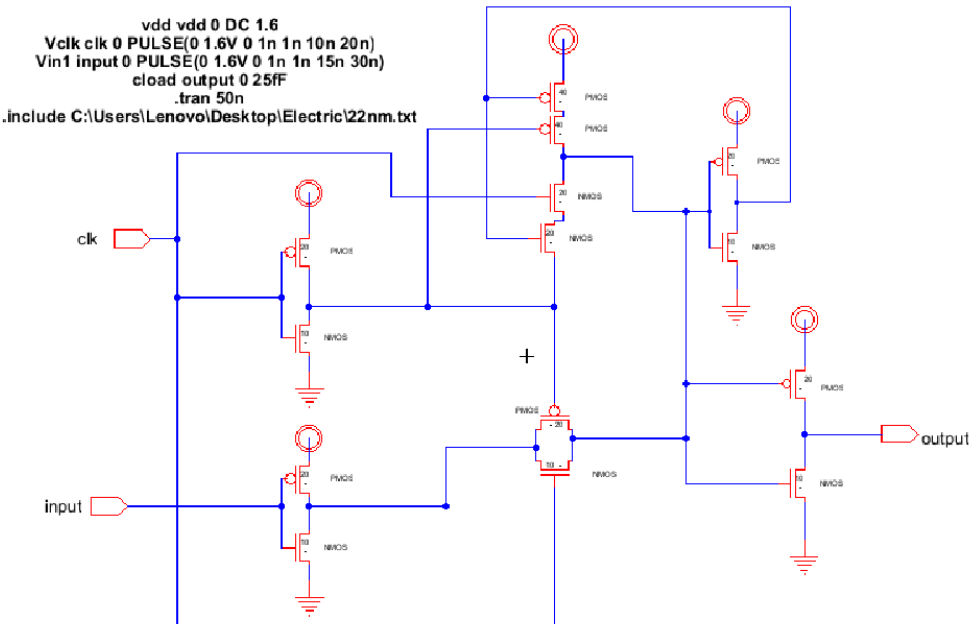


Figure 1: N-Latch Schematic

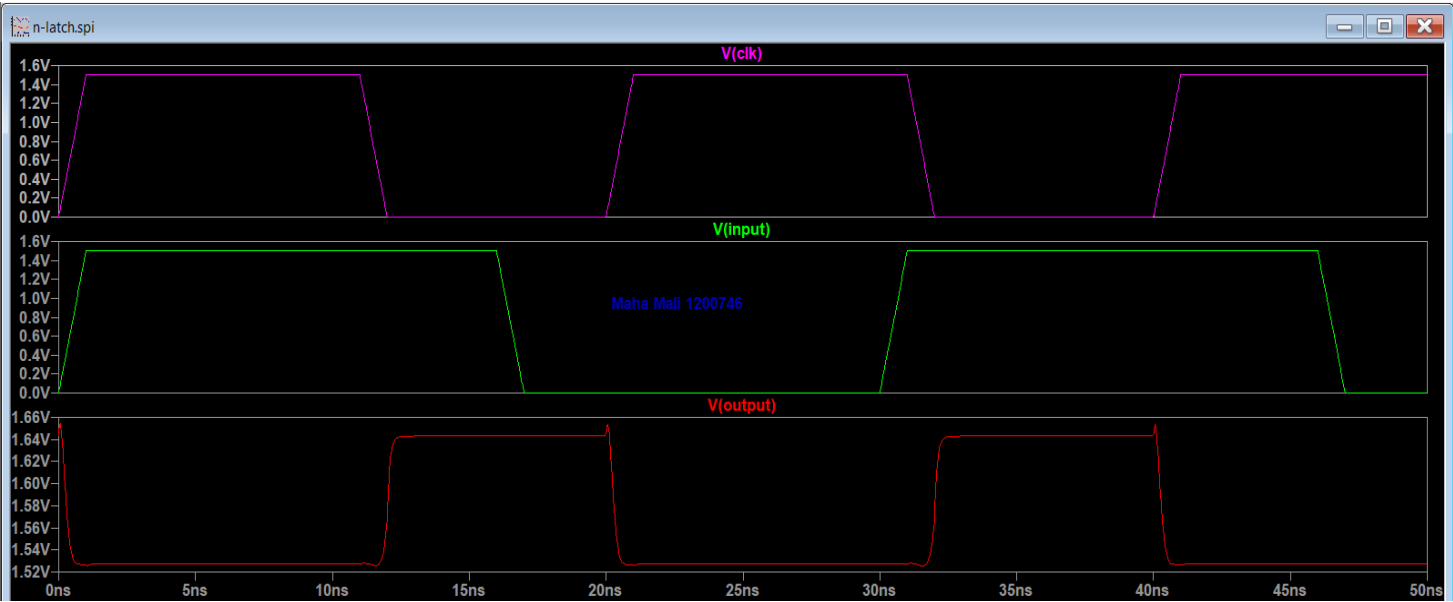


Figure 2:N-Latch Schematic Simulation

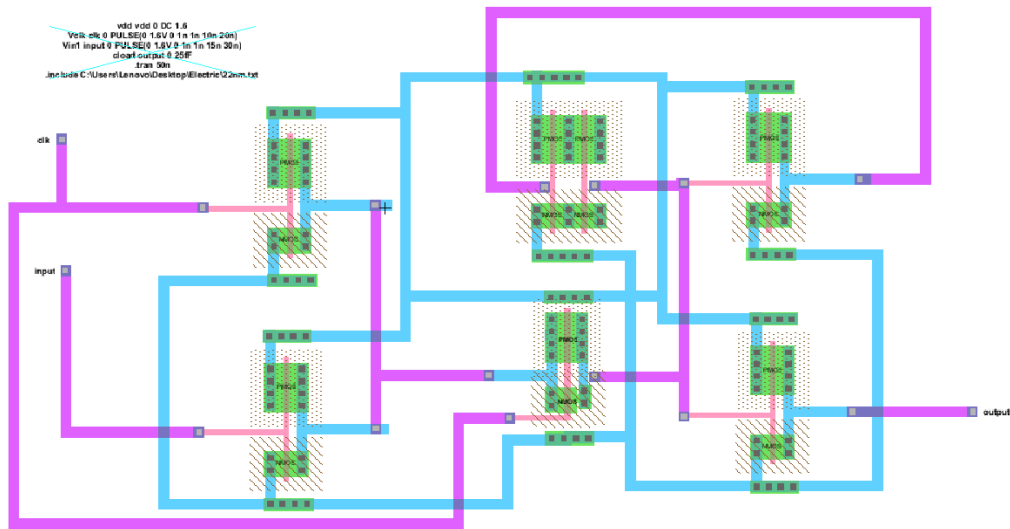


Figure 3: N-Latch Layout

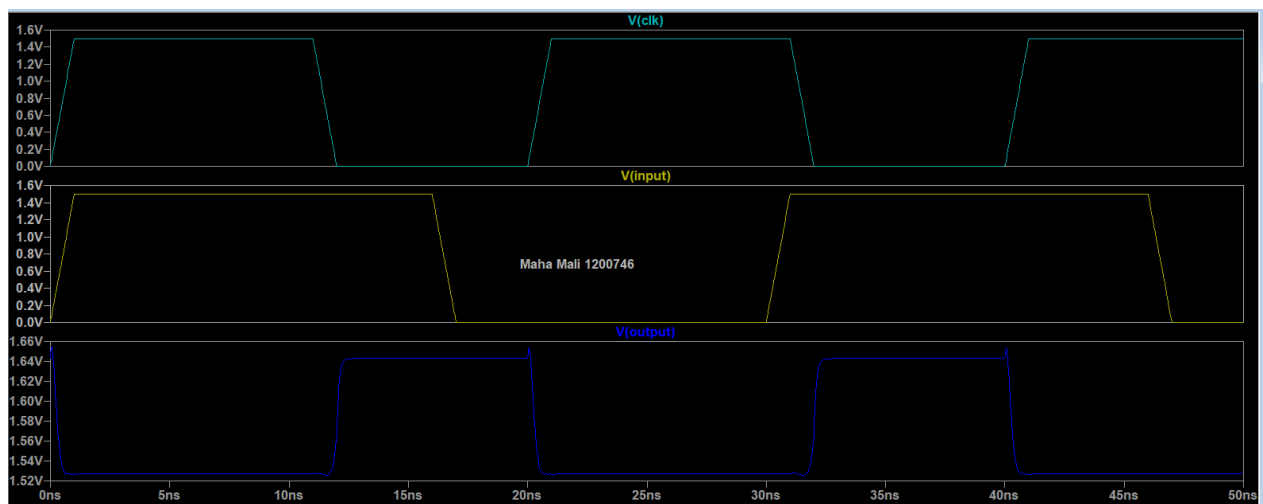


Figure 4: N-Latch Layout Simulation

```
Measurement "vin1_delay" FAIL'ed
Measurement "vout_delay" FAIL'ed
ckout_delay=1.285e-007 FROM 2.15e-008 TO 1.5e-007
Measurement "dout_delay" FAIL'ed
```

Figure 5: N-latch Measurement

Show cases when simulations failed when missing setup/hold window.

Ans: The failing case was shown on the third clock cycle when the clock it was changed from zero to one. The output should be one but it appears as zero.

P-Latch

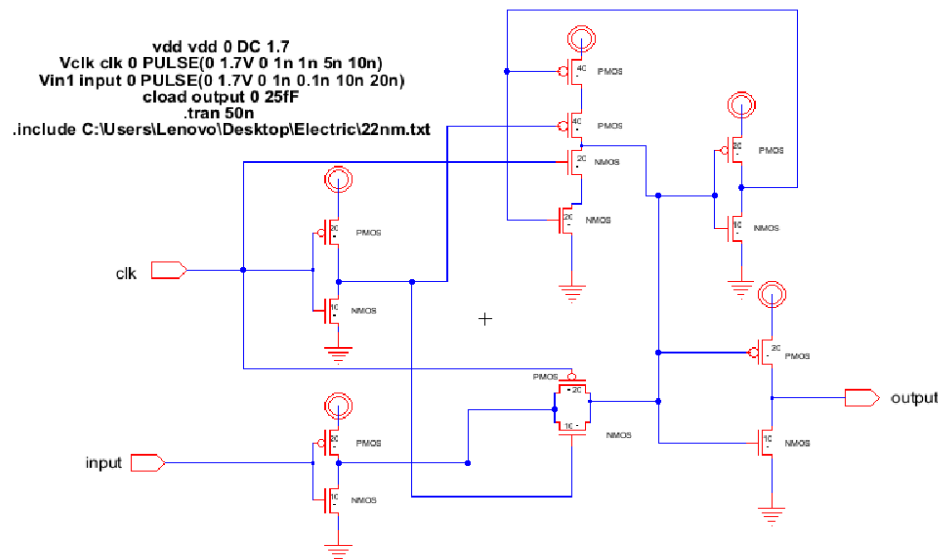


Figure 6: P-Latch Schematic

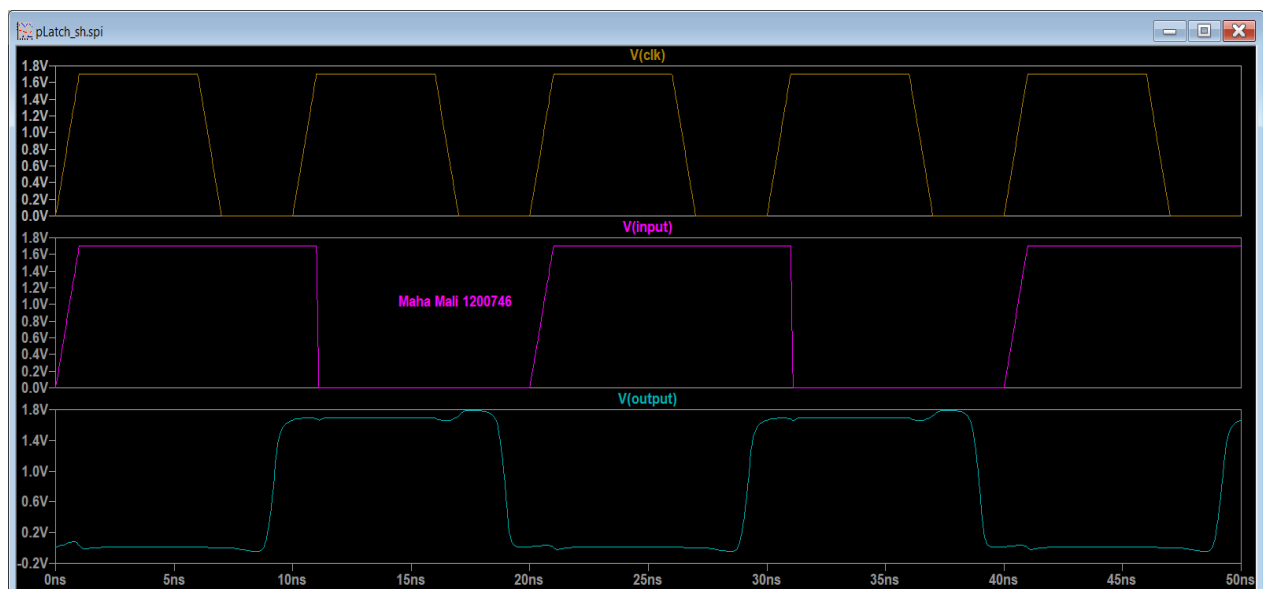


Figure 7: P-Latch Simulation

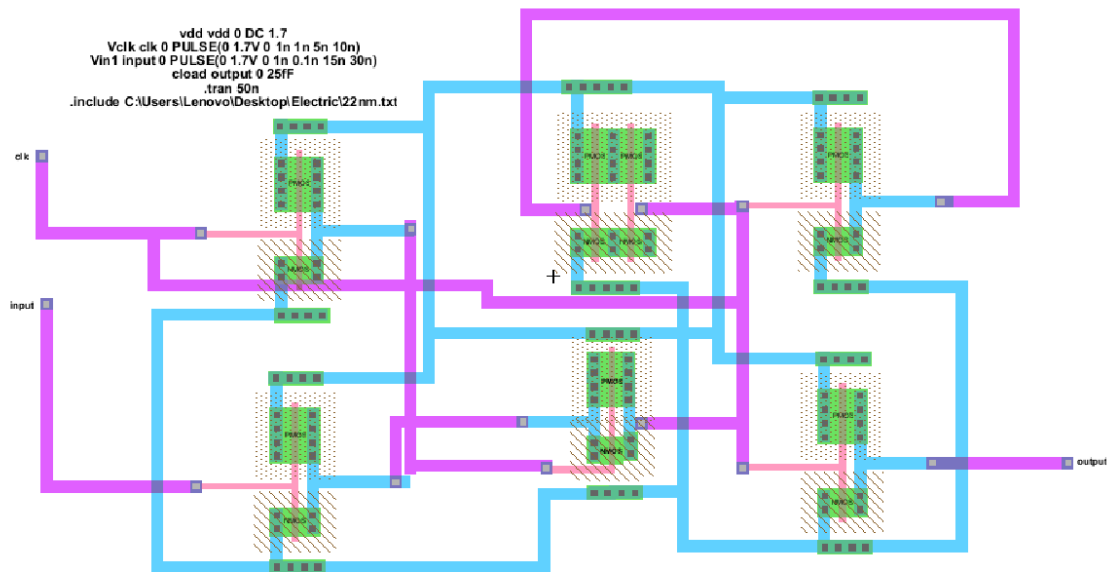


Figure 8: P-Latch Layout

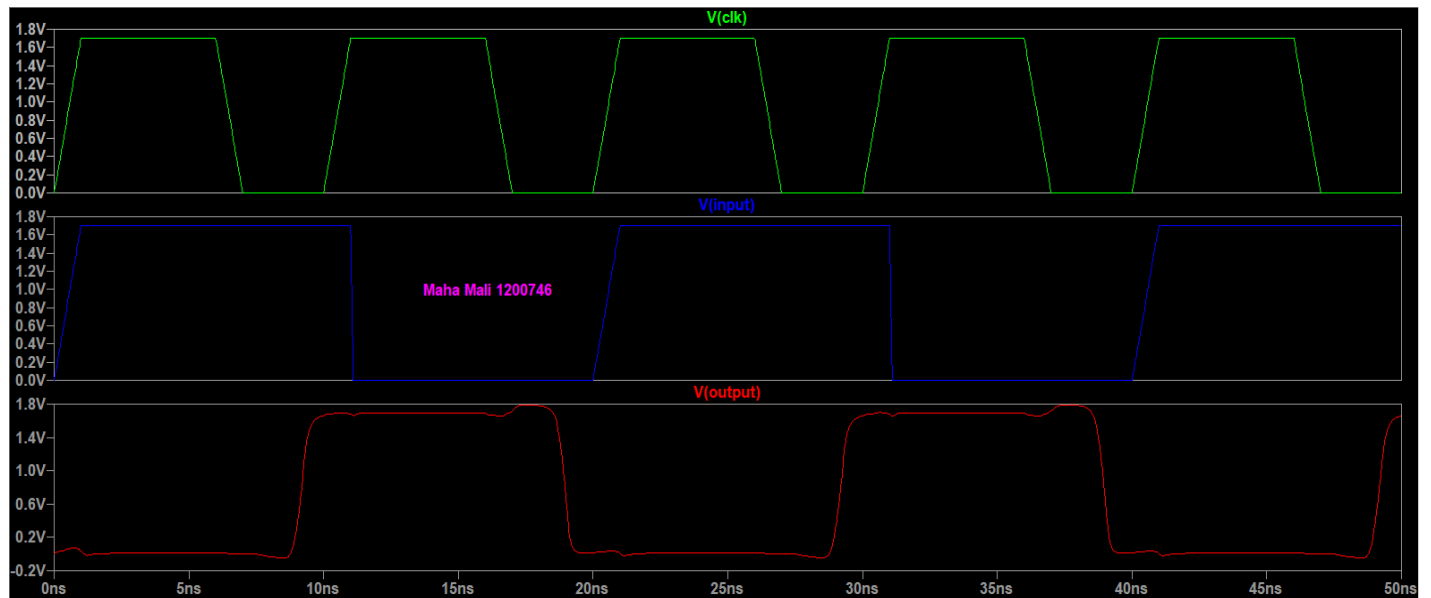


Figure 9: P-Latch Layout Simulation

```

Measurement "vin1_delay" FAIL'ed

Measurement "vout_delay" FAIL'ed
ckout_delay=1.285e-007 FROM 2.15e-008 TO 1.5e-007

Measurement "dout_delay" FAIL'ed

```

Figure 10: P-latch Measurement

Rising Edge Flip-Flop

In rising edge flip-flop, I connect p-latch then n-latch.

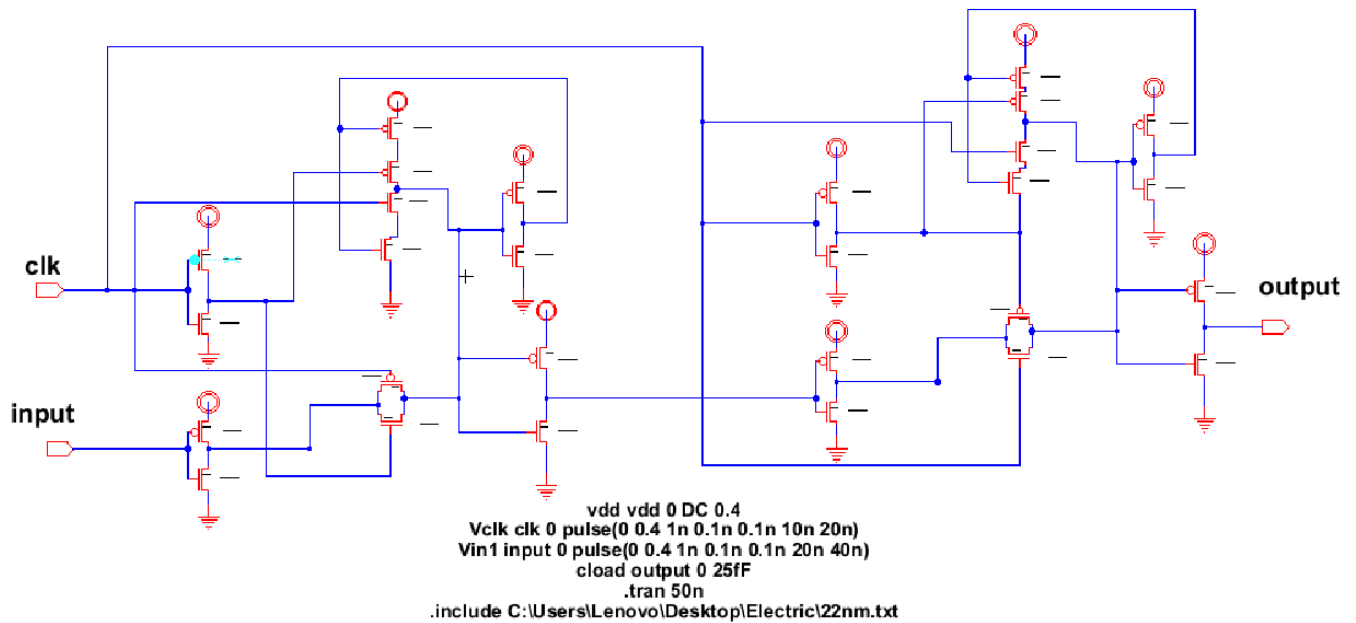


Figure 11: Rising Edge Flip-Flop Schematic

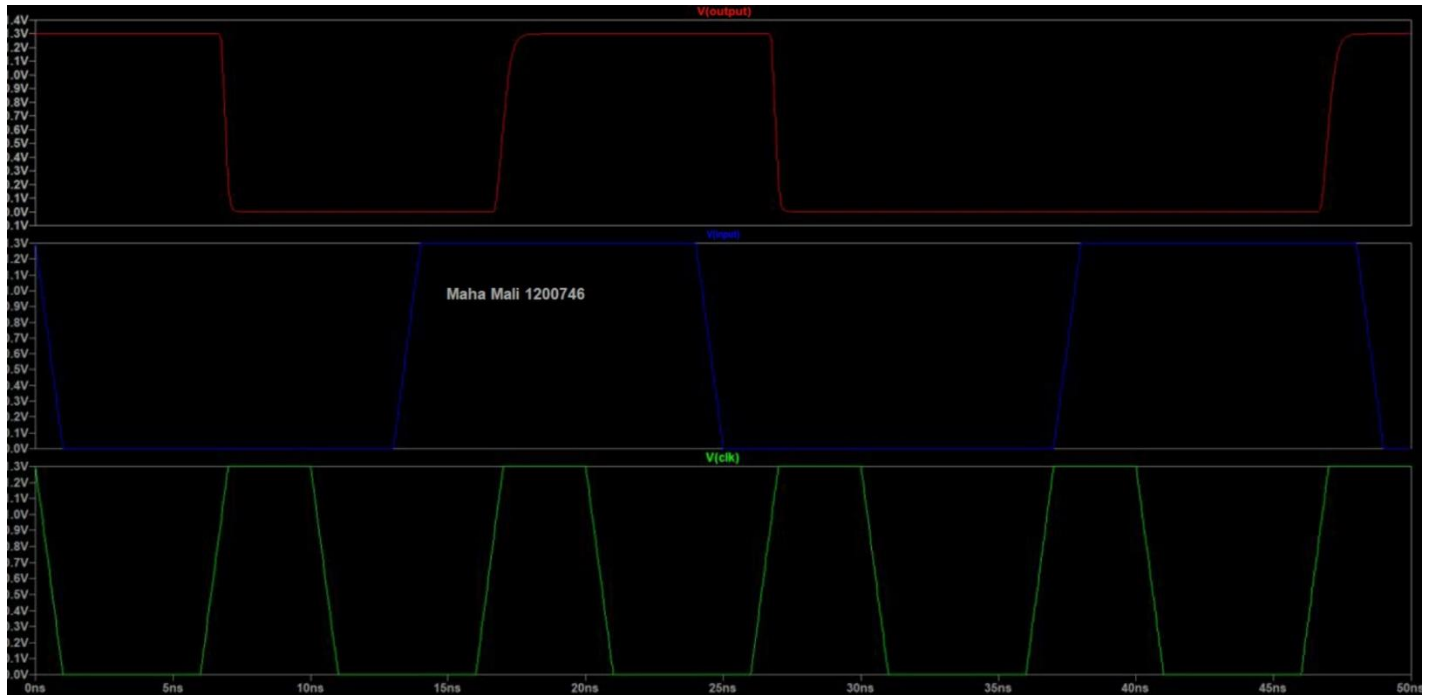


Figure 12: Rising Edge Flip-Flop Schematic Simulation

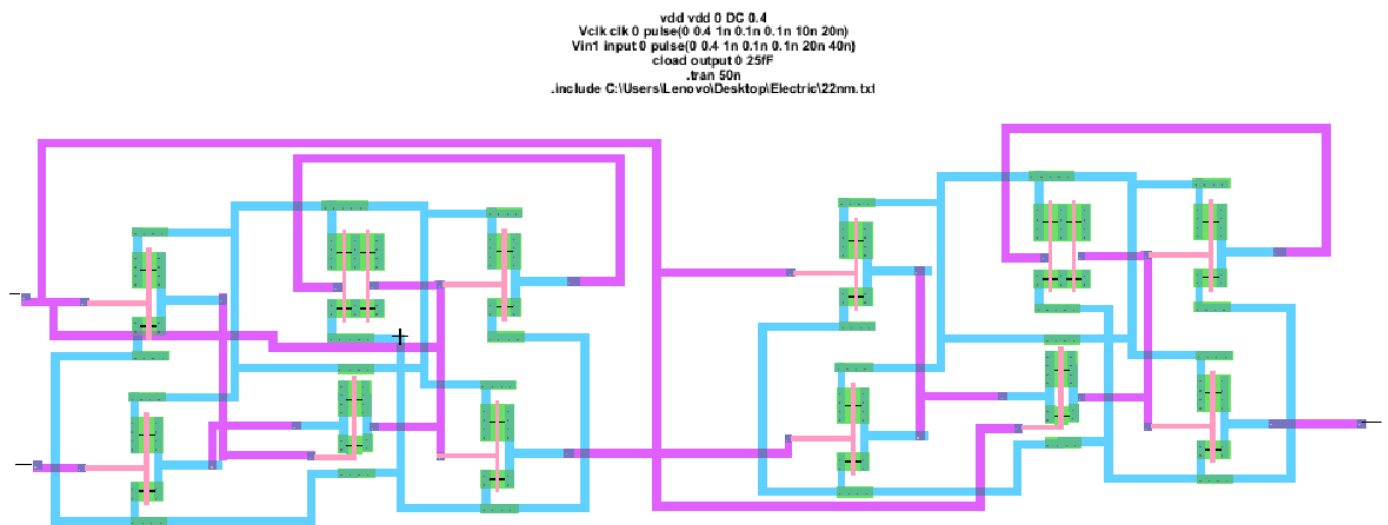


Figure 13: Rising Edge Flip-Flop Layout

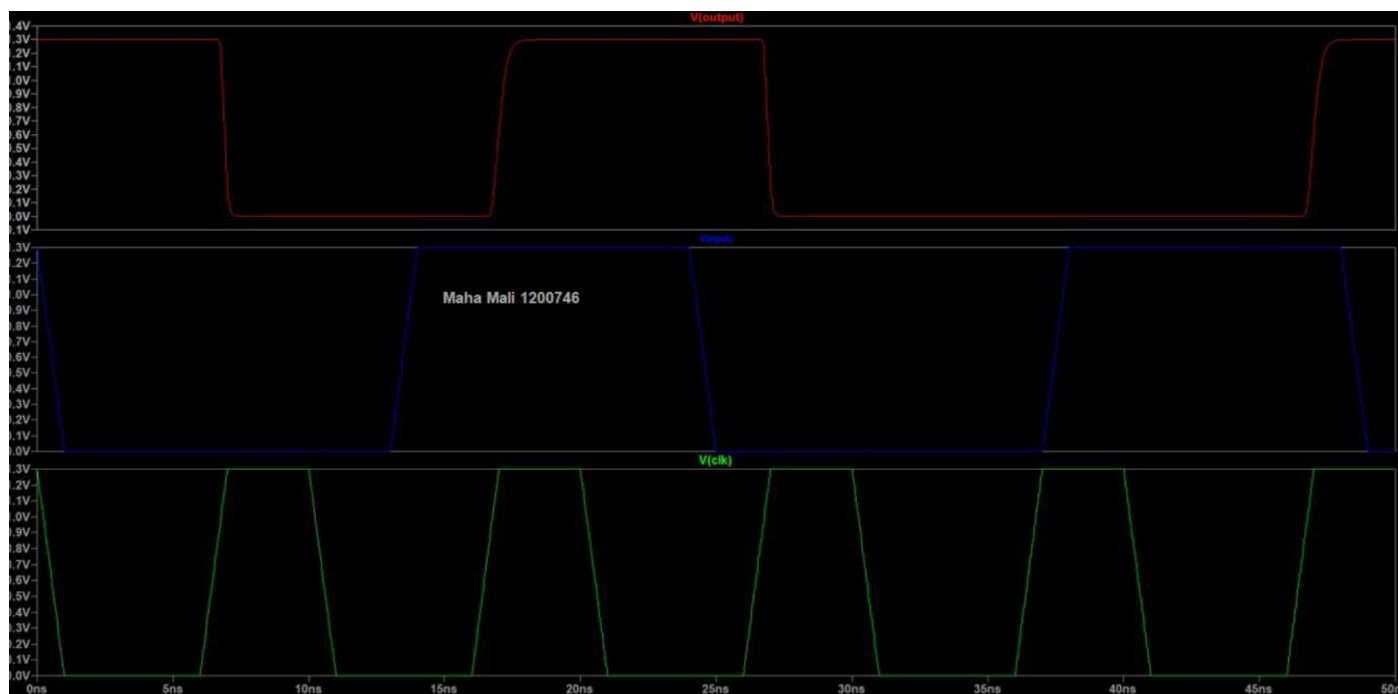


Figure 14: Rising Edge Flip-Flop Layout Simulation

```
Measurement "vin1_delay" FAIL'ed
Measurement "vout_delay" FAIL'ed
ckout_delay=1.285e-007 FROM 2.15e-008 TO 1.5e-007
Measurement "dout_delay" FAIL'ed
```

Figure 15: Rising Edge Flip-Flop Measurement

Falling Edge Flip-Flop

In falling edge flip-flop, I connect n-latch then p-latch.

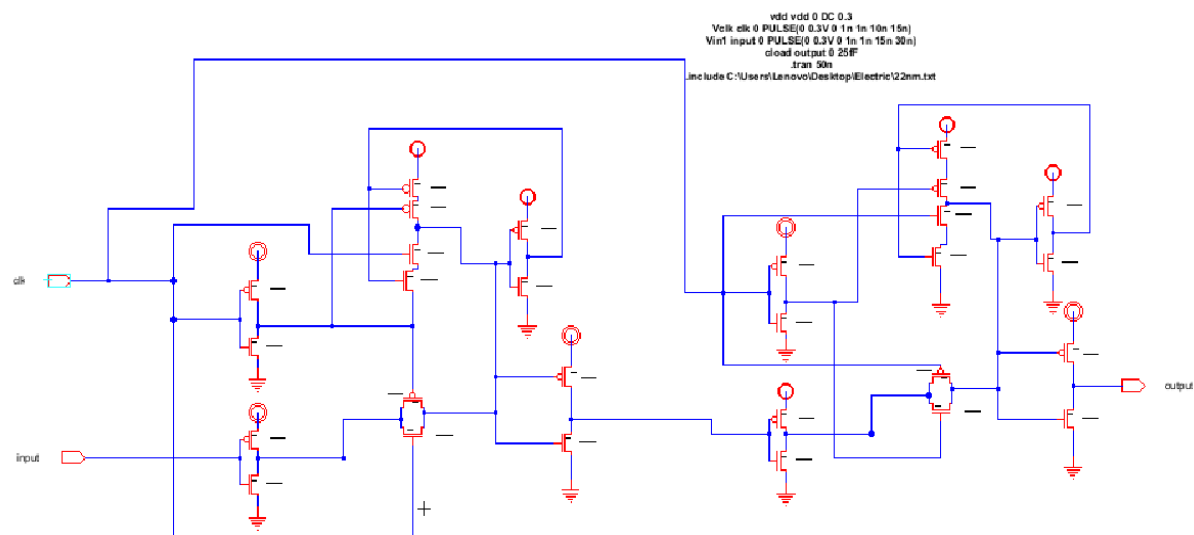


Figure 16: Falling Edge Flip-Flop schematic

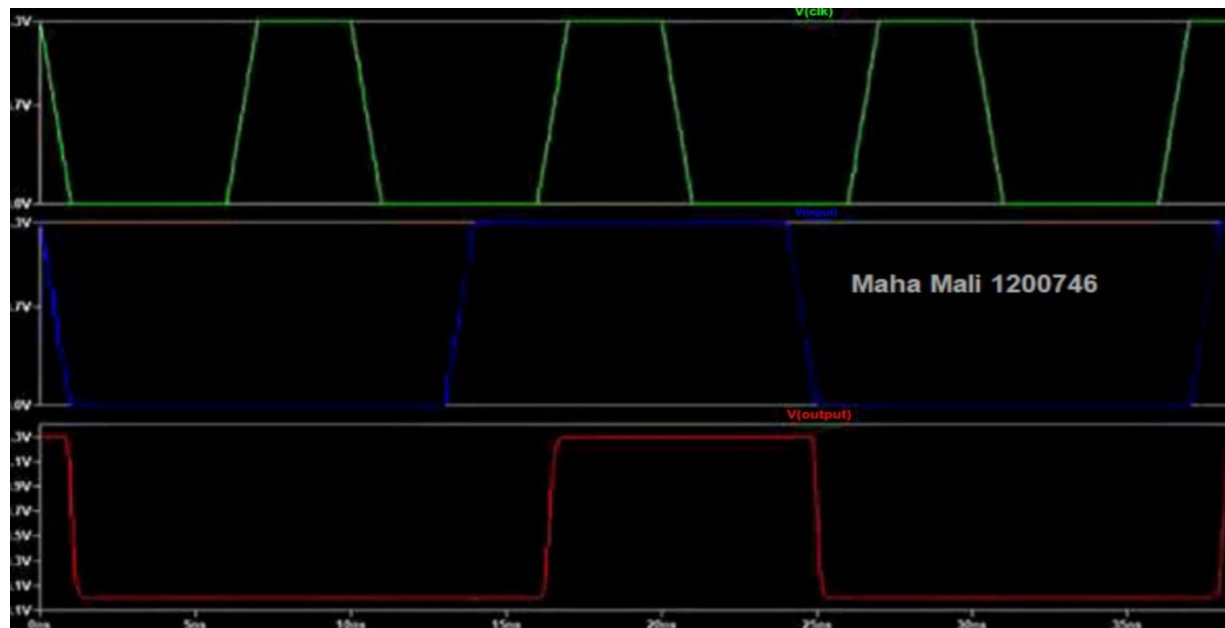


Figure 17: Falling Edge Flip-Flop schematic simulation

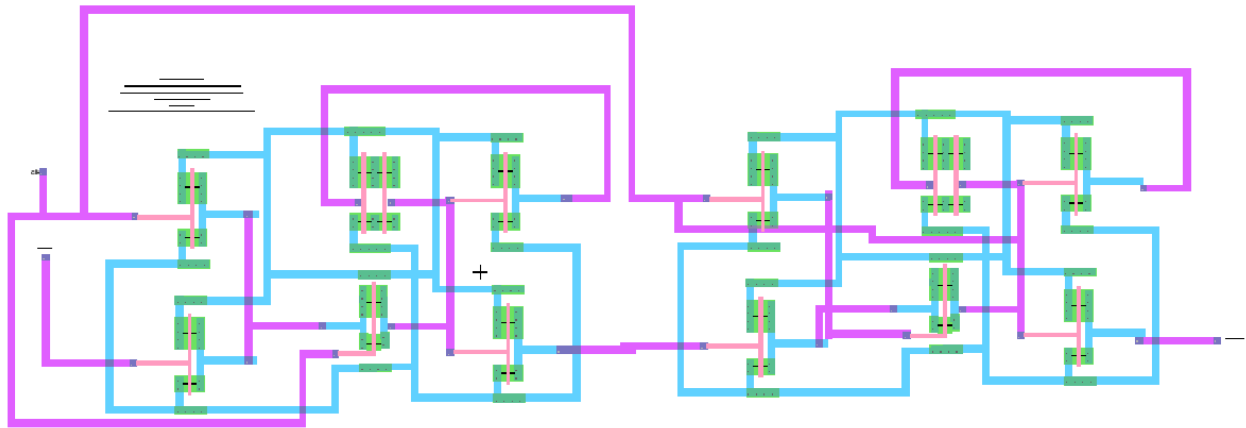


Figure 18: Falling Edge Flip-Flop Layout

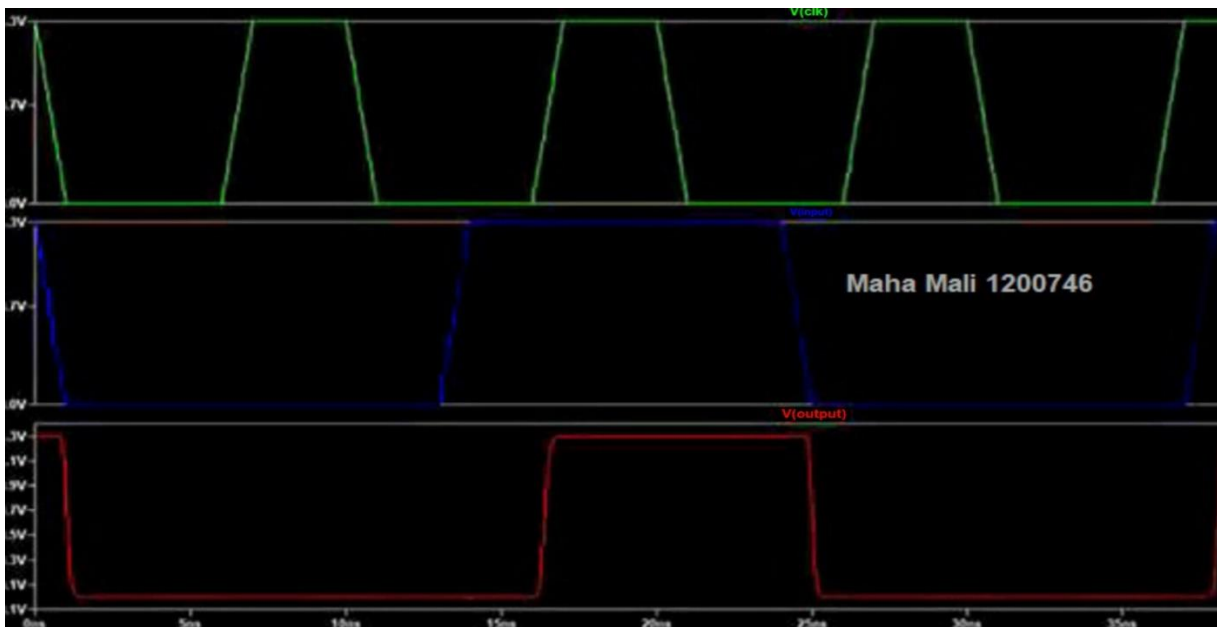


Figure 19: Falling Edge Flip-Flop Layout Simulation

```
Measurement "vin1_delay" FAIL'ed
Measurement "vout_delay" FAIL'ed
ckout_delay=1.285e-007 FROM 2.15e-008 TO 1.5e-007
Measurement "dout_delay" FAIL'ed
```

Figure 20: Falling Edge Flip-Flop Measurement