MD MAHABUBUL ALAM

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SUMMARY

Ph.D. candidate (4^{th} year), experienced in (i) Python (qiskit, pytorch, pennylane, sklearn, numpy, unittest, etc.), (ii) qubit mapping/quantum circuit compilation, (iii) quantum-classical hybrid algorithms (QAOA, Quantum ML) (iv) machine learning/data analytics, and (v) EDA/VLSI - seeking full-time opportunities from Fall-2021.

EDUCATION

Pennsylvania State University, University Park, PA *January 2018 - Present*
PhD Candidate in Electrical Engineering, *GPA: 3.92/4.0*
Thesis Topic: Methodologies to Restore the Computational Power of Quantum-classical Hybrid Algorithms.
Advisor: Dr. Swaroop Ghosh

Courses: Digital Integrated Circuits, Linear Integrated Circuits, Data Mining, Applied Statistics, Manufacturing Methods in Microelectronics.

Auburn University, AL *January 2017 - December 2017*
Graduate Student (Credits transferred to Penn State) in Electrical Engineering, *GPA: 4.0/4.0*

Courses: Advanced VLSI Design, Computer Architecture and Design, Information Networks and Technology, Analog Circuit Design, Introduction to Hardware Security.

Bangladesh University of Engineering and Technology *May 2010 - August 2015*
Bachelor of Science in Electrical and Electronic Engineering, *GPA: 3.73/4.0*

SOFTWARE SKILLS

- **Scripting/Programming:** Python $^{[sample]}$, Tcl, Perl, C/C++, VBA, Verilog HDL, Assembly- 8086.
- **Engineering & Documentation Tools:** MATLAB, MS Excel/PowerPoint/Word, LaTeX.
- **EDA/CAD Tools:** IC Compiler, Design Compiler, Cadence Virtuoso, VCS, Verdi, Vivado, HSPICE.
- **Operating Systems:** Microsoft Windows, UNIX.

WORK EXPERIENCE

Graduate Technical Intern, Intel Corporation *May 2020 - December 2020*

- Time-zero defective parts per million (DPPM) predictive analysis using Intel proprietary tools (DART/XDART) for various products, assisted in methodology development for DPPM predictions on external foundry products, reviewed yield and DPPM modeling principles, attended weekly discussions, prepared reports/presentations, and developed tutorials on our DPPM analysis methodology.
- Assisted in test generation, and debug of TAP network.

Interim Engineering Intern, Qualcomm, Bridgewater, NJ *May 2018 - August 2018*

- Developed a floorplan congestion prediction framework (inspired from *link*).

Graduate Teaching Assistant (Penn State) *January 2018 - December 2018*

- Conducted two laboratory sessions per week ($\approx$ 40 students) on electronic circuit design (inverter, amplifiers, current sources, etc.), held weekly office hour, and evaluated the lab-reports ($\approx$ 40/week).

Physical Design Engineer, Primesilicon Technologies, Bangladesh *October 2015 - December 2016*

- Block-level floorplanning, power-mesh/clock-tree synthesis, timing closure, DRC cleanup, and scripting (Tcl/Perl).

RESEARCH EXPERIENCE

Graduate Research Assistant (Penn State) *January 2019 - Present*

- Studied the performance of QAOA, a prime candidate for early demonstration of quantum supremacy, under noise in superconducting qubits [c7] and developed efficient circuit compilation methodologies for QAOA to improve noise-resilience [c8, c9, c10].

- Developed a parameter initialization scheme to accelerate QAOA using machine learning [c5].
- Developed a Python-based noisy quantum circuit simulator [c2].
- Developed heuristics to address spatial and temporal qubit quality fluctuations [c2, c3, c6].

Graduate Research Assistant (Auburn University) *January 2017 - December 2017*

- Developed a recycled IC detection technique using the frequency degradation of ring oscillators and a digital signature of the test-time frequency to be stored in an on-chip NVM [c1].

MAJOR PUBLICATIONS

[c10] **Alam, Mahabubul**, A. Ash-Saki, and S. Ghosh. "Circuit Compilation Methodologies for Quantum Approximate Optimization Algorithm." MICRO-2020 (Acceptance Rate $\approx$ 19.0%).

[c9] **Alam, Mahabubul**, A. Ash-Saki, and S. Ghosh. "Noise-resilient Compilation Policies for Quantum Approximate Optimization Algorithm" ICCAD-2020 (Invited Paper).

[c8] **Alam, Mahabubul**, A. Ash-Saki, and S. Ghosh. "An Efficient Circuit Compilation Flow for Quantum Approximate Optimization Algorithm." DAC-2020 (Acceptance Rate $\approx$ 24.0%).

[c7] **Alam, Mahabubul**, A. Ash-Saki, and S. Ghosh. "Design-Space Exploration of Quantum Approximate Optimization Algorithm under Noise." CICC-2020 (Acceptance Rate $\approx$ 20.0%).

[c6] Ash-Saki, Abdullah, **Mahabubul Alam**, and S. Ghosh. "Improving Reliability of Quantum True Random Number Generator using Machine Learning." ISQED-2020 (Acceptance Rate $\approx$ 30.0%).

[c5] **Alam, Mahabubul**, A. Ash-Saki, and S. Ghosh. "Accelerating Quantum Approximate Optimization Algorithm using Machine Learning." DATE-2020 (Acceptance Rate $\approx$ 37.0%).

[c4] Bhattacharjee, Debjyoti, A. Ash-Saki, **Mahabubul Alam**, A. Chattopadhyay, S. Ghosh "MUQUT: Multi-Constraint Quantum Circuit Mapping on NISQ Computers." ICCAD-2019 (Invited Paper).

[c3] **Alam, Mahabubul**, A. Ash-Saki, and S. Ghosh. "Addressing Temporal Variations in Qubit Quality Metrics for Parameterized Quantum Circuits." ISLPED-2019 (Acceptance Rate $\approx$ 23.0%).

[c2] Ash-Saki, Abdullah, **Mahabubul Alam**, and S. Ghosh. "QURE: Qubit Re-allocation in Noisy Intermediate-Scale Quantum Computers." DAC-2019 (Acceptance Rate $\approx$ 24.3%).

[c1] **Alam, Mahabubul**, S. Chowdhury, M. M. Tehranipoor, and U. Guin. "Robust, low-cost, and accurate detection of recycled ICs using digital signatures." HOST-2018, (Acceptance Rate $\approx$ 24.0%).

MAJOR GRADUATE PROJECTS

- **16-bit Pipelined Processor:** Design of a 16-bit 5-stage (MIPS-like) pipelined processor with 16 instructions using Verilog HDL, and implementation on Nexys 4 DDR FPGA module.
- **10-bit, 5 MS/s ADC:** Schematic and layout of 10-bit 5 MS/s SAR ADC (monotonic capacitor switching topology) in 600nm technology node using Cadence Virtuoso.
- **2KB SRAM Array:** Schematic and layout of a 2KB SRAM array with peripherals in 180nm technology node using Cadence Virtuoso.
- **SRAM PUF:** SRAM PUF with the on-board SRAM chip of CMOD A7 FPGA module.

ACHIEVEMENTS

- Second Place, Student Research Competition at the IEEE/ACM International Conference on Computer Aided Design, 2020 (SRC@ICCAD2020).
- Richard Newton Young Student Fellow, IEEE/ACM Design Automation Conference (DAC), 2020.
- NSF Student Travel Award, IEEE VLSI Test Symposium (VTS), 2018.
- Dean's List and Faculty Honors as an undergraduate student (2015/2013), Bangladesh.
- Merit scholarships for excellence in junior, secondary, and higher-secondary public examinations, Bangladesh.