MD MAHABUBUL ALAM

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SUMMARY

Ph.D. candidate (4^{th} year), experienced in (i) Python (qiskit, pytorch, tensorflow, pennylane, sklearn, numpy, scipy), (ii) software stack for quantum computing: qubit mapping/quantum circuit compilation/approximate synthesis, (iii) applied machine learning/deep learning/data analytics, and (iv) Physical Design/EDA/VLSI/Quality & Reliability Engineering - seeking full-time opportunities from May 2022.

EDUCATION

Pennsylvania State University, University Park, PA *January 2018 - Present*
PhD Candidate in Electrical Engineering, *GPA: 3.92/4.0*
Thesis Topic: Resilient Quantum Computing and Machine Learning
Advisor: Dr. Swaroop Ghosh

Courses: Digital Integrated Circuits, Linear Integrated Circuits, Data Mining, Applied Statistics, Manufacturing Methods in Microelectronics.

Auburn University, AL *January 2017 - December 2017*
Graduate Student (Credits transferred to Penn State) in Electrical Engineering, *GPA: 4.0/4.0*

Courses: Advanced VLSI Design, Computer Architecture and Design, Information Networks and Technology, Analog Circuit Design, Introduction to Hardware Security.

Bangladesh University of Engineering and Technology *May 2010 - August 2015*
Bachelor of Science in Electrical and Electronic Engineering, *GPA: 3.73/4.0*

ACHIEVEMENTS

- James E Marley Graduate Fellowship in Engineering, College of Engineering, Penn State, Spring 2021.
- Second Place, Student Research Competition, IEEE/ACM ICCAD, 2020 (SRC@ICCAD2020).
- Richard Newton Young Student Fellow, IEEE/ACM Design Automation Conference (DAC), 2020.
- NSF Student Travel Award, IEEE VLSI Test Symposium (VTS), 2018.

WORK EXPERIENCE

Graduate Technical Intern, Intel Corporation *May 2020 - December 2020*

- Time-zero defective parts per million (DPPM) predictive analysis using Intel proprietary tools (DART/XDART) for various products, assisted in methodology development for DPPM predictions on external foundry products, attended weekly discussions, and prepared reports/presentations.
- Assisted in test generation, and debug of TAP network.

Interim Engineering Intern, Qualcomm, Bridgewater, NJ *May 2018 - August 2018*

- Developed a floorplan congestion prediction framework (inspired from *here*).

Physical Design Engineer, Primesilicon Technologies, Bangladesh *October 2015 - December 2016*

- Block-level floorplanning, power-mesh design, clock-tree synthesis (CTS), timing closure (STA), and DRC.
- Scripting in Perl/Tcl for data parsing and automation.

RESEARCH EXPERIENCE

Graduate Research Assistant (Penn State) *January 2018 - Present*

- Developed a **scalable and noise-resilient** quantum neural network (QNN) architecture called **QNet** and demonstrated ≈43% better accuracy on average over the state-of-the-art methods under noise [10].
- Developed **efficient circuit compilation methodologies** for quantum approximate optimization algorithm **(QAOA)** and achieved ≈23% reduction in gate-count, ≈53% reduction in circuit-depth, and ≈25.8% improvement in success probability on average over the state-of-the-art [6, 7, 8].

- Developed a **parameter initialization** scheme to accelerate **QAOA** using **machine learning** and demonstrated ≈44.9% speed-up on average for various MaxCut problems [4].

Graduate Research Assistant (Auburn University) *January 2017 - December 2017*

- Developed a low-cost **Recycled IC Detection** technique [2].
- Developed an **Edge Device Authentication** scheme for the internet of things [1].

SOFTWARE SKILLS

- **Engineering & Documentation Tools:** MATLAB, MS Excel/PowerPoint/Word, LaTeX.
- **EDA/CAD Tools:** IC Compiler, Design Compiler, Cadence Virtuoso, VCS, Verdi, Vivado, HSPICE.
- **Scripting/Programming:** Python, Tcl, Perl, C/C++, Verilog.
- **Operating Systems:** Microsoft Windows, Linux.

MAJOR OPEN SOURCE CONTRIBUTIONS

- **QAOA Compiler:** This Python-based project incorporates the QAOA-specific compilation techniques developed in [6, 7, 8]. It can be used for aggressive optimization of QAOA workloads ( )
- **QNN Builder:** This Python-based research tool can be used to build and train QNN with a variety of design choices for any given dataset. It can be useful for QNN design-space exploration ( )

MAJOR PUBLICATIONS

Synopsis: Conferences - 23, Journals - 5, Pre-prints - 3, Citations - 248 (*Google Scholar*)

[10] **Mahabubul Alam**, and Swaroop Ghosh. "QNet: A Scalable and Noise-resilient Quantum Neural Network Architecture for Noisy Intermediate-Scale Quantum Computers." Frontiers in Physics, 2021.

[9] **Mahabubul Alam**, Satwik Kundu, Rasit Topaloglu, and Swaroop Ghosh. "Quantum-Classical Hybrid Machine Learning for Image Classification." ACM/IEEE ICCAD, 2021 (Invited Paper).

[8] **Mahabubul Alam**, Abdullah Ash-Saki, and Swaroop Ghosh. "Circuit Compilation Methodologies for Quantum Approximate Optimization Algorithm." IEEE/ACM MICRO, 2020 (Acceptance Rate ≈ 19.0%).

[7] **Mahabubul Alam**, Abdullah Ash-Saki, and Swaroop Ghosh. "Noise-resilient Compilation Policies for Quantum Approximate Optimization Algorithm." ACM/IEEE ICCAD, 2020 (Invited Paper).

[6] **Mahabubul alam**, Abdullah Ash-Saki, and Swaroop Ghosh. "An Efficient Circuit Compilation Flow for Quantum Approximate Optimization Algorithm." ACM/IEEE DAC, 2020 (Acceptance Rate ≈ 24.0%).

[5] **Mahabubul Alam**, Abdullah Ash-Saki, and Swaroop Ghosh. "Design-Space Exploration of Quantum Approximate Optimization Algorithm under Noise." IEEE CICC, 2020 (Acceptance Rate ≈ 20.0%).

[4] **Mahabubul Alam**, Abdullah Ash-Saki, and Swaroop Ghosh. "Accelerating Quantum Approximate Optimization Algorithm using Machine Learning." ACM/IEEE DATE, 2020 (Acceptance Rate ≈ 37.0%).

[3] Abdullah Ash-Saki, **Mahabubul Alam**, and Swaroop Ghosh. "QURE: Qubit Re-allocation in Noisy Intermediate Scale Quantum Computers." ACM/IEEE DAC, 2019 (Acceptance Rate ≈ 24.3%).

[2] **Mahabubul Alam**, Sreeja Chowdhury, Mark M. Tehranipoor, and Ujjwal Guin. "Robust, low-cost, and accurate detection of recycled ICs using digital signatures." IEEE HOST, 2018 (Acceptance Rate ≈ 24.0%).

[1] Ujjwal Guin, Adit Singh, **Mahabubul Alam**, Janice Canedo, and Anthony Skjellum. "A secure low-cost edge device authentication scheme for the Internet of Things." IEEE VLSID, 2018 (Acceptance Rate ≈ 24.0%).

MAJOR GRADUATE PROJECTS

- **16-bit Pipelined Processor:** Design of a 16-bit 5-stage (MIPS-like) pipelined processor with 16 instructions using Verilog HDL, and implementation on Nexys 4 DDR FPGA module.
- **10-bit, 5 MS/s ADC:** Schematic and layout of 10-bit 5 MS/s SAR ADC (monotonic capacitor switching topology) in 600nm technology node using Cadence Virtuoso.
- **2KB SRAM Array:** Schematic and layout of a 2KB SRAM array with peripherals in 180nm technology node using Cadence Virtuoso.