PARITY GENERATOR AND PARITY CHECKING

AIM

To design and verify the truth table of a three bit Odd and Even Parity generator and checker.

COMPONENTS REQUIRED

S.NO	COMPONENTS	SPECIFICATION	QUANTITY
1.	Digital IC trainer Kit	-	1
2.	NOT Gate	IC 7404	1
3.	EX-OR Gate	IC 7486	1
4.	Connecting wires	-	As required

PARITY GENERATOR AND PARITY CHECKER

A Parity bit is used for the purpose of detecting errors during transmission of binary information. A parity bit is an extra bit included with a binary message to make the number of 1's either odd or even. The message including the parity bit is transmitted and then checked at the receiving end for errors. An error is detected if the checked parity does not correspond with the one transmitted. The circuit that generates the parity bit in the transmitter is called a parity generator and the circuit that checks the parity in the receiver is called a parity checker.

In even parity the added parity bit will make the total number of 1's an even amount and in odd parity the added parity bit will make the total number of 1's an odd amount. In a three bit odd parity generator the three bits in the message together with the parity bit are transmitted to their destination, where they are applied to the parity checker circuit. The parity checker circuit checks for possible errors in the transmission.

Since the information was transmitted with odd parity the four bits received must have an odd number of 1's. An error occurs during the transmission if the four bits received have an even number of 1's, indicating that one bit has changed during transmission. The output of the parity checker is denoted by PEC (parity error check) and it will be equal to 1 if an error occurs, i.e., if the four bits received has an even number of 1's.

ODD PARITY GENERATOR

Truth Table

Input (Three Bit Message)			**Output** (Odd Parity Bit)
A	**B**	**C**	**P**
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

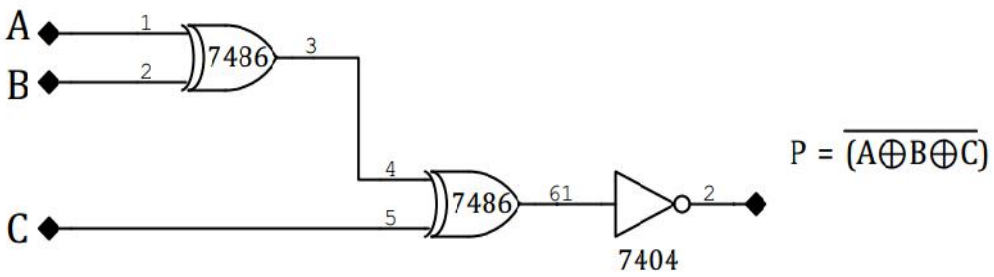
From the truth table, the expression for the output parity bit is,

$$P\ (A,B,C) = \sum(0,3,5,6)$$

Also written as

$$\begin{aligned} P &= \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\,C + A\,\overline{B}\,C + A\,B\,\overline{C} \\ &= \overline{A}\left(\overline{B}\,\overline{C} + B\,C\right) + A\left(\overline{B}\,C + B\,\overline{C}\right) \\ &= \overline{A}\left(\overline{B \oplus C}\right) + A\,(B \oplus C) \\ &= \overline{A \oplus B \oplus C} \end{aligned}$$

Circuit Diagram



ODD PARITY CHECKER

Truth Table

INPUT (Four bit message received)				OUTPUT (Parity error check)
A	**B**	**C**	**P**	**X**
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

From the truth table

$$X\ (A,B,C,P) = \sum(0,3,5,6,9,10,12,15)$$

$$X = \overline{A}\,\overline{B}\,\overline{C}\,\overline{P} + \overline{A}\,\overline{B}\,C\,P + \overline{A}\,B\,\overline{C}\,P + \overline{A}\,B\,C\,\overline{P} + A\,\overline{B}\,\overline{C}\,P + A\,\overline{B}\,C\,\overline{P} + A\,B\,\overline{C}\,\overline{P} + A\,B\,C\,P$$

$$= \overline{A}\,\overline{B}\left(\overline{C}\,\overline{P} + C\,P\right) + \overline{A}\,B\left(\overline{C}\,P + C\,\overline{P}\right) + A\,\overline{B}\left(\overline{C}\,P + C\,\overline{P}\right) + A\,B\left(\overline{C}\,\overline{P} + C\,P\right)$$

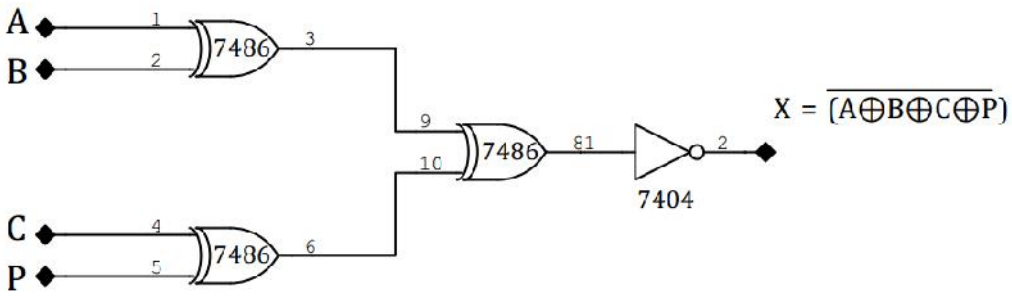
$$= \overline{A}\,\overline{B}\left(\overline{C \oplus P}\right) + \overline{A}\,B\,(C \oplus P) + A\,\overline{B}\,(C \oplus P) + A\,B\left(\overline{C \oplus P}\right)$$

$$= \left(\overline{A}\,\overline{B} + A\,B\right)\left(\overline{C \oplus P}\right) + \left(\overline{A}\,B + A\,\overline{B}\right)(C \oplus P)$$

$$= \left(\overline{A \oplus B}\right)\left(\overline{C \oplus P}\right) + (A \oplus B)\,(C \oplus P)$$

$$= \left(\overline{A \oplus B \oplus C \oplus P}\right)$$

Circuit Diagram



EVEN PARITY GENERATOR

Truth Table

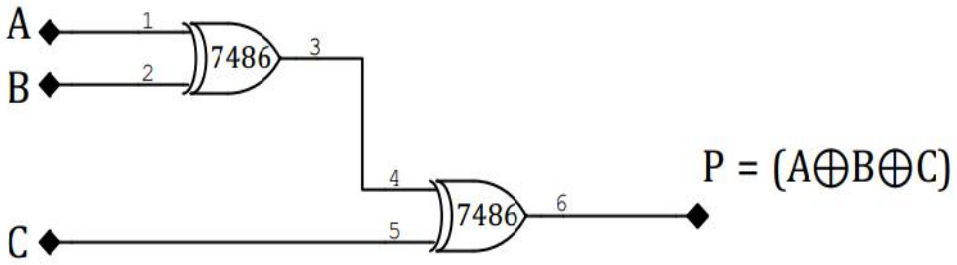
Input (Three Bit Message)			**Output** (Even Parity Bit)
A	**B**	**C**	**P**
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

From the truth table

$$P\ (A,B,C) = \sum(1,2,4,7)$$

$$\begin{aligned} P &= \overline{A}\,\overline{B}\,C + \overline{A}\,B\,\overline{C} + A\,\overline{B}\,\overline{C} + A\,B\,C \\ &= \overline{A}\left(\overline{B}\,C + B\,\overline{C}\right) + A\left(\overline{B}\,\overline{C} + B\,C\right) \\ &= \overline{A}(B \oplus C) + A\left(\overline{B \oplus C}\right) \\ &= (A \oplus B \oplus C) \end{aligned}$$

Circuit Diagram



EVEN PARITY CHECKER

Truth Table

INPUT (Four bit message received)				**OUTPUT** (Parity error check)
A	**B**	**C**	**P**	**X**
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

From the truth table

$$X\ (A,B,C,P) = \sum(1,2,4,7,8,11,13,14)$$

Also written as

$$X = \overline{A}\,\overline{B}\,\overline{C}\,P + \overline{A}\,\overline{B}\,C\,\overline{P} + \overline{A}\,B\,\overline{C}\,\overline{P} + \overline{A}\,B\,C\,P + A\,B\,\overline{C}\,P + A\,B\,C\,\overline{P} + A\,\overline{B}\,\overline{C}\,\overline{P} + A\,\overline{B}\,C\,P$$

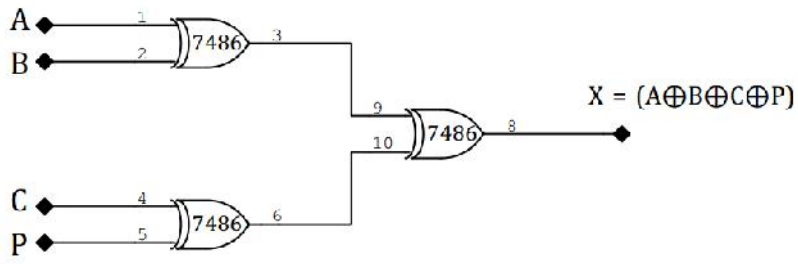
$$= \overline{A}\,\overline{B}(\overline{C}\,P + C\,\overline{P}) + \overline{A}\,B\,(\overline{C}\,\overline{P} + C\,P) + A\,B\,(\overline{C}\,P + C\,\overline{P}) + A\,\overline{B}\,(\overline{C}\,\overline{P} + C\,P)$$

$$= \overline{A}\,\overline{B}(C \oplus P) + \overline{A}\,B\,\overline{(C \oplus P)} + A\,B(C \oplus P) + A\,\overline{B}\,\overline{(C \oplus P)}$$

$= (C \oplus P)\ \overline{(A \oplus B)} + (A \oplus B)\ \overline{(C \oplus P)}$

$= (A \oplus B \oplus C \oplus P)$

Circuit Diagram



Result

Thus the Parity Generator and Parity Checker for odd and even parity were designed.