CS221: Digital Design

Counter & Registers

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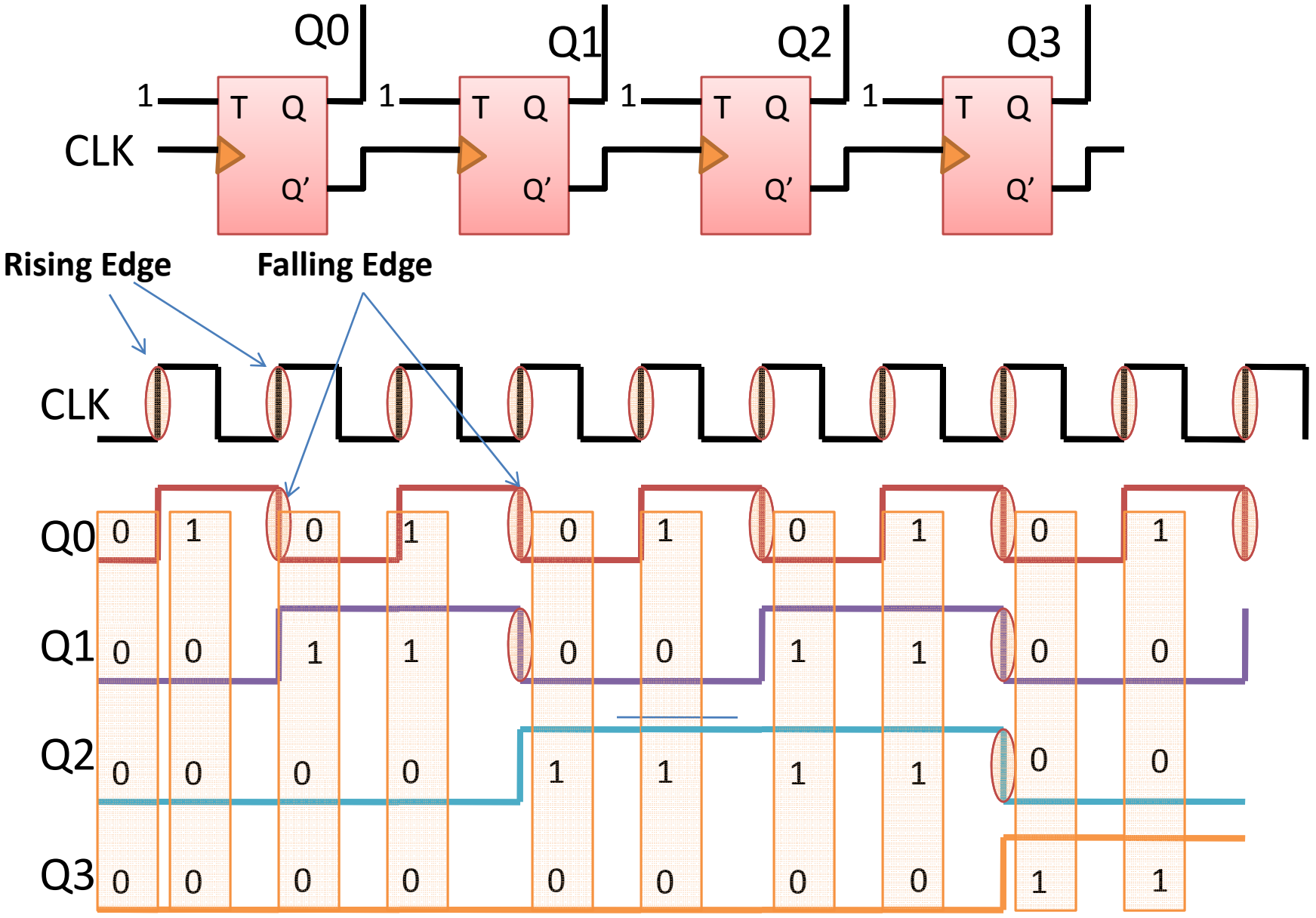
Outline

- Counter : Synchronous Vs Asynchronous
- Counter: Finite State Machine
  - **A register and Combinational logic**
- Counter & FSM Controller:
  - Using JK FFs, RS FF and T FFs
- Up/Down Counter, Clear, Load Counter
- Registers
  - Preset/Clear, Load, Left/Right Shift
- Counter Based on Shift Registers

Binary Counter: Asynchronous

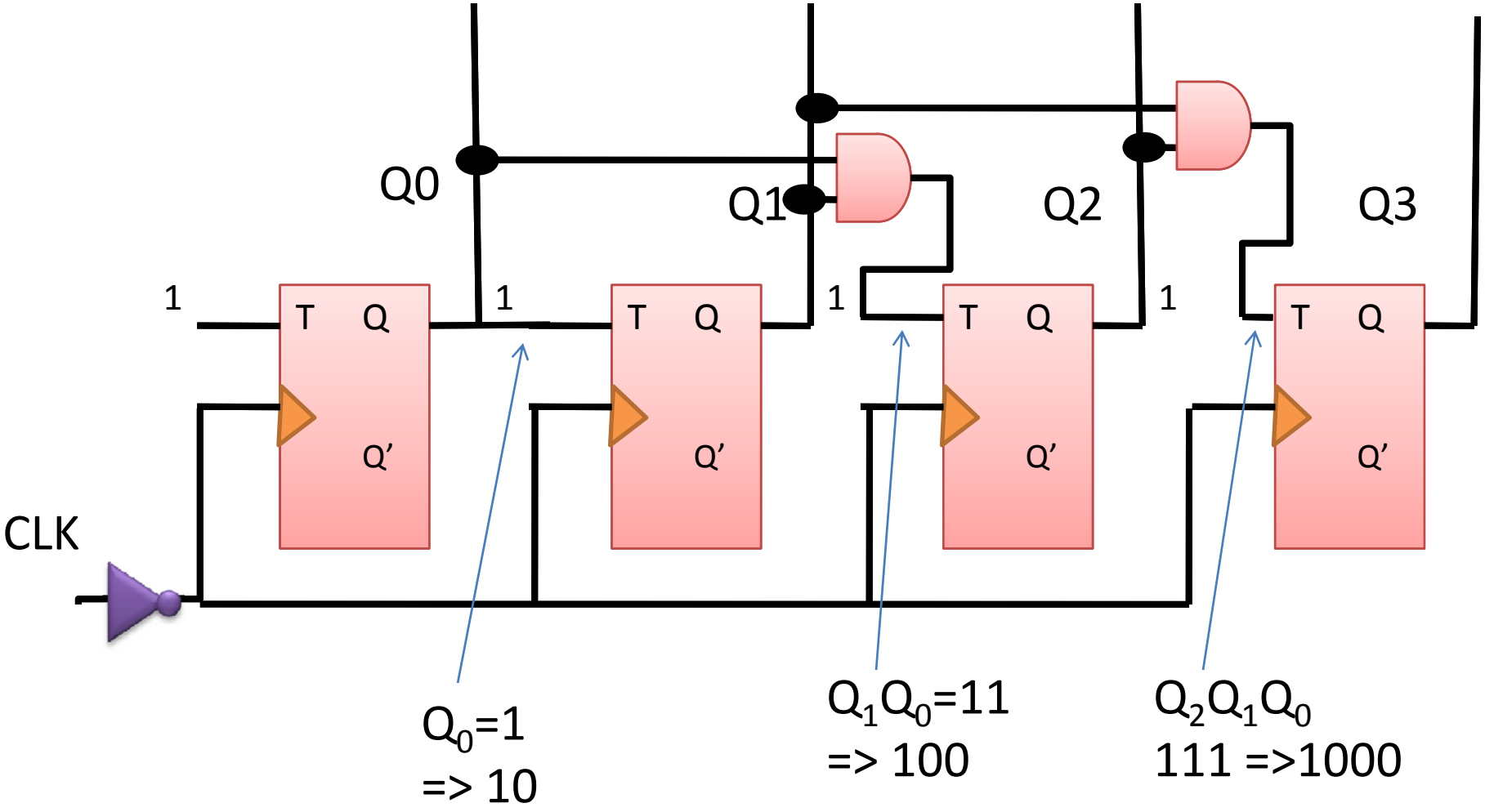


Counter : Sync Vs Async

- **Asynchronous Counter : Ripple Counter**
  - Change in State of Q_{i-1} is used to Toggle Q_i
  - Clock is applied at FF0, it propagate through to FFn
  - Input Clock to FF1= Skewed version of Clk of FF0
    - Clock + Propagation delay of FF
  - Rippling : Overall time delay of occurrence of count pulse and when stabilized count appear at O/P
  - When counter : 1111..11 to 0000..00, toggle signal must propagate through all FFs
  - **Wrost case Settling time: $n \times t_{pd}$**

    where t_{pd} =Propagation delay of a FF
- **Synchronous Counter**: One single clock to all FF

Binary Counter: Synchronous

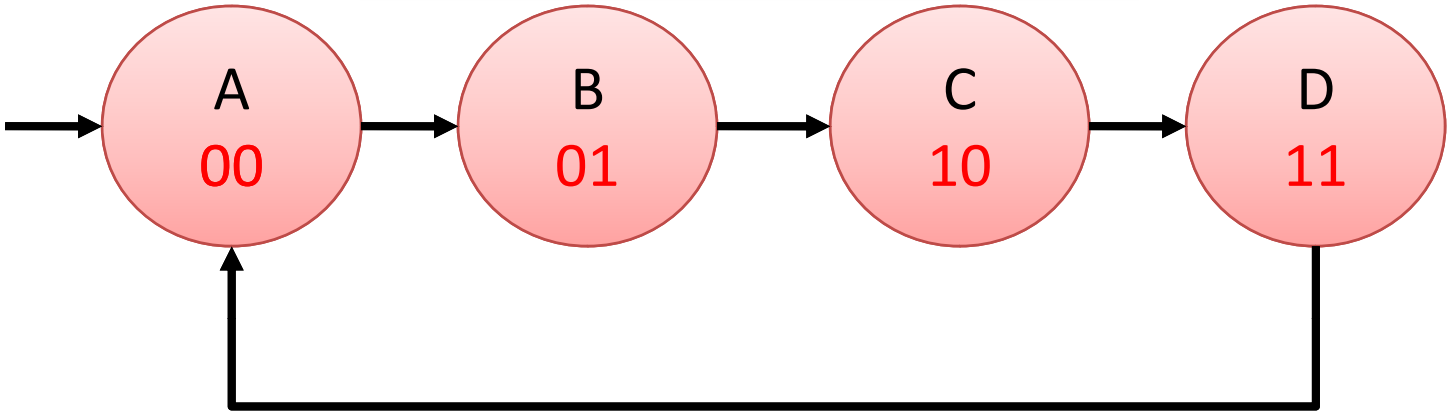


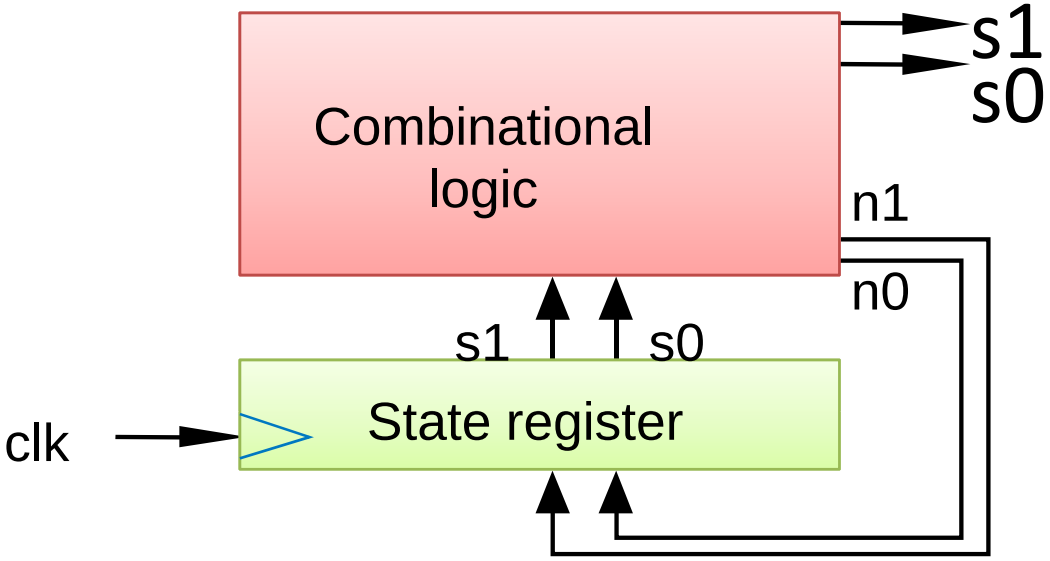
Counter

- Example of 4 bit counter
- Count from 0000 to 1111 and repeat
- Up counter : 0000 to 1111
- Down counter : 1111 to 0000
- Mod N counter:
  - Mod 10 counter : 0000 to 1001 (0 to 9) and repeat
  - Mod 6 counter : 000 to 101 (0 to 5) and repeat

FSM of Counter : 2 bit

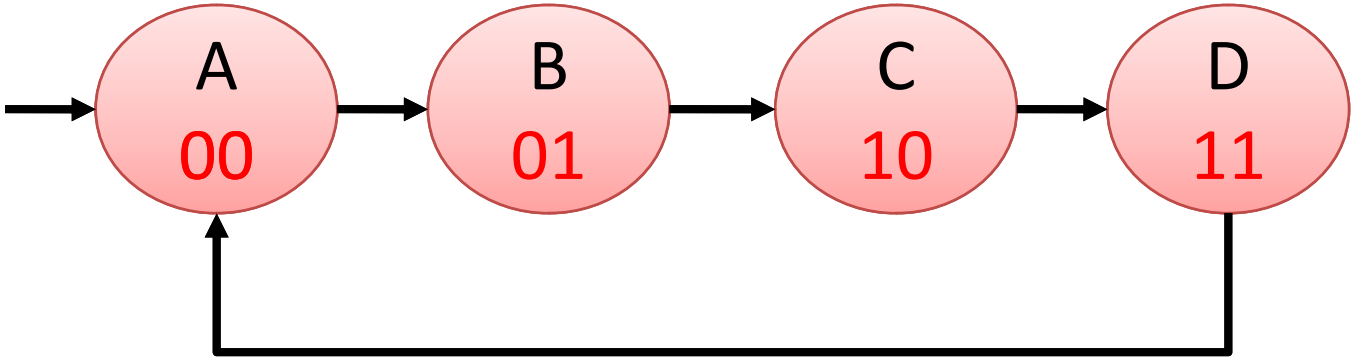
State bits = Output bits





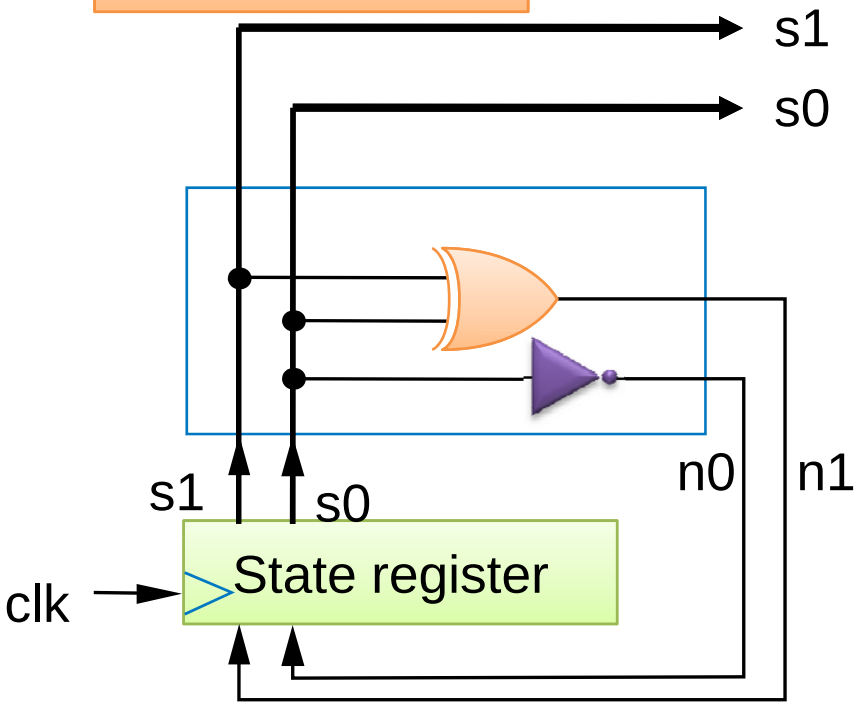
	I/P		O/P	
	s1	s0	n0	n1
A	0	0	0	1
B	0	1	1	0
C	1	0	1	1
B	1	1	0	0

FSM Controller: Binary Counter



n1 = s1 xor s0
n0 = s0'

	I/P		O/P	
	s1	s0	n0	n1
A	0	0	0	1
B	0	1	1	0
C	1	0	1	1
B	1	1	0	0

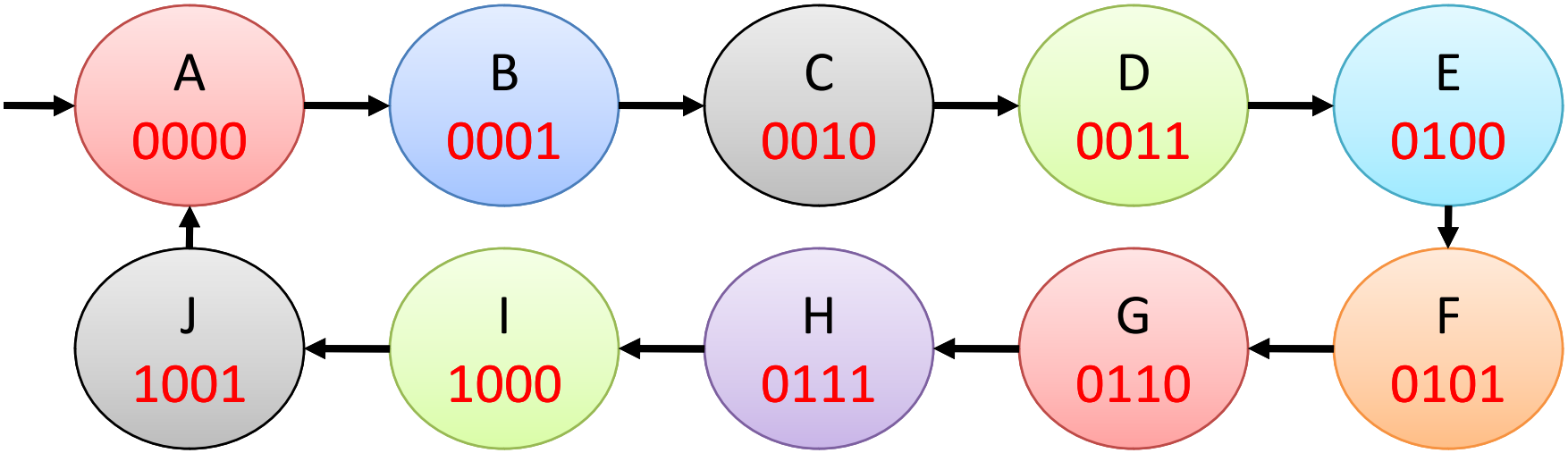


Synchronous Counter : Design

- **Together: Create FSM, Encode Bit**
- State Table
- Design Combination Circuit

Mod 10 Counter: BCD Counter

- Count from 0000 to 1001 (0-9 the Reset)
- FSM with Encoding **done**



State Table Creation

Present State				Next State			
S3	S2	S1	S0	N3	N2	N1	N0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0

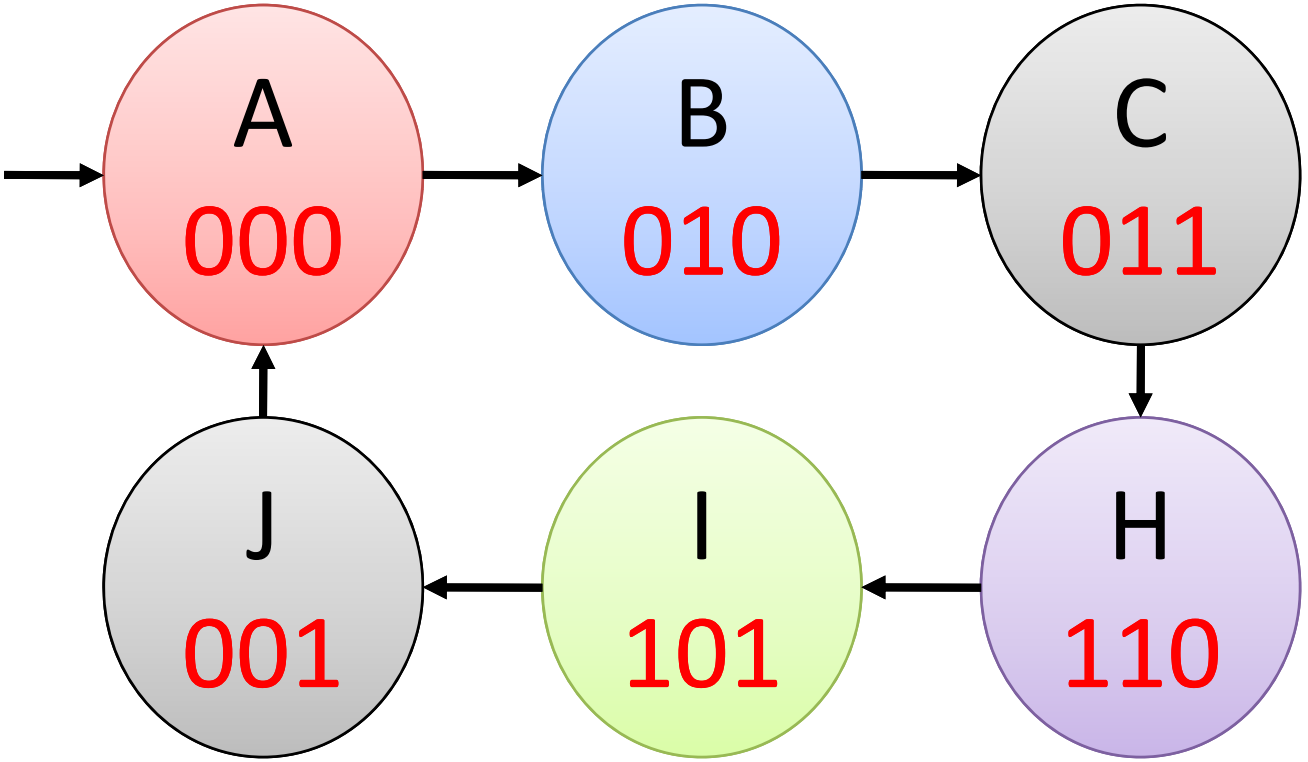
N0=S0’
N1=
N3=
N4=

Using other FF in Counter

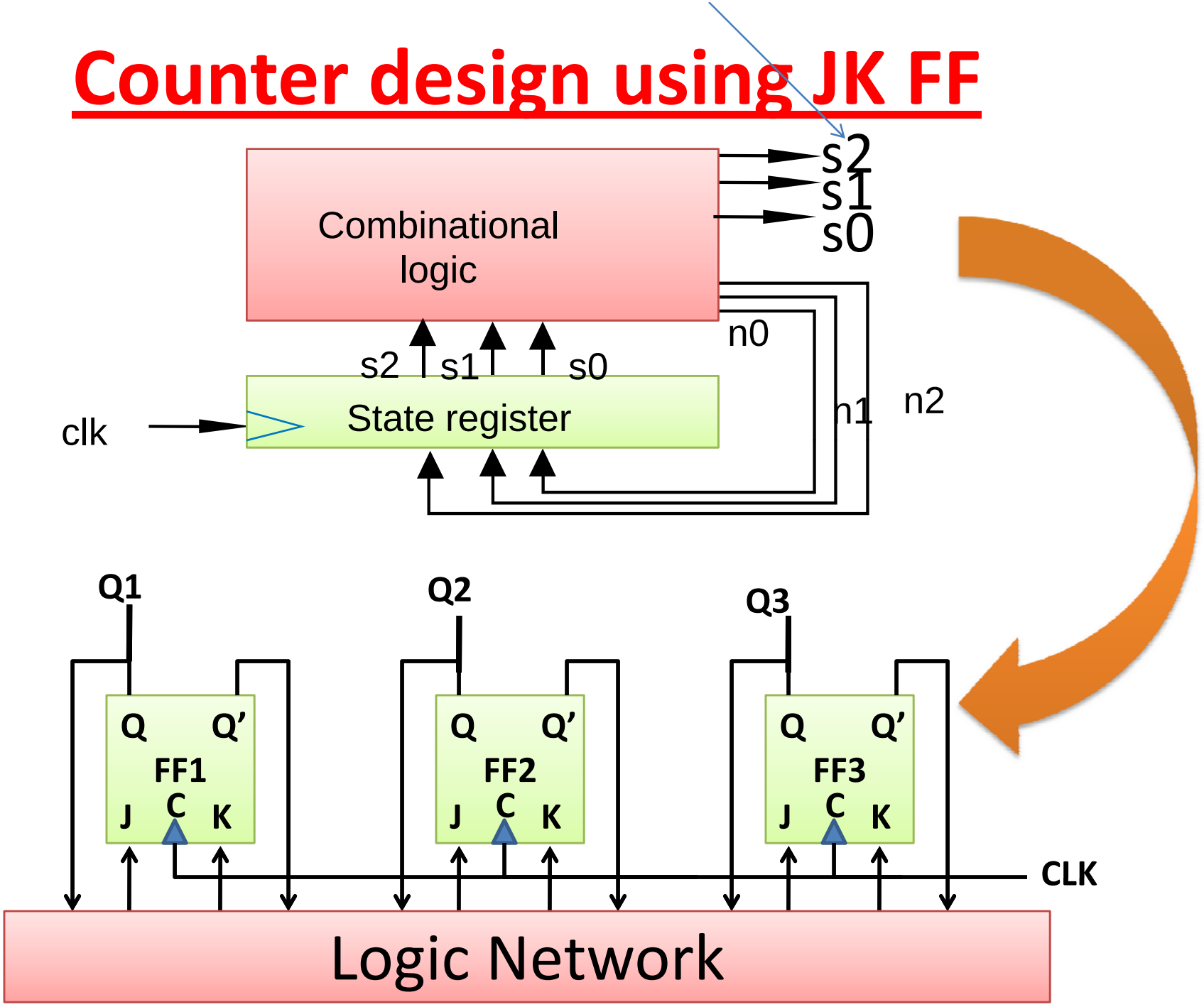
- Takes benefit of dual inputs to FF
- Counter can be implemented using Small Combinational Circuit
- More Inputs from Combinational Circuit
- Use of Excitation Table
  - How FF out changes from one to others
  - Required FF inputs to change FF output
  - 0 to 0, 0 to 1, 1 to 0 and 1 to 1

Design of Counter: With FFs

0,2,3,4,5,1,0…



Counter design using JK FF



4 Types of Flip-Flops

S	R	Q+
0	0	Qt
0	**1**	**0**
1	**0**	**1**
1	1	U

D	Q+
0	0
1	1

J	K	Q+
0	**0**	**Qt**
0	1	0
1	0	1
1	**1**	**Qt’**

T	Q+
0	Qt
1	Qt’

Characteristic Equations

- A descriptions of the next-state table of a flip-flop
- Constructing from the Karnaugh map for Q_{t+1} in terms of the present state and input

Characteristic tables

- The tables that we've made so far are called characteristic tables.
  - They show the next state Q(t+1) in terms of the current state Q(t) and the inputs.
  - For simplicity, the control input C is not usually listed.
  - Again, these tables don't indicate the positive edge-triggered behavior of the flip-flops that we'll be using.

J	K	Q+
0	**0**	**Qt**
0	1	0
1	0	1
1	**1**	**Qt'**

D	Q+
0	0
1	1

T	Q+
0	Qt
1	Qt'

Characteristic equations

- We can also write characteristic equations, where the next state Q(t+1) is defined in terms of the current state Q(t) and inputs.

J	K	Q+
0	**0**	**Qt**
0	1	0
1	0	1
1	**1**	**Qt'**

$$Q^{+} = K'Q + JQ'$$

$$Q(t+1) = K'Q(t) + JQ'(t)$$

Characteristic equations

- We can also write characteristic equations, where the next state Q(t+1) is defined in terms of the current state Q(t) and inputs.

D	Q+
0	0
1	1

$Q^{+}=D$

$Q(t+1) = D$

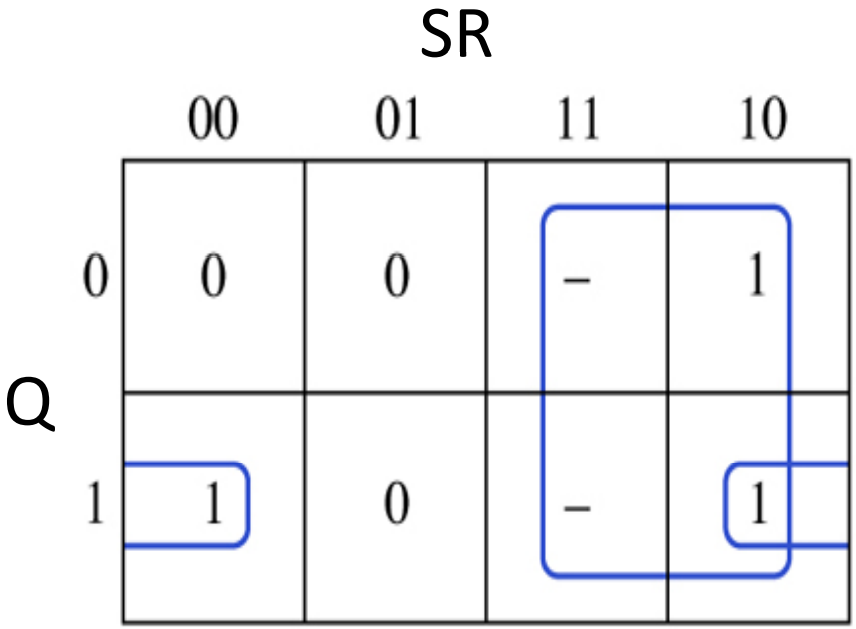
T	Q+
0	Qt
1	Qt’

$Q+= T'Q+TQ' = T \oplus Q$

$Q(t+1) = T'Q(t) + TQ'(t)$

$= T \oplus Q(t)$

Characteristic equations



$Q^+ = S + R'Q \quad (SR=0)$

Flip Flop Type	Characteristic Equation
SR	$Q^+ = S + R'Q \quad (SR=0)$
JK	$Q^+ = JQ' + K'Q$
D	$Q^+ = D$
T	$Q^+ = TQ' + T'Q = T \oplus Q$

Excitation Table for JK Flip Flop

- It is different than Characteristic Equation
- Tabling requires **Input** to change from **Q to Q^+**

J	K	Q+
0	**0**	**Qt**
0	1	0
1	0	1
1	**1**	**Qt'**

Characteristic Table

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation Table

Excitation Table for T Flip Flop

- It is different than Characteristic Equation
- Tabling requires **Input** to change from **Q to Q^+**

T	Q+
0	Qt
1	Qt’

Characteristic Table

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Table

Excitation Table for D Flip Flop

- It is different than Characteristic Equation
- Tabling requires **Input** to change from **Q to Q^+**

D	Q+
0	0
1	1

Characteristic Table

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

Excitation Table

Excitation Table for SR Flip Flop

- It is different than Characteristic Equation
- Tabling requires **Input** to change from **Q to Q^+**

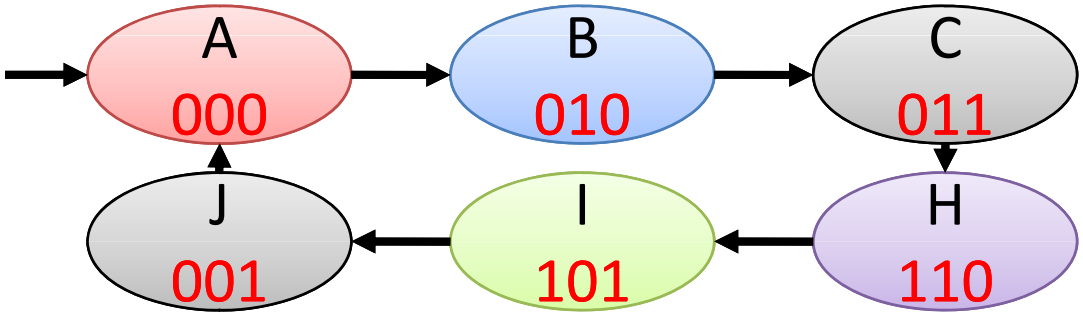
S	R	Q+
0	**0**	**Qt**
0	1	0
1	0	1
1	**1**	**U**

Characteristic Table

Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Excitation Table

Excitation Table: Sync Counter Using JK FF



Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Present State			Next State			Flip Flop Inputs					
Q1	Q2	Q3	$Q1^+$	$Q2^+$	$Q3^+$	J1	K1	J2	K2	J3	K3
0	0	0	**0**	1	0	0	X	1	X	0	X
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	1	0	1	X	X	0	X	1
1	1	0	1	0	1	X	0	X	1	1	X
1	0	1	0	0	1	X	1	0	X	X	0
0	0	1	0	0	0	0	X	0	X	X	1

FF Input Functions

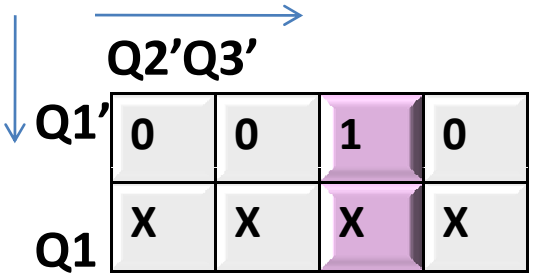
Present State			Flip Flop Inputs					
Q1	Q2	Q3	J1	K1	J2	K2	J3	K3
0	0	0	0	X	1	X	0	X
0	1	0	0	X	X	0	1	X
0	1	1	1	X	X	0	X	1
1	1	0	X	0	X	1	1	X
1	0	1	X	1	0	X	X	0
0	0	1	0	X	0	X	X	1

J1= F (Q1,Q2,Q3) **J2= F (Q1,Q2,Q3)** **J3= F (Q1, Q2,Q3)**

K1= F (Q1,Q2,Q3) **K2= F (Q1, Q2,Q3)** **K3= F (Q1, Q2,Q3)**

Solve Each Function Using KMAP

Present State			Flip Flop Inputs					
Q1	Q2	Q3	J1	K1	J2	K2	J3	K3
0	0	0	0	X	1	X	0	X
0	1	0	0	X	X	0	1	X
0	1	1	1	X	X	0	X	1
1	1	0	X	0	X	1	1	X
1	0	1	X	1	0	X	X	0
0	0	1	0	X	0	X	X	1



J1= Q2Q3

J2= Q3'

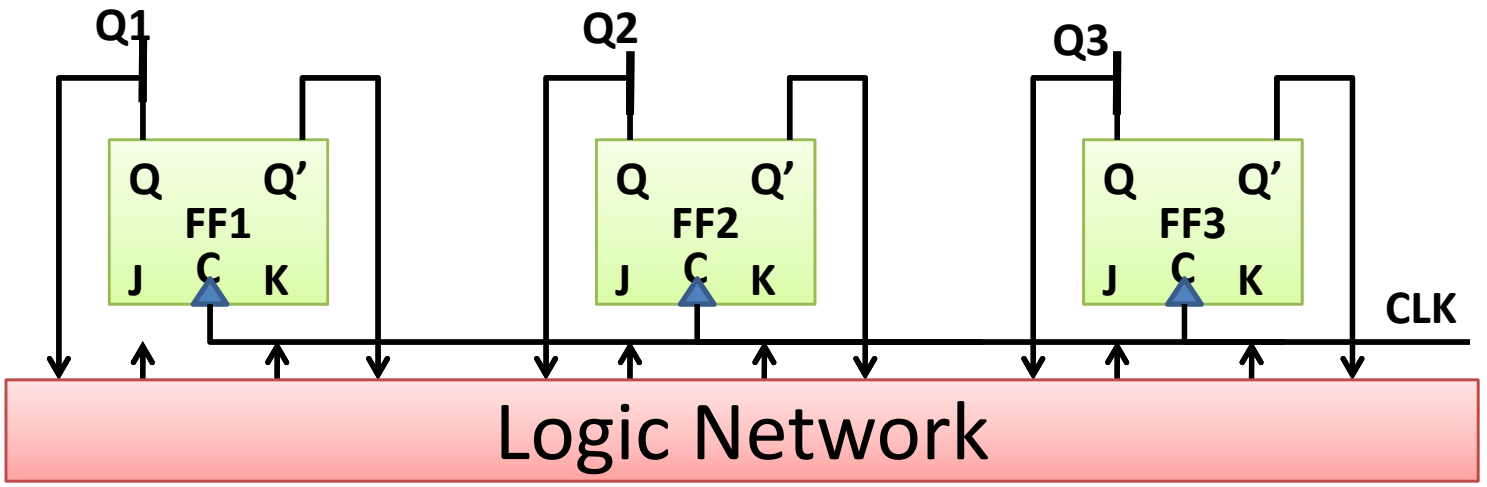
J3= Q2

K1= Q2'

K2= Q1

K3= Q1'

Counter Logic Diagram



J1= Q2Q3

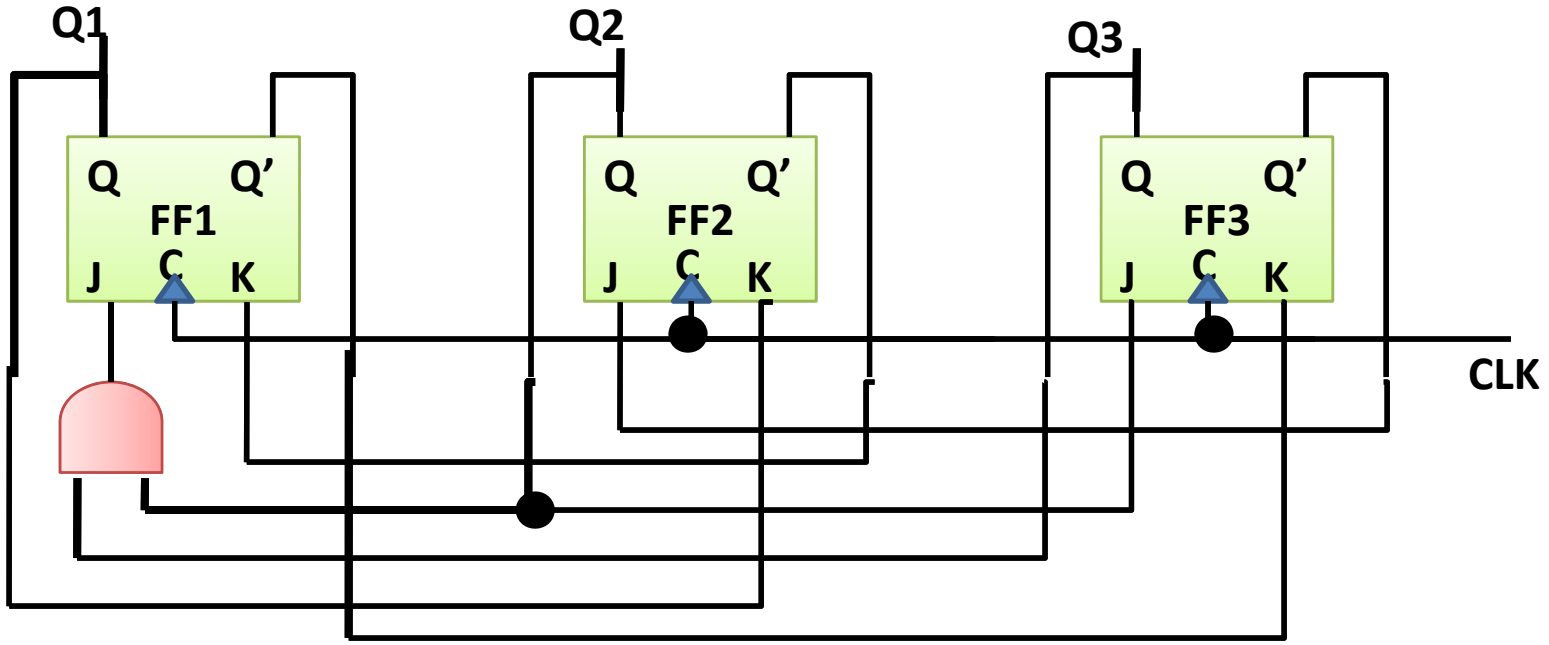
K1= Q2'

J2= Q3'

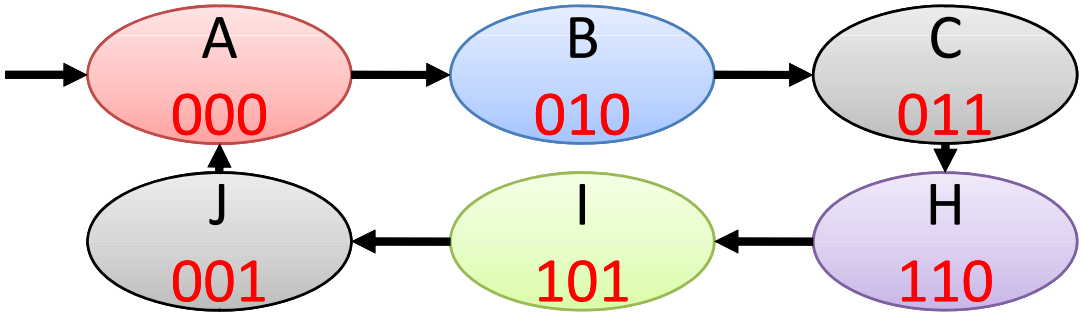
K2= Q1

J3= Q2

K3= Q1'



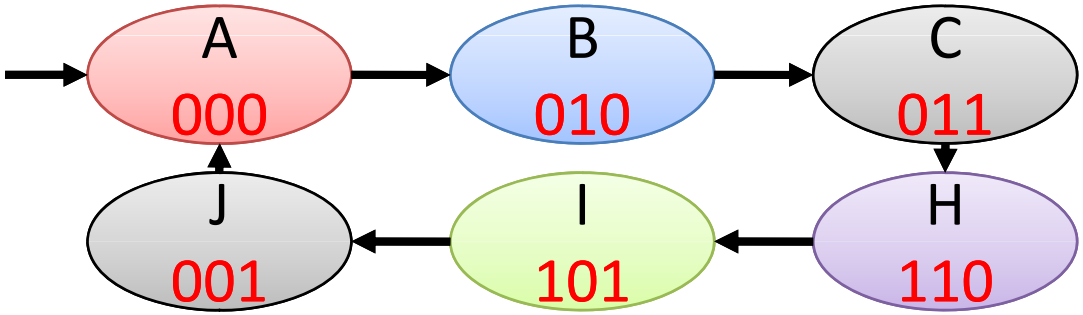
Excitation Table: Sync Counter Using D FF



Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

Present State			Next State			Flip Flop Inputs		
Q1	Q2	Q3	$Q1^+$	$Q2^+$	$Q3^+$	D1	D2	D3
0	0	0	**0**	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	1	0	1	1	0
1	1	0	1	0	1	1	0	1
1	0	1	0	0	1	0	0	1
0	0	1	0	0	0	0	0	0

Excitation Table: Sync Counter Using D FF



Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

Present State			Flip Flop Inputs		
Q1	Q2	Q3	D1	D2	D3
0	0	0	0	1	0
0	1	0	0	1	1
0	1	1	1	1	0
1	1	0	1	0	1
1	0	1	0	0	1
0	0	1	0	0	0

$D_1 = Q_1Q_2 + Q_2Q_3$

$D_2 = Q_1'Q_2 + Q_2'Q_3'$

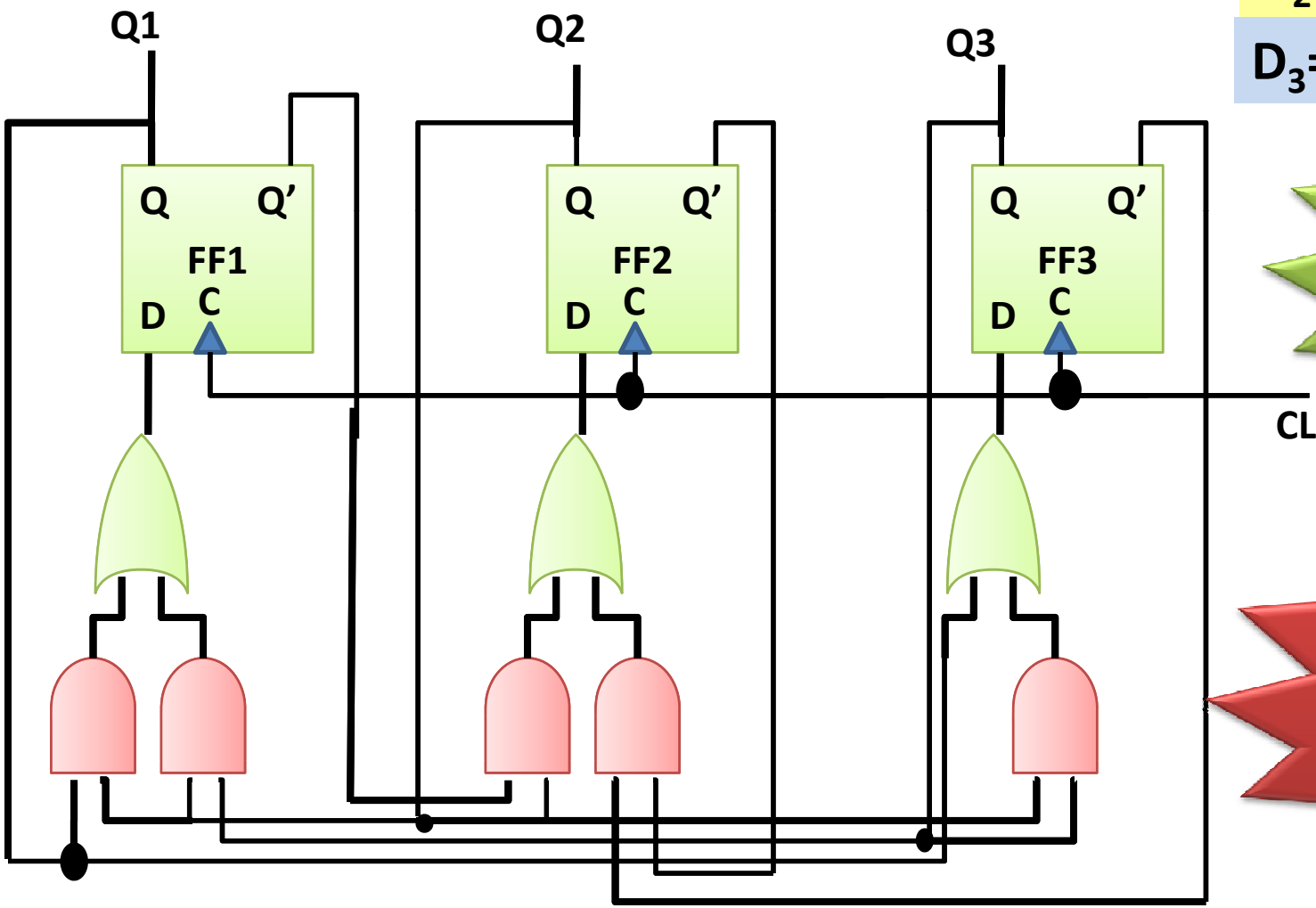
$D_3 = Q_1 + Q_2Q_3$

Counter Implementation using D FF

$D_1 = Q_1Q_2 + Q_2Q_3$

$D_2 = Q_1'Q_2 + Q_2'Q_3'$

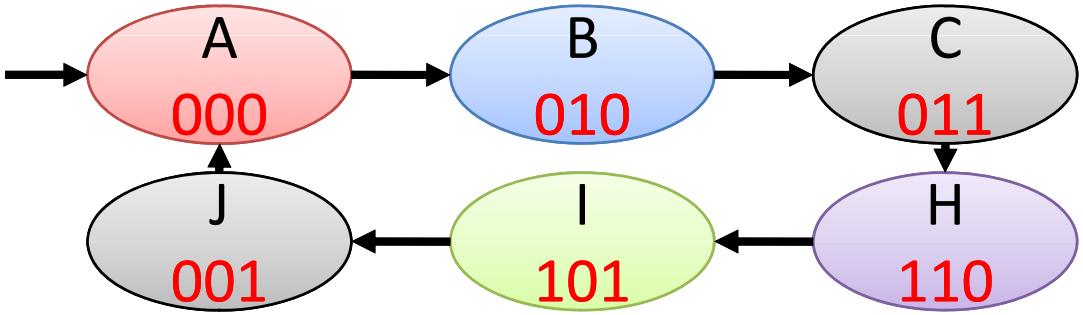
$D_3 = Q_1 + Q_2Q_3$



Same as FSM Controller

Require more Logic as JK FF Based

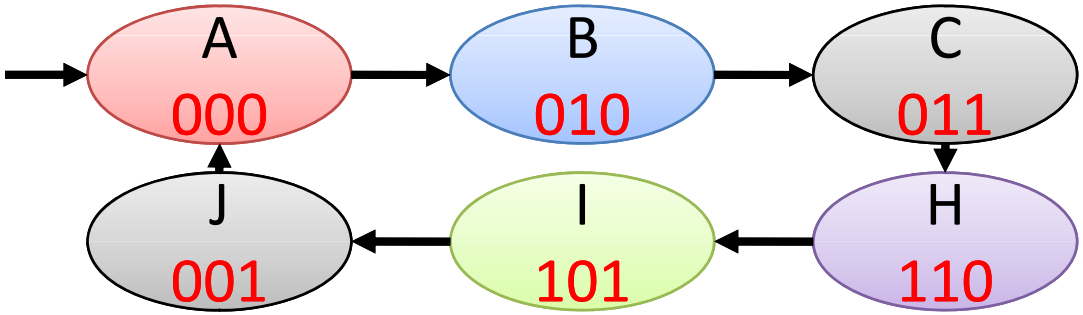
Excitation Table: Sync Counter Using T FF



Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

Present State			Next State			Flip Flop Inputs		
Q1	Q2	Q3	$Q1^+$	$Q2^+$	$Q3^+$	T1	T2	T3
0	0	0	**0**	1	0	0	1	0
0	1	0	0	1	1	0	0	1
0	1	1	1	1	0	1	0	1
1	1	0	1	0	1	0	1	1
1	0	1	0	0	1	1	0	0
0	0	1	0	0	0	0	0	1

Excitation Table: Sync Counter Using D FF



Q	Q^+	T
0	0	0
0	1	1
1	0	0
1	1	1

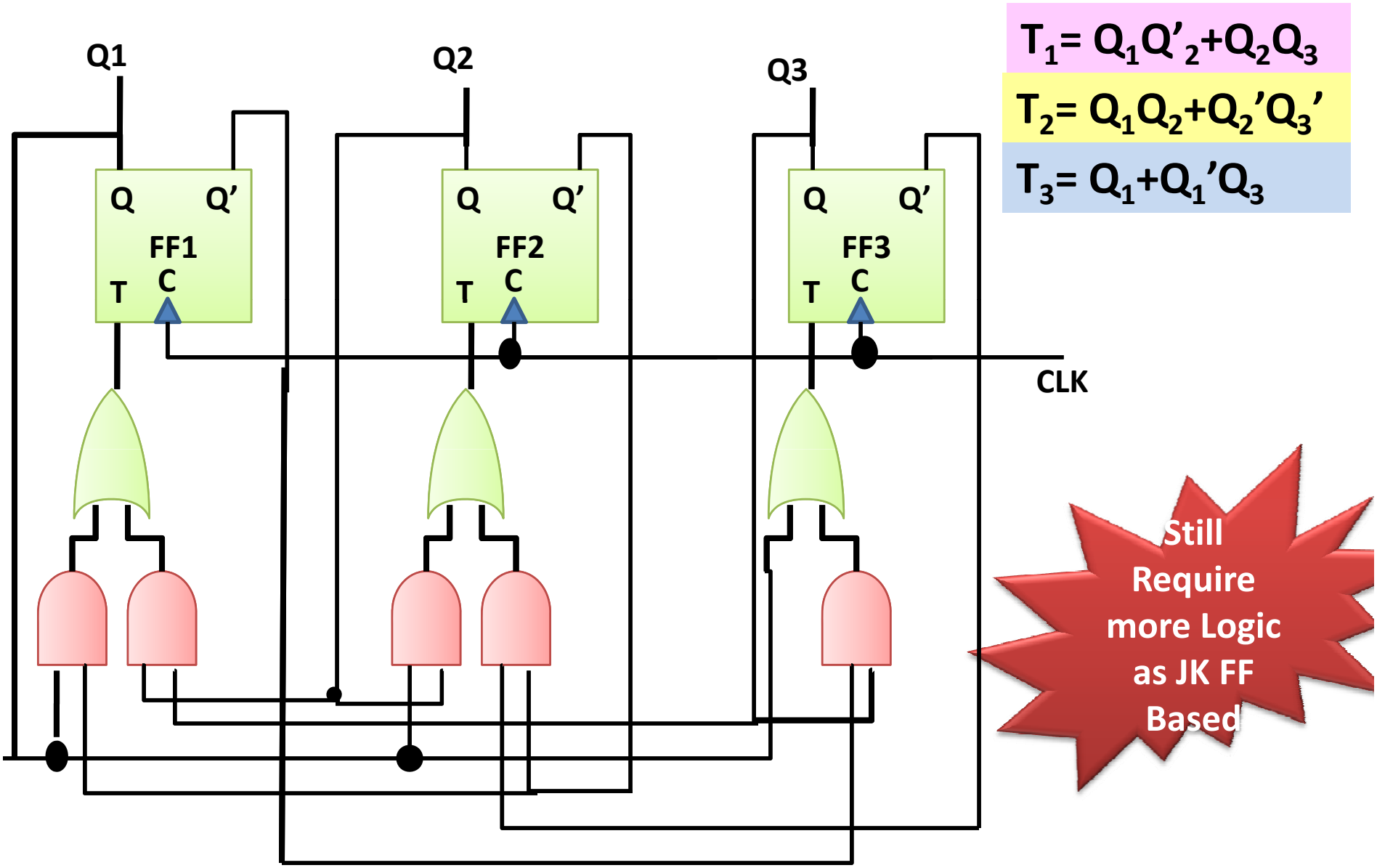
Present State			Flip Flop Inputs		
Q1	Q2	Q3	T1	T2	T3
0	0	0	0	1	0
0	1	0	0	0	1
0	1	1	1	0	1
1	1	0	0	1	1
1	0	1	1	0	0
0	0	1	0	0	1

$T_1 = Q_1Q'_2 + Q_2Q_3$

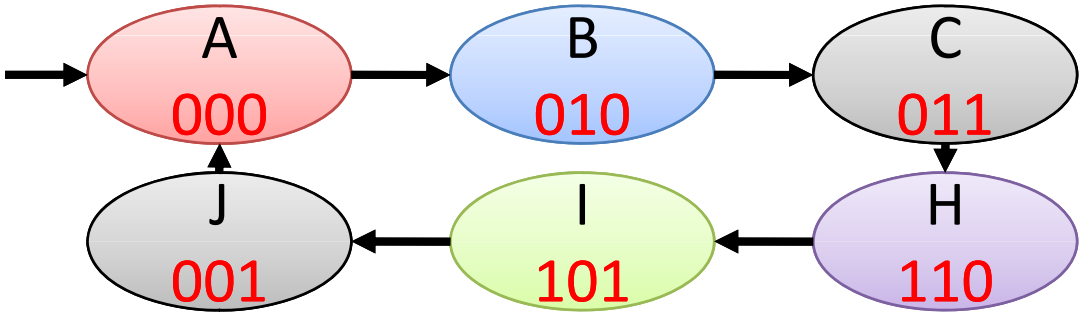
$T_2 = Q_1Q_2 + Q_2'Q_3'$

$T_3 = Q_1 + Q_1'Q_3$

Counter Implementation using D FF



Excitation Table: Sync Counter Using RS FF



Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Present State			Next State			Flip Flop Inputs					
Q1	Q2	Q3	$Q1^+$	$Q2^+$	$Q3^+$	S1	R1	S2	R2	S3	R3
0	0	0	**0**	1	0	0	X	1	0	0	X
0	1	0	0	1	1	0	X	X	0	1	0
0	1	1	1	1	0	1	0	X	0	0	1
1	1	0	1	0	1	X	0	0	1	1	0
1	0	1	0	0	1	0	1	0	X	X	0
0	0	1	0	0	0	0	X	0	X	0	1

FF Input Functions

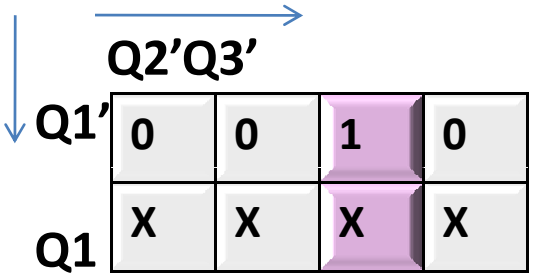
Present State			Flip Flop Inputs					
Q1	Q2	Q3	S1	R1	S2	R2	S3	R3
0	0	0	0	X	1	0	0	X
0	1	0	0	X	X	0	1	0
0	1	1	1	0	X	0	0	1
1	1	0	X	0	0	1	1	0
1	0	1	0	1	0	X	X	0
0	0	1	0	X	0	X	0	1

S1= F (Q1,Q2,Q3) **S2= F (Q1,Q2,Q3)** **S3= F (Q1, Q2,Q3)**

R1= F (Q1,Q2,Q3) **R2= F (Q1, Q2,Q3)** **R3= F (Q1, Q2,Q3)**

Solve Each Function Using KMAP

Present State			Flip Flop Inputs					
Q_1	Q_2	Q_3	R_1	S_1	S_2	R_2	S_3	R_3
0	0	0	0	X	1	X	0	X
0	1	0	0	X	X	0	1	X
0	1	1	1	X	X	0	X	1
1	1	0	X	0	X	1	1	X
1	0	1	X	1	0	X	X	0
0	0	1	0	X	0	X	X	1



$S_1 = Q_2Q_3$

$S_2 = Q_1'Q_3'$

$S_3 = Q_2Q_3'$

$R_1 = Q_2'$

$R_2 = Q_1$

$R_3 = Q_1'Q_3$

Counter Logic Diagram

$S_1 = Q_2Q_3$

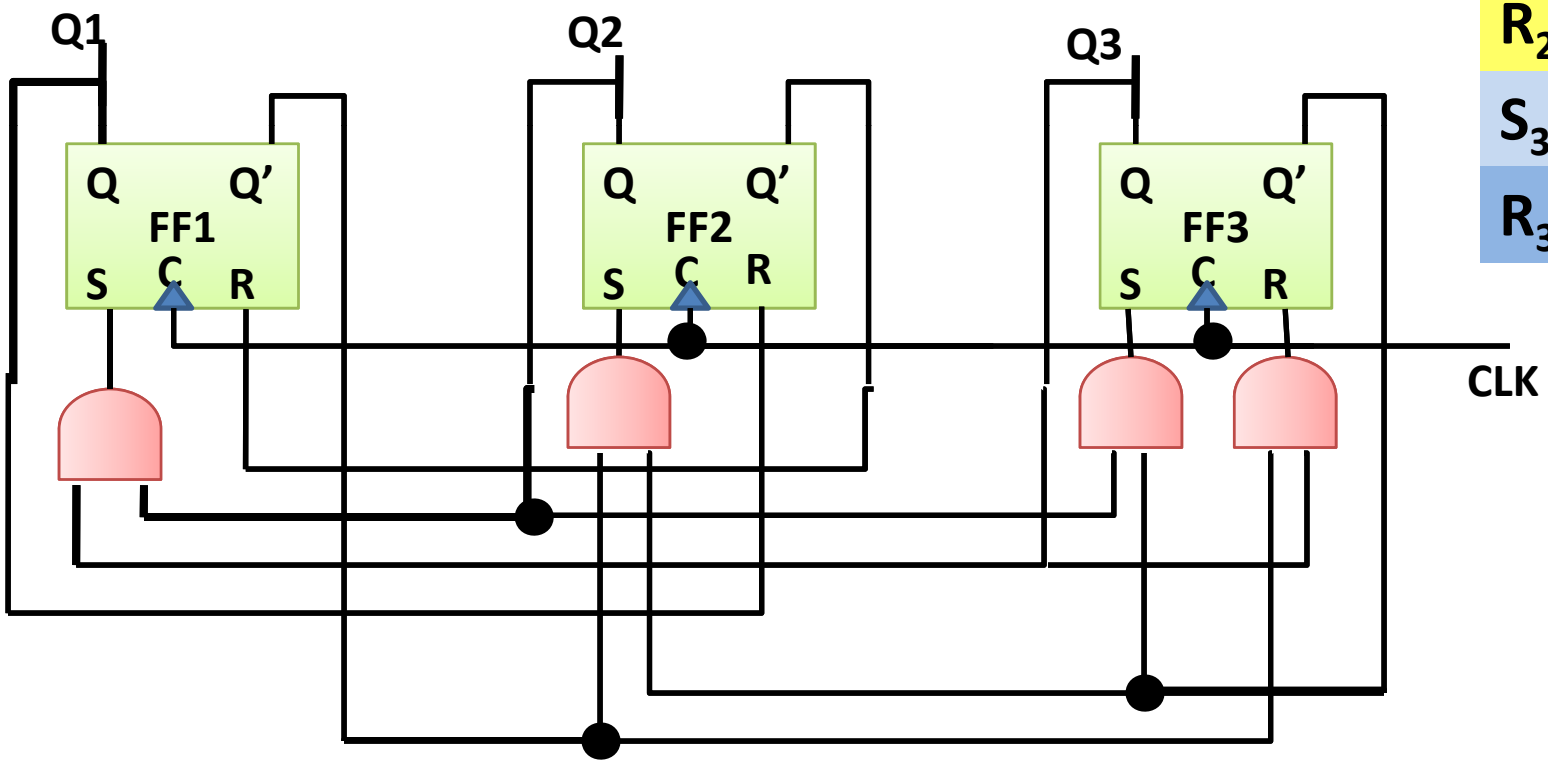
$R_1 = Q_2'$

$S_2 = Q_1'Q_3'$

$R_2 = Q_1$

$S_3 = Q_2Q_3'$

$R_3 = Q_1'Q_3$



Thanks