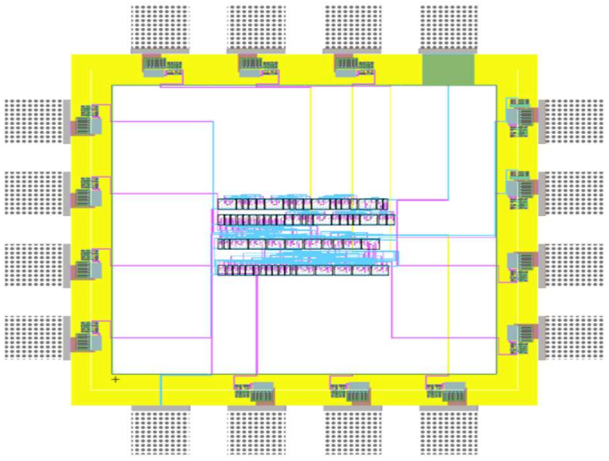

Synthesis of a 4 Bit Down Comparator with LUT6 for PWM Generator

08.07.2023 Md Mahade Sarkar, UAS Kempten

Pulse Width Modulator is a commonly used component in FPGA circuit design and servo motor control like application. Main component of PWM generator design includes counter, comparator, and register. This report represents only the synthesis of a 4 Bit down comparator with LUT6 and time analysis of the comparator output. Also, an investigation on the chip area, number of transistor and propagation delay. A step-by-step design of schematic, layout, truth table verification and padframe generation is presented.

I. Introduction (Task)

4 Bit down comparator compares two 4-bit binary numbers starting from Most Significant Bit to Least Significant Bit and produces the output of less and equal bit. Synthesis of comparator circuit starts from preparing a truth table which is known as LUT6[A] and implementation of the desired output logic cells with CMOS logic blocks from sclib.jelib library. A stepwise preparation of schematic, icon, VHDL code, layout and padframe generation is presented with electric VLSI. Time signal of the inputs, outputs, and truth table verification from the LTspice simulation is done.

II. Design STEPS

A truth table based on the comparison logic of two numbers are prepared in LUT6 table[A] which shows the 6 inputs and 2 outputs. Each 4 bits of equal output is converted to hexadecimal code eqo(eqi, lessi,A1,A0,B1,B0) = LUT6_0000000012481248. Now hex-code block is implemented with the fundamental LUT2 logic circuit from the sclib.jelib library and with the combination of Multiplexer 4 and multiplexer 2.

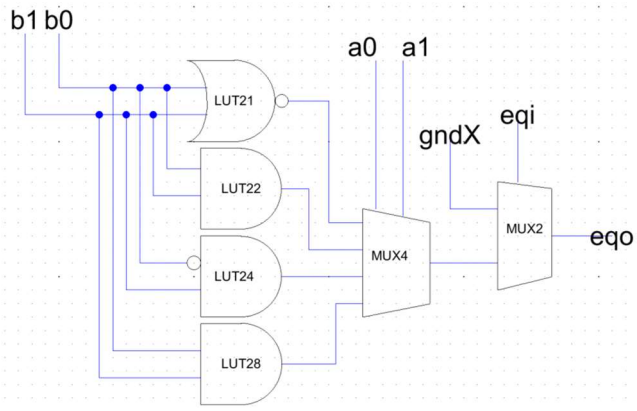

Figure 1: Schematic of equal out with LUT6

Mux2 has 2 inputs and one select line. Based on the low or high input at the select line assigned as equal input, it allows either 00000000 or 12481248. Mux4 has 4 inputs and 2 select lines. Based on the combination of a_0, a_1 select line and b_0 and b_1 input bit, it allows to pass hex-code any of 1248. Input bits are applied, and output of the equal circuit is shown in figure 2. Input signals are a_0, a_1, b_0, b_1, eqi and the output signal is eqo from the LUT6 truth table[A]. Output signal V(eqo) is at the top of the plotted graph and in gray colored. Binary digits are placed at the output signal which verifies the truth table of column eqo implemented with this logic circuit.

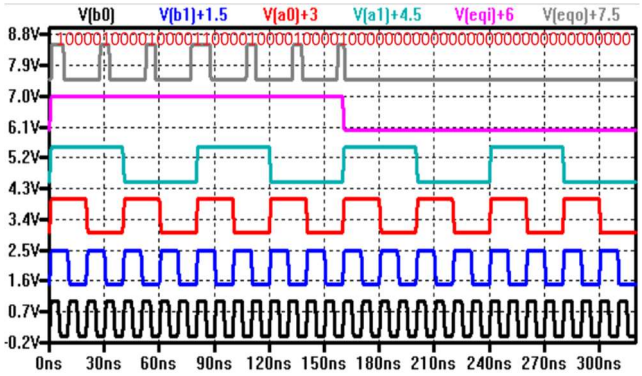

Figure 2: Input-Output signals & truth table verification eqo

Similarly for output lesso implementation, lesso output found from 6 input bit combination is converted to the hexadecimal code of lesso= LUT6_EC80FEC8EC80EC80. With the LUT2 logic circuits from sclib.jelib library, EC80 and FEC8 are implemented and multiplexed with a MUX4.

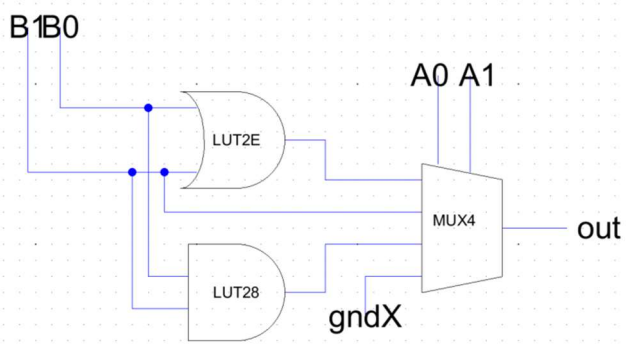

Figure 3: Schematic of EC80, a logic bloc for lesso output

EC80 from figure 3, consists of LUT2E, LUT28, C is implemented by connecting to I1 input and 0 to the ground. All inputs and output are exported. Similarly, FEC8 from figure 4, is implemented with vddX, LUT2E, LUT28 and input pin I1. Lesso consists of EC80, FEC8 and with a MUX4, logic cells are connected to the input sequentially

shown in figure 5. Select lines are coming from lessi and eqi. All the input and output ports are exported and simulated in LTspice. Input signals are applied with pulse signal defined as truth table bit sequence.

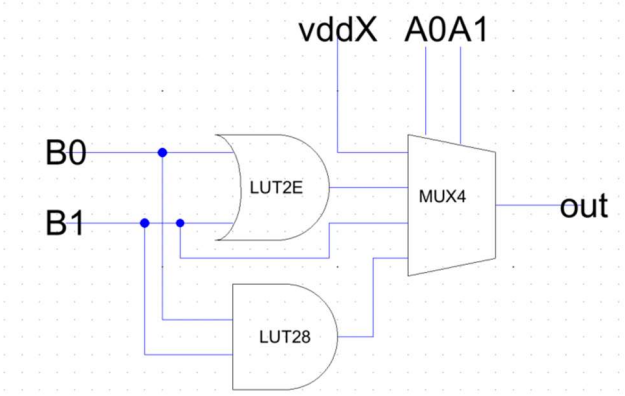

Figure 4: Schematic of FEC8, a logic bloc for lesso output

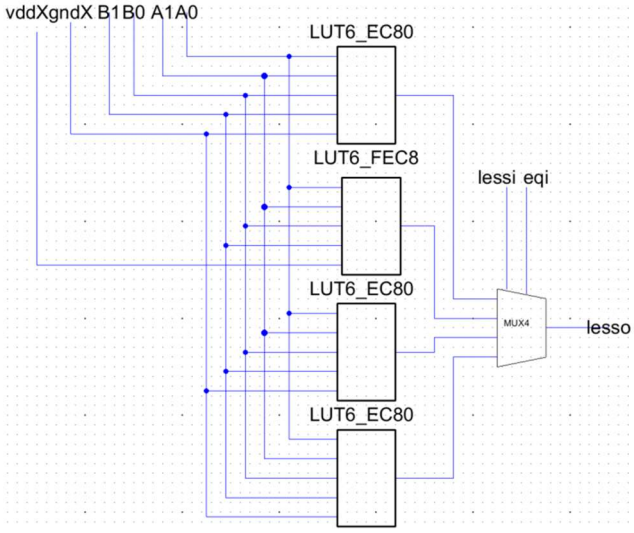

Figure 5: Schematic of lesso output circuit with LUT6

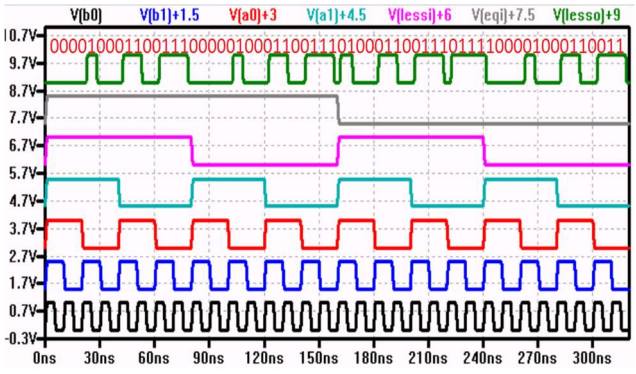

Figure 6: Input-Output signals, truth table verification lesso

CMOS parameters are in cmosedu_model.txt file and included in LTspice simulation. Voltage source Vdd is defined as DC voltage from 0 to 1v. Ground voltage is set to 0v. Two external pin voltage vddX and vgndX are set to 1v and 0v respectively. From truth table it is visible that B_0 has the bit sequence of 0 and 1 alternatively. Input signal B0 is defined as below,

V0 B0 0 PULSE (0 1 0 1n 1n 4n 10n)

Where V0 is the source name, B0 is the input pin, pulse is the signal type, 0 is the lowest level volt, 1 is the highest-level volt, 1n is the rise time, 1n is the fall time, 4n is the bit duration and 10n is the single pulse duration. Similarly, all input signals are defined by increasing the pulse duration according to truth table. Figure 6 shows the input and output signals. The green top signal plot is the output signal lesso and bit stream of lesso are placed on top of the signal which verify the logic circuit.

Figure 7 shows the 2 Bit compare circuit with LUT6 combined from previously created lesso and eqo logic block and IC icon.

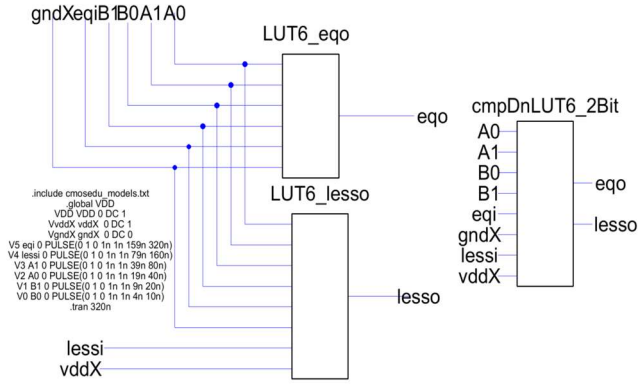

Figure 7: Schematic of 2 Bit compare circuit.

Spice simulation shows the eqo and lesso output signal in figure 8 from 2 Bit compare circuit, which verify the LUT6 truth table.

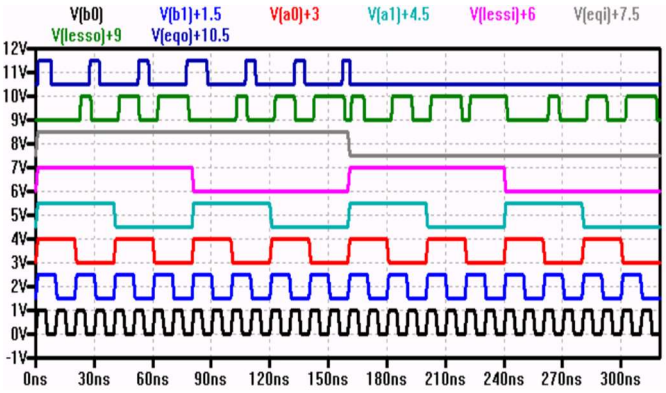

Figure 8: Input-Output signals, 2 Bit compare.

A 4 Bit down comparator can be made from two 2 Bit compare circuits. Comparison starts from the MSB to LSB, so two MSB bits A2, A3 and B2, B3 with lessi, eqi are applied at the first comparator and the output of the first comparator lesso and eqo is fed to the second comparator's lessi and eqi respectively along with A0, A1 and B0, B1 two LSB bits. Figure 9 shows the connection diagram of 4 Bit compare down circuit. Two 4-bit signals are applied and the output signal less and equal are plotted in figure 10. In figure 10 top blue plot is the compared less and red is the equal. Figure 11 shows the magnified view of less and equal plot.

Plot shows the compared output of 4-bit data which is either equal or less/greater than other 4 bit.

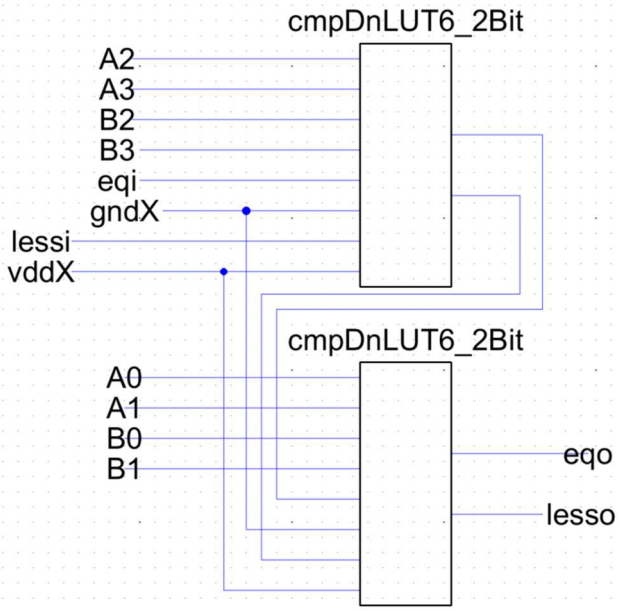

Figure 9: Schematic of 4 Bit compare down LUT6 circuit.

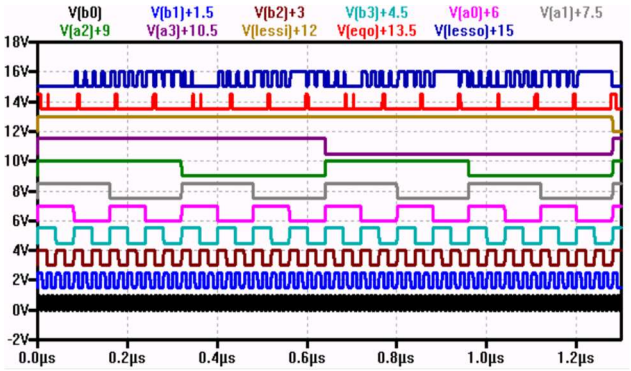

Figure 10: equal and less output from cmpDnLUT6

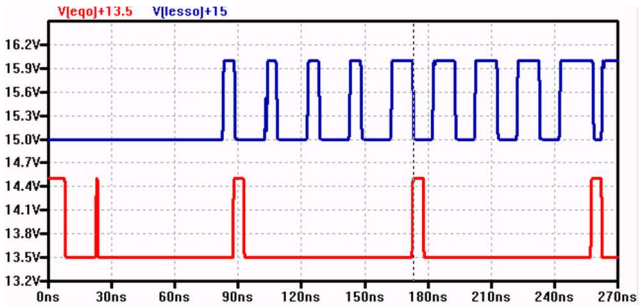

Figure 11: Output from cmpDnLUT6 magnified.

The schematic of cmpDnLUT6 from figure 9 is converted to layout using silicon compiler. Silicon compiler provides the VHDL and netlist file. After optimizing the VHDL code layout of cmpDnLUT6 is found in figure 12. Blue lines are metal-1, pink lines are metal-2, green areas are the logic cells. The layout has 4 rows with length x width = 1457 x 846.5 and the scaling factor is 25nm.

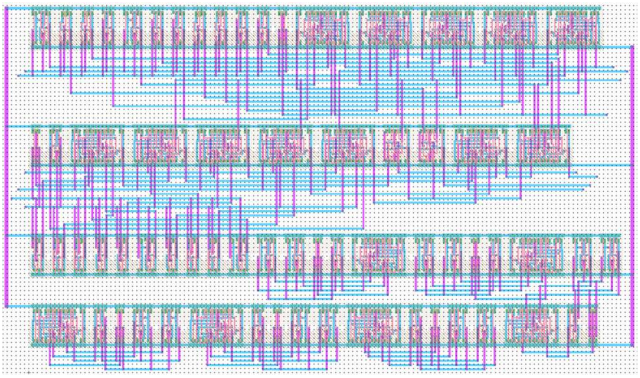

Figure 12: Layout of 4 Bit compare down cmpDnLUT6.

For packaging the comparator logic IC cmpDnLUT6, a padframe is generated with the library file padsMultiplier2x2.arr. Library file is customized for all input and output ports, gndX and vddX to generate a square shape. With padframe generator and sea of gates route option a clean wire routing is generated. Figure at the top of this report is the padframe of cmpDnLUT6.

III. Summary (Results and Learning Outcome)

Synthesis of a 4 Bit down comparator with look up table 6 is done. Truth table of 6 bit is made and required logic blocks are determined. Individual cell's output and final less/equal outputs are verified in LTspice simulation with truth table. A layout is converted from schematic and VHDL code is realized. Finally, a padframe is generated.

References

[1] Laboratorymanual:https://personalpages.hs-kempten.de/~vollratj/Microelectronics/2023_04_04_00_Synthesis_PWM.html

[2] https://kerteriz.net/4-bits-multiplier-design-in-electric-vlsi-with-vhdl-built-layout/

APPENDIX

Appendix A :

LUT6 truth table

eqi	lessi	Comment
0	0	A > B
0	1	A < B
1	0	A = B
1	1	Lower bits not present

eqi	lessi	A1	A0	B1	B0	eqo	HEX-eqo	lesso	HEX-lesso	Logic
0	0	0	0	0	0	0		0		A > B
0	0	0	0	0	1	0	0	1	E	A < B
0	0	0	0	1	0	0		1		A < B
0	0	0	0	1	1	0		1		A < B
0	0	0	1	0	0	0		0		A > B
0	0	0	1	0	1	0	0	0	C	A > B
0	0	0	1	1	0	0		1		A < B
0	0	0	1	1	1	0		1		A < B
0	0	1	0	0	0	0		0		A > B
0	0	1	0	0	1	0	0	0	8	A > B
0	0	1	0	1	0	0		0		A > B
0	0	1	0	1	1	0		1		A < B
0	0	1	1	0	0	0		0		A > B
0	0	1	1	0	1	0	0	0	0	A > B
0	0	1	1	1	0	0		0		A > B
0	0	1	1	1	1	0		0		A > B
0	1	0	0	0	0	0		1		A < B
0	1	0	0	0	1	0	0	1	F	A < B
0	1	0	0	1	0	0		1		A < B
0	1	0	0	1	1	0		1		A < B
0	1	0	1	0	0	0		0		A > B
0	1	0	1	0	1	0	0	1		A < B
0	1	0	1	1	0	0		1	E	A < B
0	1	0	1	1	1	0		1		A < B
0	1	1	0	0	0	0		0		A > B
0	1	1	0	0	1	0	0	0		A > B
0	1	1	0	1	0	0		1	C	A < B
0	1	1	0	1	1	0		1		A < B
0	1	1	1	0	0	0		0		A > B
0	1	1	1	0	1	0	0	0		A > B
0	1	1	1	1	0	0		0	8	A > B
0	1	1	1	1	1	0		1		A < B
1	0	0	0	0	0	1		0		A = B
1	0	0	0	0	1	0	1	1	E	A < B
1	0	0	0	1	0	0		1		A < B
1	0	0	0	1	1	0		1		A < B
1	0	0	1	0	0	0		0		A > B
1	0	0	1	0	1	1	2	0	C	A = B
1	0	0	1	1	0	0		1		A < B
1	0	0	1	1	1	0		1		A < B
1	0	1	0	0	0	0		0		A > B
1	0	1	0	0	1	0	4	0	8	A > B
1	0	1	0	1	0	1		0		A = B
1	0	1	0	1	1	0		1		A < B
1	0	1	1	0	0	0		0		A > B
1	0	1	1	0	1	0	8	0		A > B
1	0	1	1	1	0	0		0	0	A > B
1	0	1	1	1	1	1		0		A = B
1	1	0	0	0	0	1		0		A = B
1	1	0	0	0	1	0	1	1	E	A < B
1	1	0	0	1	0	0		1		A < B
1	1	0	0	1	1	0		1		A < B
1	1	0	1	0	0	0		0		A > B
1	1	0	1	0	1	1	2	0		A = B
1	1	0	1	1	0	0		1	C	A < B
1	1	0	1	1	1	0		1		A < B
1	1	1	0	0	0	0		0		A > B
1	1	1	0	0	1	0	4	0	8	A > B
1	1	1	0	1	0	1		0		A = B
1	1	1	0	1	1	0		1		A < B
1	1	1	1	0	0	0		0		A > B
1	1	1	1	0	1	0	8	0	0	A > B
1	1	1	1	1	0	0		0		A > B
1	1	1	1	1	1	1		0		A = B

lesso (eqi,lessi,A1,A0,B1,B0) = LUT6_EC80FEC8EC80EC80
eqo (eqi,lessi,A1,A0,B1,B0) = LUT6_0000000012481248