COMSATS University Islamabad, Abbottabad Campus

Department of Electrical & Computer Engineering

Course Syllabus (Theory)

Digital Logic Design

CPE-241 (3+1)

BS Computer Engineering

Date Created: 09 August 2021 Revision: DLDTCPE241-00

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1 Course Description

Introduction to Digital Computer and Systems, Number Systems, Binary Arithmetic, Boolean Algebra, Algebraic Manipulation, Canonical and Standard Form and Conversions, Logical Operations and Gates, Simplification of Functions, Karnaugh Map Methods, Two Level Implementations, Don't Care Conditions, Prime Implicants, Combinational Logic Design, Arithmetic Operations and Circuits, Analysis Procedures, Multilevel NAND/NOR Circuits, Decoders, Encoders, Multiplexers, Demultiplexers, Memory Types, Read Only Memory, Random Access Memory, Programmable Logic Array (PLA), Sequential Logic, Flip-Flops, Clocked Sequential Circuits, State Machine Concept, Design of Sequential Circuits using State Machines, Counters and their Design, Synchronous Counters, Asynchronous Counters, Shift Registers etc.

1.1 Prerequisites/Co-requisites

None

1.2 Recommended Textbook and Other Readings

1. M. Morris Mano and Charles R. Kime, Logic and Computer Design Fundamentals (2nd Edition Updated, Prentice Hall, 2000)
2. Thomas L. Floyd, Digital Fundamentals (7th Edition)

1.3 Course Requirements

1. Active COMSIS account
2. Freuqent visit to COMSIS & CU portal for course updates
3. Computer resources
4. Valid CUI official email address

2 Course Learning Objectives

1. Develop the ability to design both combinational and sequential digital logic circuits.
2. Learn to design with common library hardware components.

3 Course Learning Outcomes (CLOs)

After completing the course, students will be able to:

1. Describe number system, logic gates, boolean algebra/expression and their corresponding logic diagrams. (C2-PLO1)
2. Apply boolean properties and Karnaugh Maps to simplify digital logics. (C3-PLO1)
3. Analyse combinational and sequential circuits (C4-PLO2)
4. Design combinational and sequential logic circuits (C5-PLO3)

3.1 Standard Program Outcomes (PLOs) Addressed in Course:

PLO1	**Engineering Knowledge**: An ability to apply knowledge of mathematics, science, and engineering fundamentals and an engineering specialization to the solution of complex engineering problems
PLO2	**Problem Analysis**: An ability to identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principle of mathematics, natural sciences and engineering sciences.
PLO3	**Design/Development of Solutions**: An ability to design solutions for complex engineering problems and design systems, components or processes that meet specific needs with appropriate consideration for public health and safety, cultural, societal, and environmental considerations.

3.2 CLOs/PLOs Mapping

CLOs	**PLOs**											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
CLO 1	C2											
CLO 2	C3											
CLO 3		C4										
CLO 4			C5									

3.3 Knowledge Profile (WK) Addressed in Course:

WK3	Theory-based engineering fundamentals
WK4	Engineering specialist knowledge that provides theoretical frameworks and bodies of knowledge for the practice areas; much is forefront
WK5	Knowledge that supports Engineering design in the practice areas

3.4 CLOs/WKs Mapping

CLOs	**WKs**							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
CLO 1			✓					
CLO 2			✓					
CLO 3				✓				
CLO 4					✓			

4 Course Structure

4.1 weekly Lecture Plan

Week#	Topics
1	• Digital Computers and Information Digital computers and Binary Numbers Other base numbers (base-8, base-16 etc.)
2	• Number base conversions 1's and 2's Complements Unsigned and Signed numbers and Arithmetic operations (Addition, subtraction, Multiplication and Division)
3	• COMBINATIONAL LOGIC CIRCUITS Binary Logic and Introduction to Logic Gates Timing Diagrams Introduction to Boolean Algebra Standard forms
4	• Positive and Negative Logic Boolean Functions and their implementation Canonical and Standard Forms (Minterms, Maxterms, Conversions) Minimization of Boolean functions using K-Map
5	• Don't Care States Universal gates and implementation of Boolean functions using universal gates
6	• COMBINATIONAL LOGIC DESIGN Binary Subtractor Binary Adder/Subtractor Binary Multipliers
7	• Code Conversion Magnitude Comparator

Week#	Topics
8	• Parity Generators/ Checkers, Design Applications
9	• SEQUENTIAL CIRCUITS Introduction to Sequential Circuits Introduction to Latches Introduction to Flip Flops Type of Flip Flops Analysis of Sequential Circuits
10	• Design Procedures Introduction to develop state diagram and state table State reduction excitation tables
11	• REGISTERS AND COUNTERS, Registers
12	• Counters, Synchronous/Asynchronous
13	• Shift Registers Serial Shift Registers
14	• REGISTERS AND COUNTERS Loading Registers
15	• Parallel Registers Ripple Counters
16	• Synchronous Binary Counters Other Counters

4.2 Class Structure

- Credit hours: (3+0)
- Lectures: Total 32 lectures. Two lectures per week, each of one and half hour
- Discussion and Q & A activities.

4.3 Course Assessment Methods and Evaluation Criteria

Assesment Method	Mraks %age
04 Quizzes	15%
04 Homework assignments	10%
2 Sessional exams (in class, 60-80 minutes each, 10%+15%)	25%
Terminal exam (3 hours)	50%
Total (theory)	100%

4.3.1 Course Learning Outcomes Assessment Plan

Sr. #	Course Learning Outcomes	Assessment
1.	CLO 1	Assignment No. 1
2.	CLO 1	Quiz No. 1
3.	CLO 1	Sessional No. 1
4.	CLO 2	Assignment No. 2
5.	CLO 2	Quiz No. 2
6.	CLO 3	Assignment No. 3
7.	CLO 3	Quiz No. 3
8.	CLO 2, CLO 3	Sessional No. 2
9.	CLO 4	Assignment No. 4
10.	CLO 4	Quiz No. 4
11.	CLO 1-4	Terminal Examination

5 Class Policy

- Class attendance is mandatory. Student should come to the classroom before the instructor. Latecomers will not be allowed to enter the classroom. Students, who are absent over 20% of the class time will not be allowed to enter the final examination
- Student should turn off cellular phone before entering the classroom. You should not leave the classroom to make or take cellular phone calls
- Student should bring a notepad and/or a writing instrument to every class and take detailed notes
- Student should pay attention to the instructor and participate in class discussions
- Student should not do other work during class time

6 Academic Integrity and Honesty

- Students are required to comply with the university policy on academic integrity.
- Don't cheat. Any form of cheating, plagiarism, and/or academic dishonesty will result in an "F" grade in the course.