Experiment → 10

Date → 8th October 2020

Aim → Applications of flip-flop

i) Three-bit binary counter using J K flip-flop

ii) Frequency Divider.

Apparatus required →

Source	Specification	Quantity
1) CD4000	CD4027A [JK]	7
2) Source	digiclock	2
3) 7400	7408 [and gate]	1
4) Power/Ground	• $D-HI	2
	• $D-LO	4

	Present state			Next state			Flip-flop inputs					
CLK	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	0	0	X	1	X	X	1
2	0	1	0	0	1	1	0	X	X	0	1	X
3	0	1	1	1	0	0	1	X	X	1	X	1
4	1	0	0	1	0	1	X	0	0	X	1	X
5	1	0	1	1	1	0	X	0	1	X	X	1
6	1	1	0	1	1	1	X	0	X	0	1	X
7	1	1	1	0	0	0	X	1	X	1	X	1

Q_C \ Q_BQ_A	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_C = Q_BQ_A$

Q_C \ Q_BQ_A	00	01	11	10
0	X	X	X	X
1	0	0	1	0

$K_C = Q_BQ_A$

Q_C \ Q_BQ_A	00	01	11	10
0	0	1	X	X
1	0	1	X	X

$J_B = Q_A$

Q_C \ Q_BQ_A	00	01	11	10
0	X	X	1	0
1	X	X	1	0

$K_B = Q_A$

Q_C \ Q_BQ_A	00	01	11	10
0	1	X	X	1
1	1	X	X	1

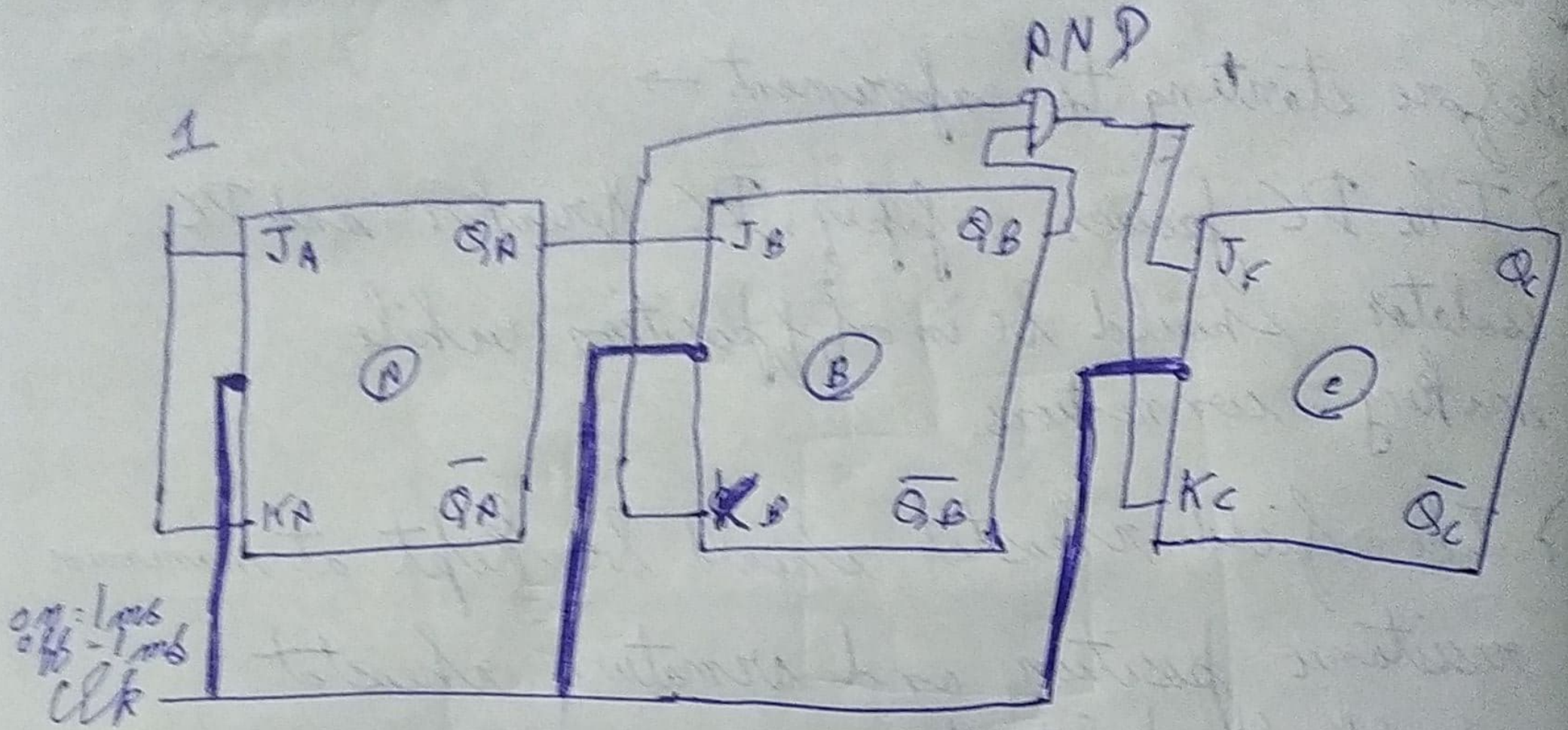
$J_A = 1$

Q_C \ Q_BQ_A	00	01	11	10
0	X	1	1	X
1	X	1	1	X

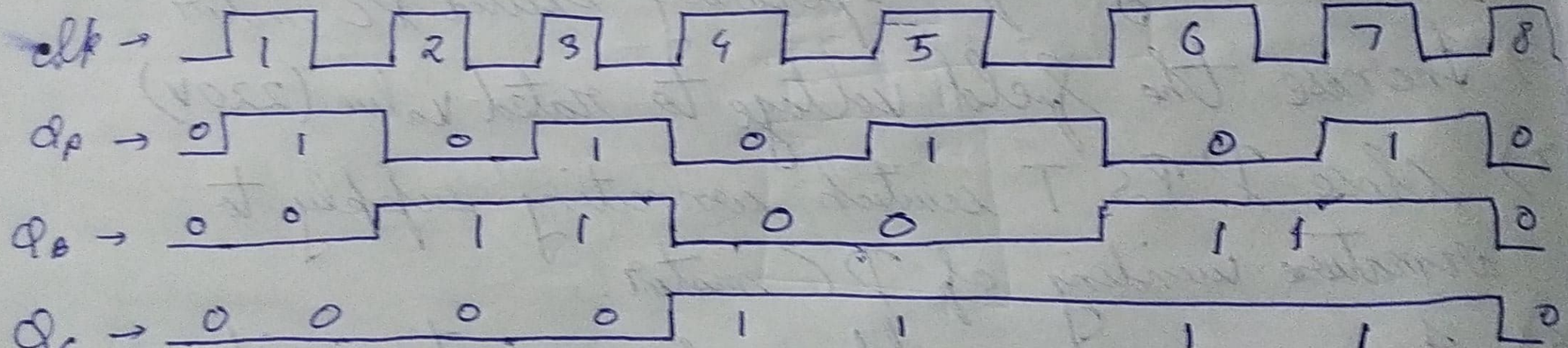
$K_A = 1$

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

} Excitation Table of JK flip-flop

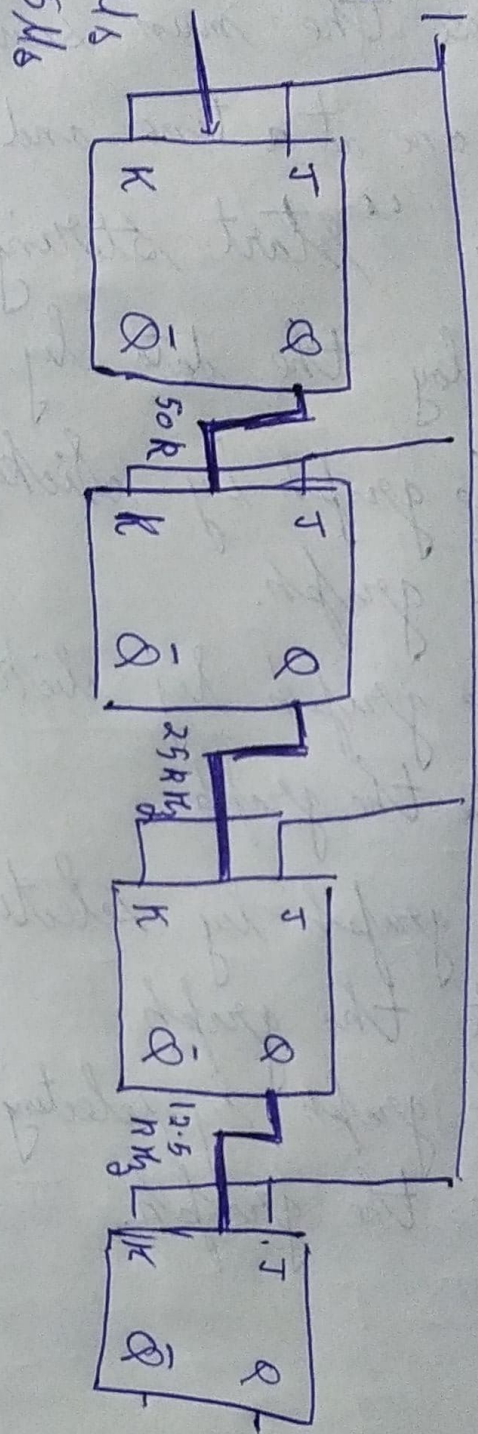


Positive edge triggered JK flip-flop.



Run-to time → 20 ns

Frequency dividers



$f = \frac{1}{T} = \frac{1}{10\,\mu s} = \frac{10^6}{10} = 10^5\,Hz = 100\,KHz$

Run to time → 200 μs

Result → We need to set settings as transient along with option of gatelevelsim, inside digiinistate as 0 instead of X in order for it to store the previous state values.