

Experiment no \rightarrow 9
Date \rightarrow 26th September 2020

19BEE0032
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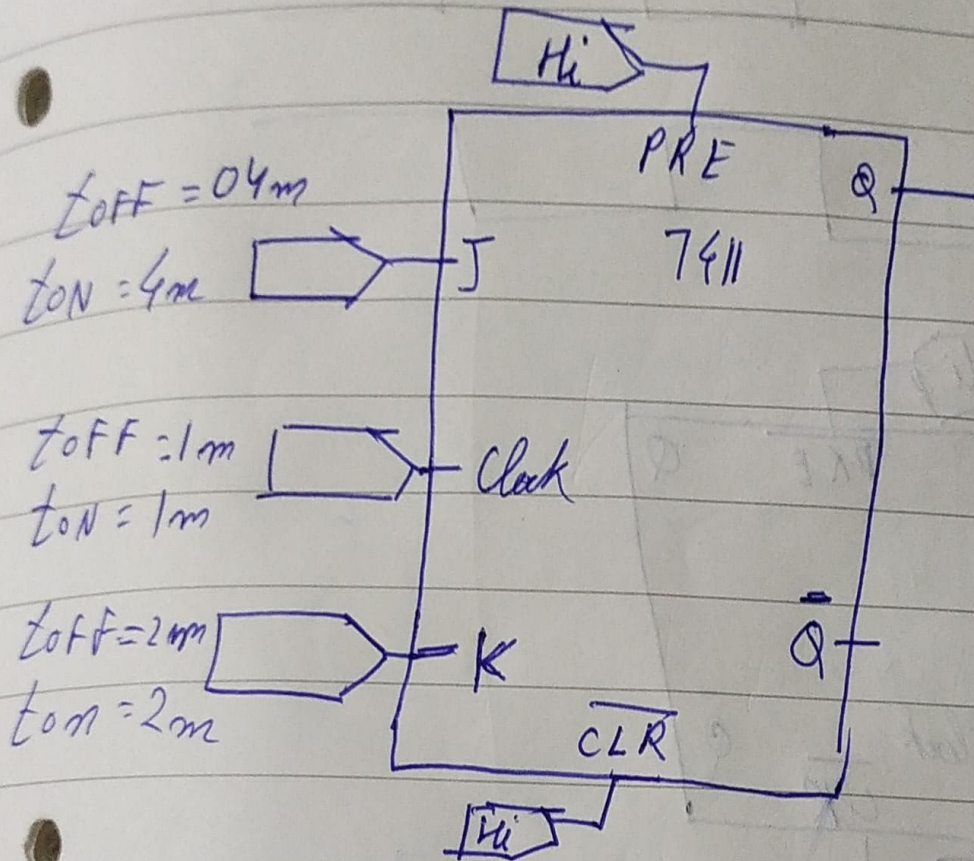
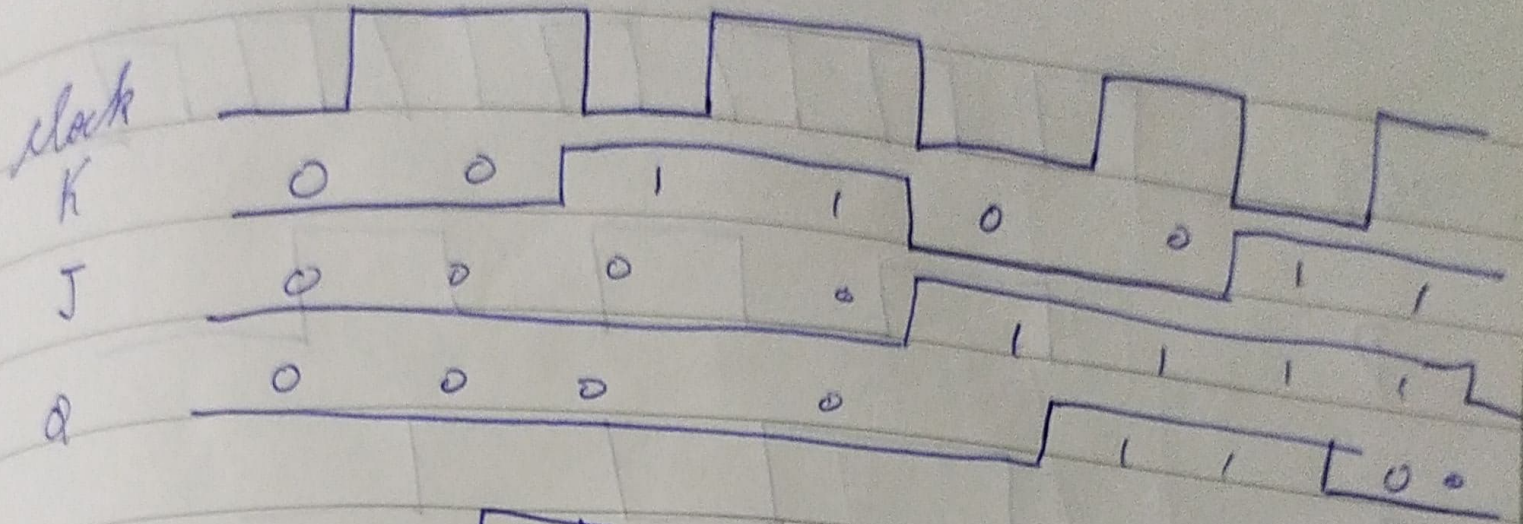
Aim \rightarrow Characteristics of flip-flop
i) JK flip-flop ii) D flip-flop

Apparatus required

Name	Specialization	Quantity
7400	• 74111 [JK]	1
	• 7474 [D]	1
Source	digiclock	5
Power/ground	source \rightarrow high [5V-HI]	4

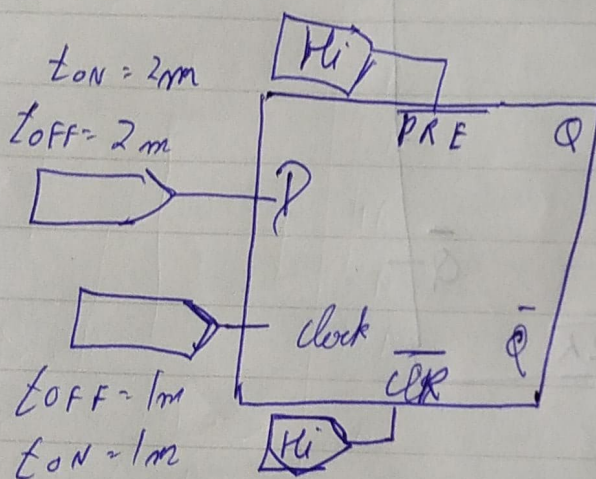
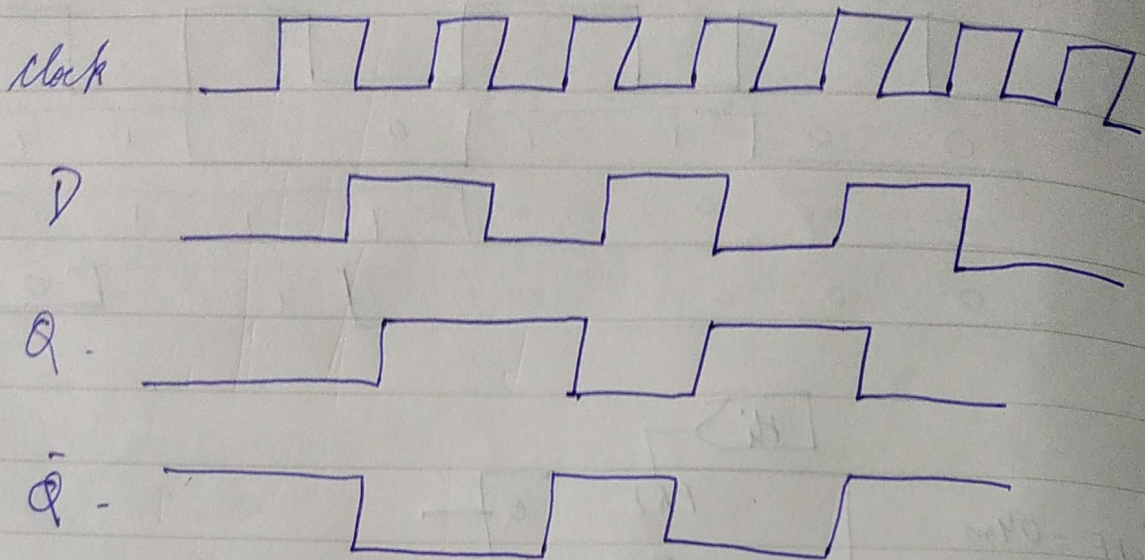
Truth table / Boolean equation / logic diagram \rightarrow
i) JK flip-flop

Clock	J-K inputs		outputs		Status
1	0	0	Q	Q	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	\bar{Q}	Q	Toggle

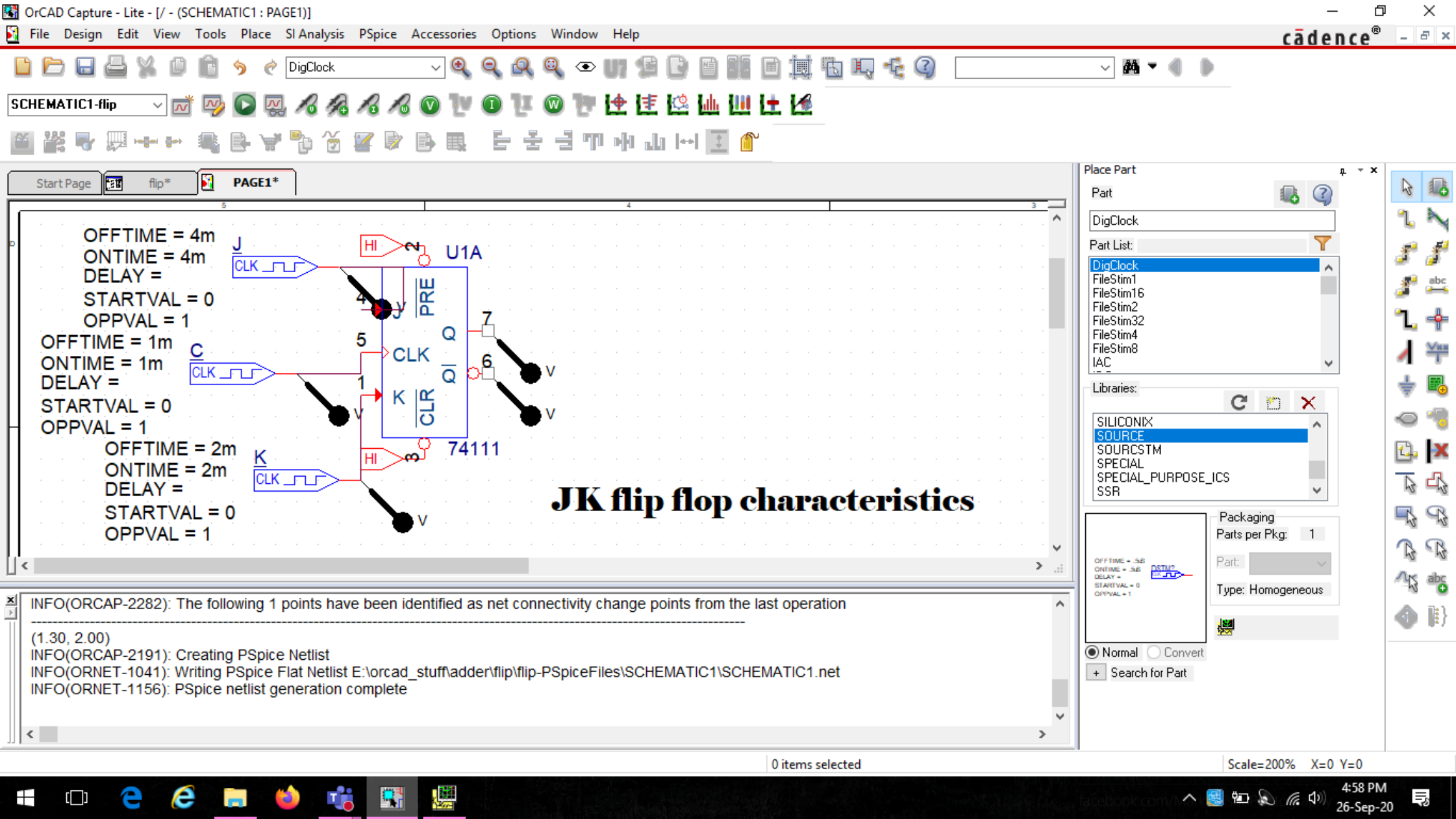


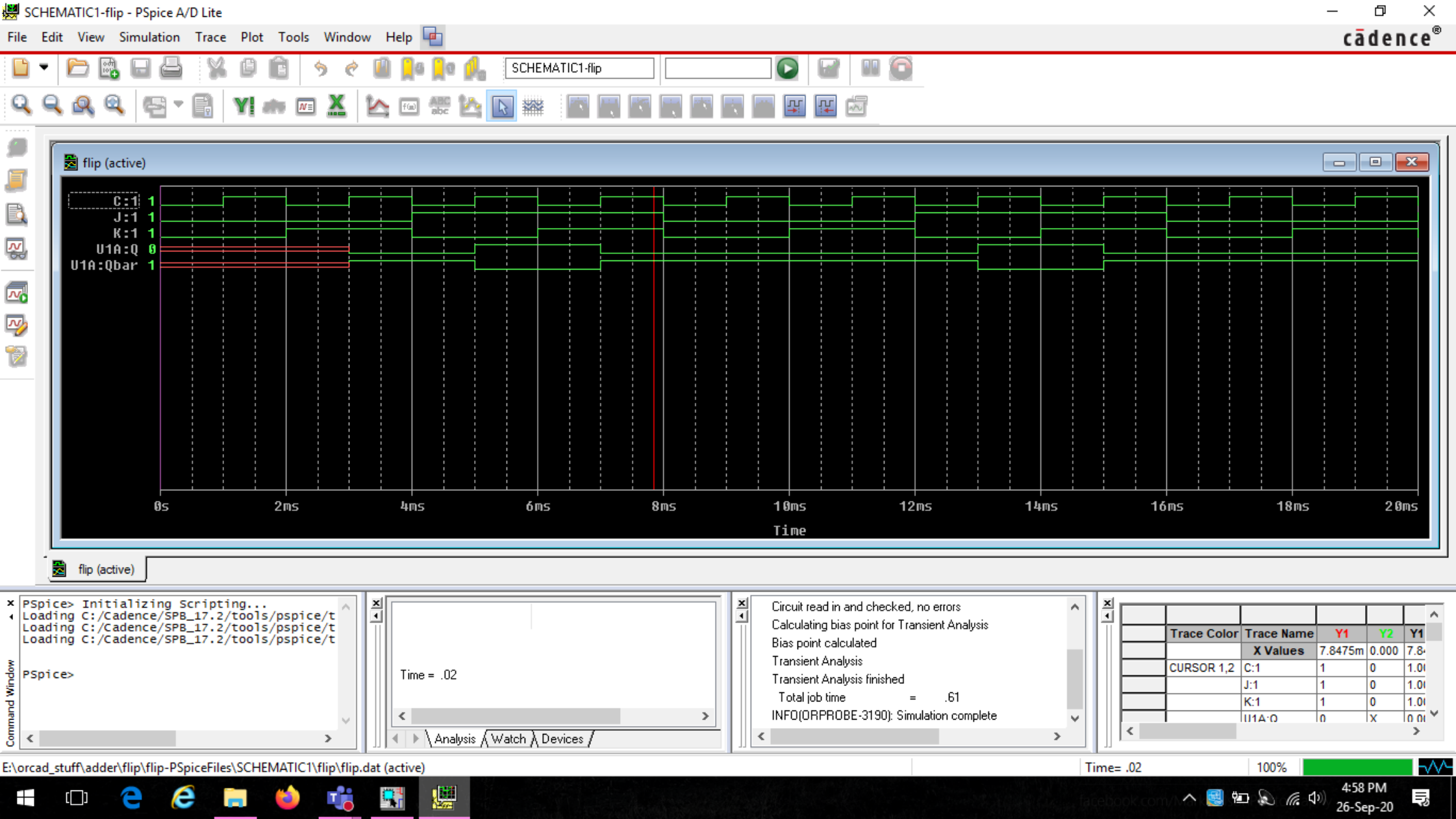
ii) D flip-flop

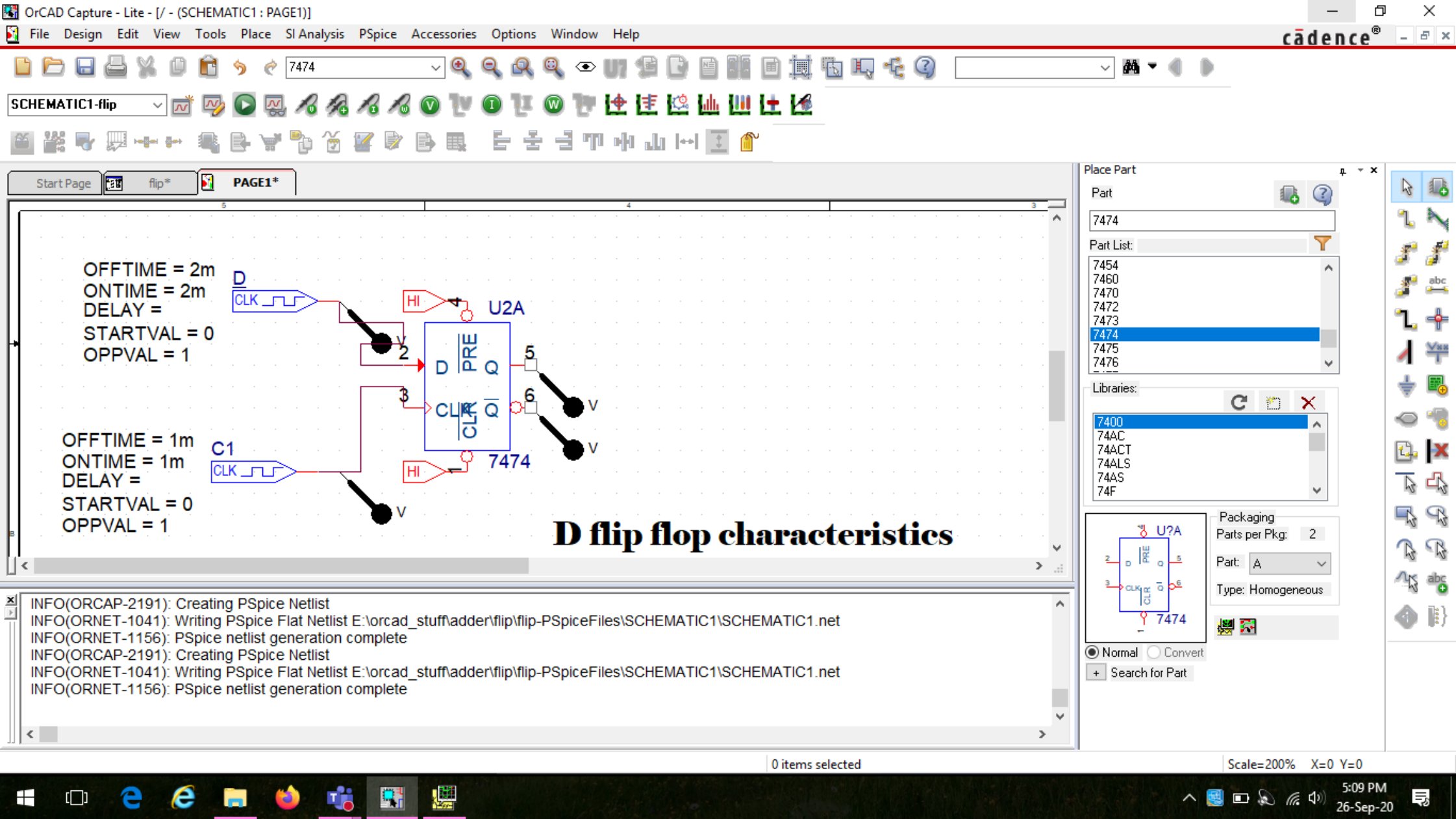
Clock	Input (D)	Output (Q, \bar{Q})
1	0	0, 1
1	1	1, 0

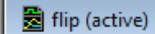


Inference & result \rightarrow We use run-to-time as $20ms$. This is because we want result for both $clock = 0$ & $clock = 1$. Also both 7474 & 7411 are positive edge triggered.









D:1
C1:1
U2A:Q
U2A:Qbar

05

2ms

4ms

6ms

8ms

10ms

12ms

14ms

16ms

18ms

20ms

Time

 flip (active)

Command Window

PSpice>

Time = .02

Time= .02

100%