

Experiment \rightarrow 7

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19BEE0032

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Aim \rightarrow Half adder and full adder using logic gates.

Apparatus required \rightarrow

Name	Specialization	Quantity
Digiclock Source	digiclock	5
7400	7486 (XOR)	3
	7408 (AND)	3
	7432 (OR)	1

Truth table / Boolean equation / Logic diagram \rightarrow

i) Half adder

Truth table \rightarrow

Input		Output	
A	B	carry	sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$$A \rightarrow \underline{0 \ 0 \ 1 \ 1}$$

$$B \rightarrow \underline{0 \ 1 \ 0 \ 1}$$

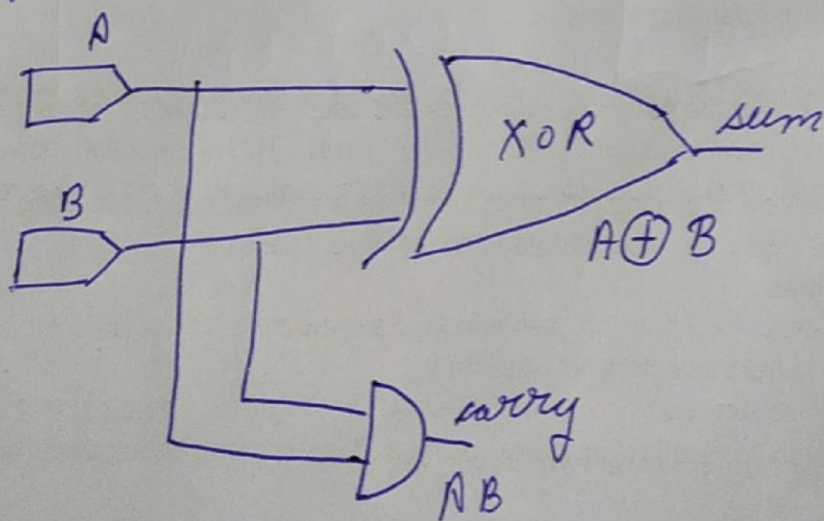
$$\text{sum} \rightarrow \underline{0 \ 1 \ 1 \ 0}$$

$$\text{carry} \rightarrow \underline{0 \ 0 \ 0 \ 1}$$

Boolean equation \rightarrow sum $\rightarrow \bar{A}B + A\bar{B}$
 $= A \oplus B$

carry $\rightarrow AB$

Logic diagram \rightarrow



2) Full adder

Truth table

A	B	C	sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$A = \underline{0000} \overline{1111}$$

$$B \rightarrow \underline{00} \overline{11} \underline{00} \overline{11}$$

$$C \rightarrow \underline{0} \overline{1} \underline{0} \overline{1} \underline{0} \overline{1} \underline{0} \overline{1}$$

$$\text{sum} \rightarrow \underline{0} \overline{1} \underline{1} \overline{0} \underline{1} \overline{0} \underline{0} \overline{1}$$

$$\text{carry} \rightarrow \underline{000} \overline{1} \underline{0} \overline{1} \underline{1} \overline{1}$$

$$\text{sum} \rightarrow \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$= \bar{A}(B \oplus C) + A(\underline{B \odot C})$$

$$= \bar{A}(B \oplus C) + A(\underline{B \oplus C})$$

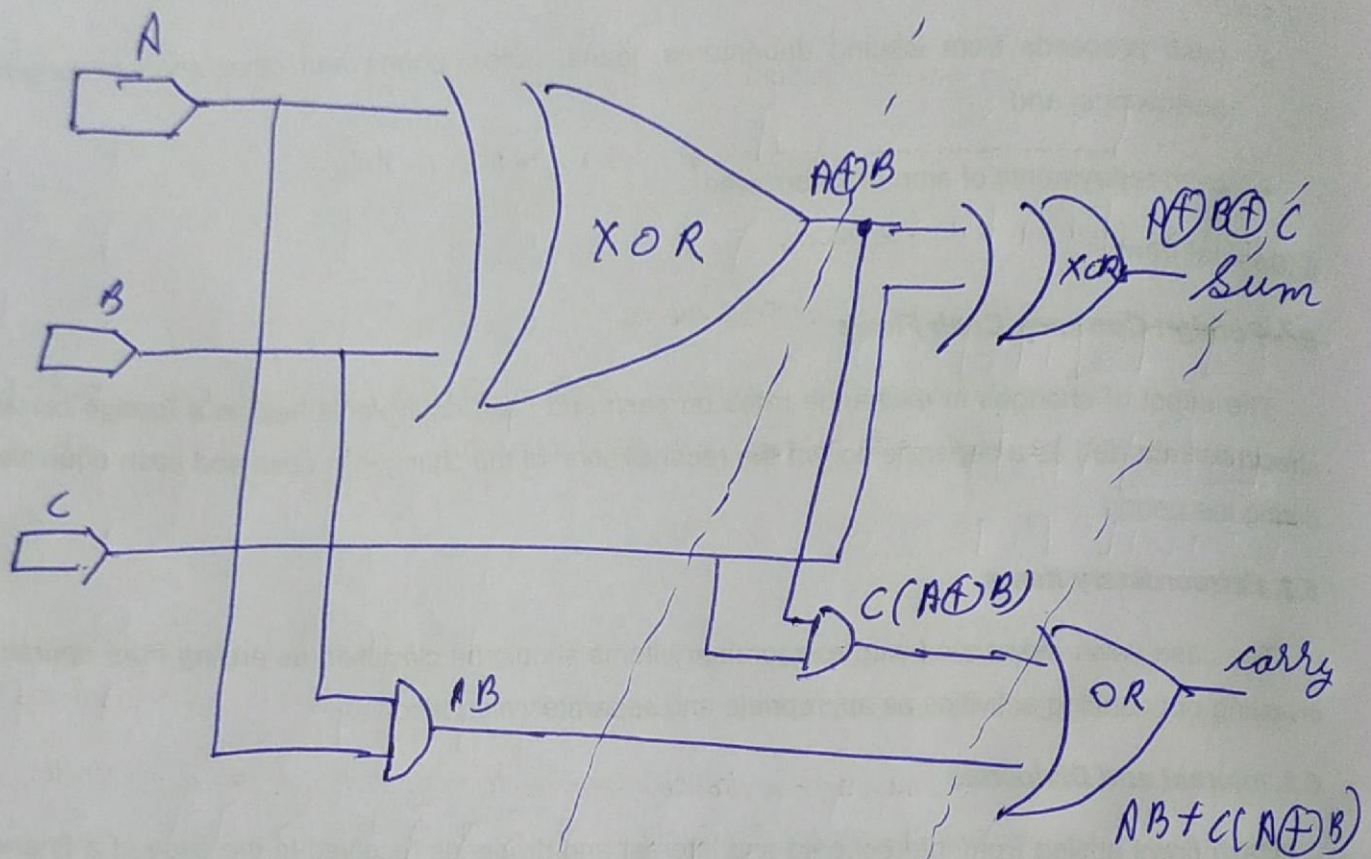
$$= A \oplus B \oplus C$$

$$\text{carry} \rightarrow \bar{A}B\bar{C} + \underline{A\bar{B}C} + \underline{AB\bar{C}} + ABC$$

$$= C(A \oplus B) + AB$$

$$[\bar{C} + C = 1]$$

Logic diagram \rightarrow



Result & inferences \rightarrow A full adder comprises of two half adders. The result of first adder has a sum of $A \oplus B$ & AB which in turn, are present in full adder. This $A \oplus B$ is added again with C as half adder. so we get a full adder.

Simulation Diagram And Output :-

