Indian Institute of Technology, Kharagpur
Department of Computer Science and Engineering
Mid-Spring Semester Examination 2017-18

High Performance Computer Architecture (CS60003)

Time=2 Hours **Max Marks=60**

Important Instructions:

- **Answer all questions.**
- **No clarification to any of the questions shall be provided. In case you have any queries, you can make suitable assumptions, but please write down your assumptions clearly.**
- **All answers should be brief and concise. Lengthy and irrelevant answers will be penalized.**

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1. What is the asymptotic prediction accuracy of a two-bit bimodal branch predictor on an infinitely repeating pattern of branch outcomes: ...T T N T T T T N T T N T N T... (T=taken, N=not taken) for a certain program. Assume that the predictor is initialized to "strongly not taken" before the start of the program. **[3]**

2. What is the storage size required (in bits) for implementing a 128-entry (2,2) correlating predictor? Clearly show your workout. **[3]**

3. Consider a simple 5 stage MIPS processor. Assume that it uses a single data/instruction cache, and 30% of all instructions issued are of load/store type. The program being executed does not cause any data or control hazards. Determine the increase/decrease in memory bandwidth of the MIPS processor compared to a similar processor that does not use instruction pipelining. **[5]**

4. Consider the following code containing a loop that is to be run on a simple MIPS 5-stage pipeline. What will be the number of stall cycles that would be encountered on each iteration of the loop. Assuming that the processor supports delayed branch, write an appropriate statically scheduled code. What will be the number of stalls of your statically scheduled code? **[1+3+1]**

```
      ADDI  R1, R0, 100
L1:   ADD   R2, R2, 1
      ADD   R3, R3, R2
      ADDI  R1, R1, -4
      BNEZ  R1, L1
```

5. The performance of a certain multi-cycle non-pipelined processor is evaluated using a program that takes 100 seconds to execute. Of this time, 20% is used for ALU operations, 50% for memory access instructions, and 30% for other types of instructions. A designer is targeting to enhance the performance of the processor through two possible improvements: (i) make the ALU instructions run four times faster than before, (ii) make memory access instructions run two times faster than before.

   a) What would be the speedup, if the performance of the ALU unit alone is enhanced? **[1]**

b) What would be the speedup if the performance of the memory access unit alone is enhanced? **[1]**

c) What will the speedup be if both the proposed enhancements are incorporated? **[3]**

6. A simple MIPS processor has two branch delay slots. An optimizing compiler can fill the first slot 85% of the time and can fill the second slot 20% of the time. The compiler fills the second slot only after the first slot is filled. What is the percentage improvement in performance achieved by this optimizing compiler relative to a compiler that does not fill any of the branch delay slots? Assume that a branch occurs once every 7 instructions. **[5]**

7. Assume that a MIPS processor with a 5 stage instruction pipeline and a split cache is being used for executing a program. A static not-taken predictor is used in the pipeline. There is no forwarding hardware. Assume that the characteristics of the program being executed are as follows. What is the average CPI? **[5]**

- 10% of the instructions are load instructions, and 40% of loads are used by the immediate next instruction. No other instructions cause a data hazard.
- 20% of the instructions are branches. Of these 10% are unconditional branches. Of the conditional branches, 50% on the average turnout to be taken.

8. A program having a nested loop is being executed on a MIPS processor. The outer loop of the program executes thousands of iterations. The inner loop always executes for 10 iterations for every outer loop iteration. The inner loop of the program has three branches (b1, b2, and b3) that execute in sequence during every inner loop iteration. The outcome pattern for these three branches is as shown below.

	Outer loop Iteration m										Outer loop Iteration m+1								
Inner Loop Iteration:	1	2	3	4	5	6	7	8	9	10	1	2	3	4	5	6	7	8	...
b1:	N	N	N	N	T	N	T	T	T	T	N	N	N	N	T	N	T	T	...
b2:	N	T	T	T	N	T	N	N	N	N	N	T	T	T	N	T	N	N	...
b3:	T	T	T	T	T	T	T	T	T	N	T	T	T	T	T	T	T	T	...

What is the asymptotic prediction accuracy for each of the three predictors mentioned in the following table on these three branches? Assume that the single bit predictors have been initialized to **NT** and the 2-bit predictor has been initialized to "strongly not taken". To concisely present your answer, copy the following table to your answer book and fill in the blanks in the table. **[9]**

Note:

- A 1-entry BHT means that there is only 1 history remembered for the entire processor.
- A huge BHT means that each branch in this code has its history tracked separately.

Predictor	Accuracy on b1	Accuracy on b2	Accuracy on b3
1bit predictor with 1entry BHT			
1-bit predictor with huge BHT			
2-bit predictor with huge BHT			

9. Consider an 8-stage instruction pipeline. It consists of the stages: IF1, IF2, ID, EX1, EX2, M1, M2, WB. The branch addresses are resolved at the end of the ID stage and branch conditions are resolved at the end of the EX2 stage. A typical workload has 20% conditional branches with 75% of the conditional branches taken on the average. Assume that only control hazards cause pipeline stalls and the pipeline does not stall on account of any other issue.

a) What is the CPI if a statically "predict-not-taken" scheme is used? **[2]**

b) What is the CPI if a statically "predict-taken" scheme is used? Assume that no Branch Prediction Buffer/Table is used and that the target address can only be known at the end of the ID stage. **[3]**

c) If a branch target buffer is added so that the branch target address is predicted during the IF1 stage, what would be the CPI? Assume that the branch target buffer does not give any prediction 10% of the time, in which case, a "predict-not-taken" scheme is applied. For the 90% of the time where a prediction is given, the prediction is correct with a probability of 50%. Assume that when a branch condition is predicted correctly, the target address is also predicted correctly. **[5]**

10. Suppose a certain processor uses a 10-stage instruction pipeline with the following stages:

F1 – start the fetch, predict if the instruction is a branch, whether it is taken or not, and if taken, the target address.
F2 – complete the fetch
D1 – decode the instruction – know if it's a branch at the end of D1,
D2 – complete decode
RR – read the registers– branch target address available at the end of this stage
A1 – start ALU operation; resolve branch condition
A2 – complete ALU operation
M1 – start memory operation
M2 – complete memory operation
WB – write the result to registers

a) What is the penalty for a mispredicted branch? **[2]**

b) What is the penalty when a branch is correctly predicted as taken, but the branch target address is incorrectly predicted? **[2]**

c) Assume the following:

i. There are no stalls in this pipeline except for branch instructions.
ii. Branch instructions account for 25% of all instructions
iii. 20% of branch instructions are taken
iv. Branch outcome is correctly predicted 90% of the time
v. The target address for a taken branch is correctly predicted 80% of the time

What is the CPI for this machine? **[6]**

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