GD

INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR
Mid-Spring Semester 2016-17

High Performance Computer Architecture (CS60003)

Time=2 Hours **Max Marks=52**

Important Instructions:

- **Answer all questions.**
- **No clarification to any of the questions shall be provided. In case you have any queries, you can make suitable assumptions, but please write down your assumptions clearly.**
- All answers should be brief and concise. Lengthy and irrelevant answers will be penalized.

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1. Estimate the speedup that would be obtained by replacing a CPU having an average CPI (clock cycles per instruction) of 5 with another CPU having an average CPI of 3.5, with the clock period increased from 100ns to 120ns. **[2]**

2. There are two processors A and B and their clock frequencies are 2.5GHz and 2.0GHz respectively. The average CPIs of these two computers are 2.5 and 2 respectively Which computer has the higher MIPs rating? **[2]**

3. Three enhancements with the following speed-ups are proposed for a new version of a processor: Enhancement A: Speed-up = 10; Enhancement B: Speed-up = 4; Enhancement C: Speed-up = 2. Enhancement A is usable for the entire execution time of a program irrespective of the usage of enhancements B and C. However, the enhancements B and C are such that they are usable 20% of time each, but are usable only one at a time. Compute the speed up that would be achieved by the new processor. **[3]**

4. SPECINT2000 benchmark program suite is to be run on the basic MIPS 5-stage pipeline processor to determine its performance. An analysis of the SPECINT2000 benchmark program suite yielded the following distribution of instructions: 25% loads, 10% stores, 10% branches, 5% jumps, and 50% R-type instructions. A further analysis reveals 40% of the register updates as well as loads are used by the immediate next instruction, in the rest of the cases these are used by instructions that are next to next (follow after one instruction). 50% of all branch instructions are mispredicted. The pipeline uses a static branch not taken prediction approach. The pipeline uses full forwarding but has no other extra circuitry. What is the average CPI? **[3]**

5. In a simple MIPS 5 stage pipeline a static not taken predictor is used. In case of a misprediction, the instructions being speculatively executed are quashed. A program has 20% branches, out of which 60% are taken and 40% are not taken. Determine the speed up of the given processor over a simple MIPS 5 stage pipeline processor that uses instruction flushing whenever any branches are encountered? **[3]**

6. Consider an unpipelined processor that has 1-ns clock cycle. In this processor, ALU instructions take 4 cycles, branch instructions take 5 cycles, and memory instructions take 4 cycles to complete execution. Assume that the relative frequencies of these instructions in a program are 50%, 30%, and 15% respectively. Suppose clock skew and pipeline register set up time

together constitute an overhead of 0.15 ns. Ignoring various hazards, how much speed up can be expected from pipelining the processor? **[4]**

7. Consider the following code that is being executed on a simple 5 stage MIPS processor. Assume that the given code is the full program and is not a segment of a program. The processor has no forwarding or control circuits to handle hazards and these are required to be taken care appropriately by the compiler by suitably restructuring the code and adding NOOPs wherever required.
   a. For the following code, add only minimal number of NOOP instructions wherever required without any restructuring of the code, so that hazards do not arise. Write the number of clock cycles that your code execution would take. **[2]**
   b. Suitably restructure the code given below and also add NOOP instructions wherever required so that that hazards do not arise and the code would run in the minimal number of clock cycles. Write the number of clock cycles that your code would take to execute. **[3]**

```
        lw R1, 10000(R7)
        add R5, R6, R1
        beqz R1, label
        sub R8, R1, R3
label:  add R4, R8, R9
        and R2, R3, R5
        add R3,R2,R1
```

8. A processor with an 18 stages pipeline and cycle time of 1ns runs a certain program P having 1000 instructions. Branches comprise 20% of the instructions, and the pipeline implements the "branch not taken" approach for handling branches. Further assume that 40% of the branches are predicted correctly, and there is an average penalty of 3 cycles for each mispredicted branch. Additionally, 40% of the total number of instructions incur an average of 2 cycles stall each on account of data hazard. Compute the execution time of the program. **[5]**

9. A proposed hardware optimization for a given processor would eliminate 10% of instructions outright and decrease the CPI of the remaining instructions by 10%. Unfortunately, this optimization would also result in decreasing the clock rate by 14%. Is this optimization worth implementing? Show the details of your calculations. **[5]**

10. Assume the execution of the following a simple instruction sequence on a 5-stage MIPS processor:

```
lw $1,40($6)   ;1
add $6,$2,$2   ;2
sw $6,50($1)   ;3
```

   a. Indicate the dependences and their types. **[1]**
   b. Assume there exists no forwarding circuitry or hazard control circuitry in one version of this pipelined processor. Indicate the hazards and add NOOP instructions to eliminate them. [1]
   c. Assume that full forwarding circuitry is in place in a different version of the processor. Indicate the hazards and appropriately add NOOP instructions to the code to eliminate

those. **[1]**

d. Assume the following clock cycle times for the two different versions of the processor: 300ps without forwarding, 400ps with full forwarding. What would be the total execution time of the given instruction sequence without forwarding and with full forwarding? **[2]**

11. Suppose you are an engineer at LMG microsystems and you have designed a pipelined processor with cycle time of 10 ns. The processor exhibits an average CPI of 1.6 on SPECINT2000 program suite. In the SPECINT2000 program suite, 10% of the instructions are branches and the branch prediction scheme deployed in the processor is 90% accurate. Branch misprediction penalty is 2 cycles. You are considering a new processor design where you target to decrease the cycle time to 9 ns by increasing the depth of the pipeline. In this new design the cost of a misprediction will increase to 7 clock cycles but everything else will remain the same. Compute the average CPI on the new processor for the SPECINT2000 benchmark. Would the SPECINT2000 benchmark program suite run faster or slower on this new processor and by how much? Show the details of your workout. **[5]**

12. Assume that the following outcome is observed for a particular branch when it gets executed within a loop: T, T, T, NT, T, T, T, NT, T, T, T, NT, . . .

a) What is the percentage of misprediction for a "predicted-taken" predictor? **[1]**

b) What is the percentage of misprediction for a 2-bit predictor with initial value set to "strongly not taken"? **[4]**

c) Assume that in a typical execution, 80% of the instructions are branches that follow the outcome pattern given in this question. A "predicted-not-taken" predictor is being used in the processor. In order to optimize the program, you can either change the predictor to a 2-bit predictor or you can change the code and reduce the number of branch instructions by half. Compute the speedup for each alternative. Which optimization is the better choice? **[5]**

---The End---