Divya Mahajan

CONTACT INFORMATION

Georgia Institute of Technology
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OBJECTIVE

To grow as a leader in the computer industry.

EDUCATION

- **Doctorate of Philosophy in Computer Science.** *May 2019*
  Georgia Institute of Technology
  Advisor: Hadi Esmaeilzadeh
- **Master of Business Administration.** *May 2019*
  Georgia Institute of Technology
- **Master of Science in Electrical and Computer Engineering.** May 2014
  The University of Texas at Austin - GPA: 3.93/4.00
- **Bachelor of Technology in Electrical Engineering.** May 2012
  Indian Institute of Technology (IIT) Ropar - GPA: 9.18/10.00
  Ranked 1st, Awarded the President of India's Gold Medal

AWARDS & HONORS

- Scheller College of Business Dean Innovation Fellowship, Spring 2018
- National Center for Women & Information Technology (NCWIT) Collegiate Award, Summer 2017
- Distinguished Paper Award, 22nd IEEE Symposium on High Performance Computer Architecture 2016
- Qualcomm Innovation Fellowship Finalist, Spring 2016
- Grace Hopper Celebration Scholar, Fall 2015
- Awarded merit certificates in semesters I, III, IV, V for being in top 7% academically in IIT Ropar
- Secured third position in group dance event at the Cultural Festival of Thapar University, Spring 2010
- Ranked 3216 in the Joint Entrance Examination among 300,000 applicants, Summer 2008
- Represented IIT Ropar in Badminton and Athletics at the forty-fourth inter IIT sports meet, Fall 2008

PUBLICATIONS

- **Divya Mahajan**, Joon Kyung Kim, Jacob Sacks, Adel Ardalan, Arun Kumar, Hadi Esmaeilzadeh. In-RDBMS Hardware Acceleration of Advanced Analytics. PVLDB, 11(11):1317-1331, 2018.
- Jacob Sacks, **Divya Mahajan**, Behnam Khaleghi, R. Connor Lawson, Hadi Esmaeilzadeh, "RoboX: An End-to-End Solution to Accelerate Autonomous Control in Robotics", *International Symposium on Computer Architecture, June 2018.*
- Jongse Park, Hardik Sharma, **Divya Mahajan**, Joon Kyung Kim, Preston Olds, and Hadi Esmaeilzadeh., "Scale-out acceleration for machine learning", *Proceedings of International Symposium on Microarchitecture, October 2017.*
- Hardik Sharma, Jongse Park, **Divya Mahajan**, Emmanuel Amaro, Joon Kyung Kim, Chenkai Shao, Asit Mishra, Hadi Esmaeilzadeh., "From High-Level Deep Neural Models to FPGAs", *International Symposium on Microarchitecture, October 2016.*
- **Divya Mahajan**, Amir Yazdanbakhsh, Jongse Park, Bradley Thwaites, Hadi Esmailzadeh., "Towards Statistical Guarantees in Controlling Quality Tradeoffs in Approximate Acceleration", *International Symposium on Computer Architecture, June 2016.*
- Amir Yazdanbakhsh, **Divya Mahajan**, Pejman Lotfi-Kamran, and Hadi Esmaeilzadeh., "AxBench: A Multi-Platform Benchmark Suite for Approximate Computing", *IEEE Design and Test, Special issue on Computing in the Dark Silicon Era, May 2016.*
- Jongse Park, Emmanuel Amaro, **Divya Mahajan**, Bradley Thwaites, Hadi Esmailzadeh., "ApproxiGame: Towards Crowd-sourcing Quality Target Determination in Approximate Computing", *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), April 2016.*

- **Divya Mahajan**, Jongse Park, Emmanuel Amaro, Hardik Sharma, Amir Yazdanbakhsh, Joon Kim, Hadi Esmailzadeh., "TABLA: A Unified Template-based Framework for Accelerating Statistical Machine Learning", *High-Performance Computer Architecture, March 2016.* **Distinguished paper award.**
- **Divya Mahajan**, Kartik Ramkrishnan, Rudra Jariwala, Amir Yazdanbakhsh, Bradley Thwaites, Jongse Park, Anandhavel Nagendrakumar, Abbas Rahimi, Hadi Esmailzadeh and Kia Bazargan., "Axilog: Abstractions for Approximate Hardware Design and Reuse", *IEEE Micro Special Issue on Alternative Computing Designs & Technologies, October 2015.*
- **Divya Mahajan**, Amir Yazdanbakhsh, Jongse Park, Bradley Thwaites, Hadi Esmailzadeh., "Prediction-based quality control for approximate accelerators", *Workshop on Approximate Computing Across the System Stack (WACAS) co-located with ASPLOS 2015, March 2015.*
- Amir Yazdanbakhsh, **Divya Mahajan**, Bradley Thwaites, Jongse Park, Anandhavel Nagendrakumar, Sindhuja Sethuraman, Kartik Ramkrishnan, Nishanthi Ravindran, Rudra Jariwala, Abbas Rahimi, Hadi Esmailzadeh and Kia Bazargan., "Axilog: Language Support for Approximate Hardware Design", to appear in *Design Automation and Test in Europe (DATE), March 2015.*
- **Divya Mahajan**, Matheen Mussadiq, and Earl E. Swartzlander Jr., "Memristor Based Adders," in *Forty Eigth Asilomar Conference on Signals, Systems and Computers, November 2014.*

WORK EXPERIENCE

- **Research Intern.** Microsoft Research — May 2018–Aug. 2018
  Working on devising low-latency FPGA-based hardware accelerators for performing advanced analytics on semi-structured data.
- **Architecture Research Intern.** Nvidia — May 2017–Aug. 2017
  Created part of high-level user interface that can program specialized hardware design languages and increase the chips customer usability.
- **Research Intern.** Microsoft Research — May 2016–Jul. 2016
  Incorporated compression for better usage of memory for Deep Networks being accelerated by FPGAs.
- **Design Engineer.** Silicon Engineering Group, Apple Inc. — May 2015–Aug. 2015
  Contributed to the simulation framework and performance evaluation of the architecture.
- **Logic Design Engineer.** Silicon Engineering Group, Apple Inc. — May 2013–Aug. 2013
  Contributed to the design and implementation of architectural and design changes of the datapath contributing towards the area and power reduction.
- **Summer Intern.** Photonics Lab, Aston University — May 2011–Jul. 2011
  Devised and created a wireless demonstration unit for a low cost optical fiber grating based sensor system.

RESEARCH EXPERIENCE

- **Research Assistant.** *Alternative Computing Technologies(ACT) Lab* — Aug. 2014–date
  Georgia Institute of Technology
  Advisor: Hadi Esmaeilzadeh

  In-RDBMS Hardware Acceleration of Advanced Analytics. *This work devises a cohesive system that enables the use of FPGA accelerators for in-RDBMS execution of advanced analytics, while exposing a high-level programming interface from conventional languages (SQL and Python) to data scientists. [ARXIV 2018]*
  An End-to-End Solution to Accelerate Autonomous Control in Robotics. *In this work we provide an end-to-end solution for roboticists to express the physics and task of a robot in a high-level domain-specific language (DSL). This high-level specification is converted to a binary to program a novel hardware accelerator. [ISCA 2018]*
  Template-based framework for accelerating machine learning. *As a part of the broader template based acceleration effort in the group, I devised a comprehensive solution, from programming model down to circuits to automatically generate accelerators for machine learning. [HPCA 2016, MICRO 2016, MICRO 2017]*
  Controlling Quality Tradeoffs in Approximate Acceleration. *This work defines a co-designed hardware-software technique with components in both compiler and microarchitecture to identify whether each approximate accelerator invocation leads to an undesirable quality loss. The hardware mechanism performs this classification at runtime and exposes a knob to the software mechanism to control quality tradeoffs. [WACAS 2015, ISCA 2016, IEEE Design & Test 2016]*
  Towards Crowdsourcing Quality Target Determination in Approximate Computing. *This work provides a crowdsourcing solution that transforms the tradeoff between quality and energy-performance gains from approximation to the tradeoff between gains and user satisfaction. [ASPLOS 2016]*
  Approximate Hardware Design. *This work provides hardware design language extensions to enable annotations in Verilog code to allow approximation of the hardware design elements. [DATE 2015, IEEE Micro 2015]*

- **Research Assistant.** Jan. 2014–May 2014
  The University of Texas at Austin
  Advisor: Earl Swartzlander

  Memristor Based Adders. *The work provides effective modeling techniques to create arithmetic units with the emerging memristor technology. [ASILOMAR 2014]*

TEACHING EXPERIENCE

- **Teaching Assistant.** Led review sessions, held office hours, answered email/newsgroup queries, designed and graded student homework.
  - *CS 6290 and ECE 6100: Advanced Computer Architecture, Georgia Tech* *Spring 2015*
  - *ME140L: Mechatronics Laboratory, The University of Texas at Austin* *Spring 2014*
  - *EE438: Fundamentals of Electronic Circuits, The University of Texas at Austin* *Fall 2013*
  - *EE338: Analog Electronics, The University of Texas at Austin* *Spring 2013*

REFERENCES

- **Hadi Esmaeilzadeh.** Associate Professor, University of California, San Deigo hadi@eng.ucsd.edu
  +1 (206) 658-3952
- **Doug Burger.** Technical Fellow, Microsoft Research dburger@microsoft.com
  +1 (425) 538-1668
- **Arun Kumar.** Assistant Professor, University of California, San Deigo arunkk@eng.ucsd.edu
  +1 (614) 602-9734