Divya Mahajan **https://www.cc.gatech.edu/ dmahajan7/**

CONTACT INFORMATION

Georgia Institute of Technology
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EDUCATION

- **Doctor of Philosophy in Computer Science.** *May 2019*
  Georgia Institute of Technology
  Dissertation: Balancing Generality and Specialization for Machine Learning in the Post ISA Era
  Advisor: Hadi Esmaeilzadeh
- **Master of Business Administration.** *May 2019*
  Georgia Institute of Technology
- **Master of Science in Electrical and Computer Engineering.** May 2014
  The University of Texas at Austin
- **Bachelor of Technology in Electrical Engineering.** May 2012
  Indian Institute of Technology (IIT) Ropar
  President of India Gold Medalist
  Thesis: FPGA based Implementation of an ALU using Harvard Architecture
  Advisor: Jyotinder S. Sahambi

AWARDS & HONORS

- Dean's Innovation Fellowship, Scheller College of Business, 2018
- National Center for Women & Information Technology (NCWIT) Collegiate Award, 2017
- Distinguished Paper Award, 22nd IEEE Symposium on High Performance Computer Architecture, 2016
- Qualcomm Innovation Fellowship Finalist, 2016
- Grace Hopper Celebration Scholar, 2015
- Awarded merit certificates in semesters I, III, IV, V for being in top 7% academically in IIT Ropar
- Actively participated and won awards as a part of the group dance team at IIT Ropar
- Represented IIT Ropar in Badminton and Athletics at the forty-fourth inter IIT sports meet, 2008
- Ranked 3216 in the Joint Entrance Examination among 300,000 applicants, 2008

ARTIFACTS

- **TABLA.** http://act-lab.org/artifacts/tabla/
- **DNNWEAVER.** http://dnnweaver.org
- **Axilog.** http://act-lab.org/artifacts/axilog/

PUBLICATIONS

Conference Papers

1. **Divya Mahajan**, Joon Kyung Kim, Jacob Sacks, Adel Ardalan, Arun Kumar, Hadi Esmaeilzadeh. In-RDBMS Hardware Acceleration of Advanced Analytics. *Proceedings of the Very Large Databases (VLDB) Endowment*, August 2018.
2. Jacob Sacks, **Divya Mahajan**, Behnam Khaleghi, R. Connor Lawson, Hadi Esmaeilzadeh, "RoboX: An End-to-End Solution to Accelerate Autonomous Control in Robotics", *International Symposium on Computer Architecture (ISCA), June 2018.*
3. Jongse Park, Hardik Sharma, **Divya Mahajan**, Joon Kyung Kim, Preston Olds, and Hadi Esmaeilzadeh., "Scale-out acceleration for machine learning", *Proceedings of International Symposium on Microarchitecture (MICRO), October 2017.*
4. Hardik Sharma, Jongse Park, **Divya Mahajan**, Emmanuel Amaro, Joon Kyung Kim, Chenkai Shao, Asit Mishra, Hadi Esmaeilzadeh., "From High-Level Deep Neural Models to FPGAs", *International Symposium on Microarchitecture (MICRO), October 2016.*
5. **Divya Mahajan**, Amir Yazdanbakhsh, Jongse Park, Bradley Thwaites, Hadi Esmailzadeh., "Towards Statistical Guarantees in Controlling Quality Tradeoffs in Approximate Acceleration", *International Symposium on Computer Architecture (ISCA), June 2016.*

6. Jongse Park, Emmanuel Amaro, **Divya Mahajan**, Bradley Thwaites, Hadi Esmailzadeh., "ApproxiGame: Towards Crowd-sourcing Quality Target Determination in Approximate Computing", *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), April 2016.*
7. **Divya Mahajan**, Jongse Park, Emmanuel Amaro, Hardik Sharma, Amir Yazdanbakhsh, Joon Kim, Hadi Esmailzadeh., "TABLA: A Unified Template-based Framework for Accelerating Statistical Machine Learning", *High-Performance Computer Architecture (HPCA), March 2016.* **Distinguished paper award.**
8. Amir Yazdanbakhsh, **Divya Mahajan**, Bradley Thwaites, Jongse Park, Anandhavel Nagendrakumar, Sindhuja Sethuraman, Kartik Ramkrishnan, Nishanthi Ravindran, Rudra Jariwala, Abbas Rahimi, Hadi Esmailzadeh and Kia Bazargan., "Axilog: Language Support for Approximate Hardware Design", to appear in *Design Automation and Test in Europe (DATE), March 2015.*
9. **Divya Mahajan**, Matheen Mussadiq, and Earl E. Swartzlander Jr., "Memristor Based Adders," in *Forty Eigth Asilomar Conference on Signals, Systems and Computers, November 2014.*

Journal Papers

1. Amir Yazdanbakhsh, **Divya Mahajan**, Pejman Lotfi-Kamran, and Hadi Esmaeilzadeh., "AxBench: A Multi-Platform Benchmark Suite for Approximate Computing", *IEEE Design and Test, Special issue on Computing in the Dark Silicon Era, May 2016.*
2. **Divya Mahajan**, Kartik Ramkrishnan, Rudra Jariwala, Amir Yazdanbakhsh, Bradley Thwaites, Jongse Park, Anandhavel Nagendrakumar, Abbas Rahimi, Hadi Esmailzadeh and Kia Bazargan., "Axilog: Abstractions for Approximate Hardware Design and Reuse", *IEEE Micro Special Issue on Alternative Computing Designs & Technologies, October 2015.*

Workshop Papers

1. **Divya Mahajan**, Amir Yazdanbakhsh, Jongse Park, Bradley Thwaites, Hadi Esmailzadeh., "Prediction-based quality control for approximate accelerators", *Workshop on Approximate Computing Across the System Stack (WACAS) co-located with ASPLOS 2015, March 2015.*
2. **Divya Mahajan**, Amir Yazdanbakhsh, Jongse Park, Bradley Thwaites, Hadi Esmailzadeh., "MITHRA: Controlling Quality Tradeoffs in Approximate Acceleration", *Techcon by Silicon Research Corporation, September 2015.*

PATENTS

1. Hadi Esmaeilzadeh, **Divya Mahajan**, Jongse Park, Hardik Sharma "Hardware Integrator for Relational Database Management Systems and Machine Learning Accelerators," Pending.
2. Hadi Esmaeilzadeh, **Divya Mahajan**, Jongse Park, Hardik Sharma "Template-Based Architecture for Automated FPGA Synthesis," Pending.
3. Hadi Esmaeilzadeh, Joon Kyung Kim, **Divya Mahajan**, "Domain Specific Language for Accelerating in-Database Advanced Analytics," Pending.

TALKS

- **Balancing Generality and Specialization for Machine Learning in the Post ISA Era**, Microsoft Research India, January 2019
- **Balancing Generality and Specialization for Machine Learning in the Post ISA Era**, IBM Research Workshop on Architectures for Secure, Cognitive, and Datacenter Computing, November 2018
- **Balancing Generality and Specialization for Machine Learning in the Post ISA Era**, Amazon Web Services, Palo Alto, October 2018
- **In-RDBMS Hardware Acceleration of Advanced Analytics**, VLDB, August 2018
- **Towards Statistical Guarantees in Controlling Quality Tradeoffs in Approximate Acceleration**, ISCA, June 2016
- **TABLA: A Unified Template-based Framework for Accelerating Statistical Machine Learning**, HPCA, March 2016

- **Prediction-based quality control for approximate accelerators**, Techcon by Silicon Research Corporation, September 2015

RESEARCH EXPERIENCE

- **In-RDBMS Hardware Acceleration of Advanced Analytics** Jun. 2017–Aug. 2018
  Alternative Computing Technologies(ACT) Lab
  Advisor: Dr. Hadi Esmaeilzadeh and Dr. Arun Kumar

  This work devises a cohesive system that enables the use of hardware accelerators for in-RDBMS execution of advanced analytics, while exposing a high-level programming interface from conventional languages (SQL and Python) to data scientists. This work takes a first step towards understanding the horizontal pipeline of systematic data processing and devises a vertical full-stack solution, from programming languages to template-based hardware, by addressing the challenges observed in executing advanced analytics within an RDBMS setting. [VLDB 2018, ARXIV 2018]

- **An End-to-End Solution to Accelerate Autonomous Control in Robotics** Jun. 2017–Jun. 2018
  Alternative Computing Technologies(ACT) Lab
  Advisor: Dr. Hadi Esmaeilzadeh

  In this work we provide an end-to-end solution for roboticists to express the physics and task of a robot in a high-level domain-specific language (DSL). This high-level specification is converted to a binary, by a specialized stack, to program our novel hardware accelerator. [ISCA 2018]

- **Template-based Framework for Accelerating Machine Learning** Jan. 2015–Mar. 2017
  Alternative Computing Technologies(ACT) Lab
  Advisor: Dr. Hadi Esmaeilzadeh

  As a part of the broader template based acceleration effort in the group, we devised a comprehensive solution, from programming model down to circuits, to automatically generate accelerators for machine learning. This effort also bridges the gap between distributed systems and accelerators by developing a specialized full stack for scale-out acceleration of machine learning. The goal is to devise a unified framework for FPGA acceleration of a wide range of machine learning algorithms without engaging the programmers in the arduous task of hardware design. [HPCA 2016, MICRO 2016, MICRO 2017]

- **Controlling Quality Tradeoffs in Approximate Acceleration** Aug. 2014–Nov. 2015
  Alternative Computing Technologies(ACT) Lab
  Advisor: Hadi Esmaeilzadeh

  This work defines a co-designed hardware-software technique with components in both compiler and microarchitecture to identify whether each approximate accelerator invocation leads to an undesirable quality loss. The hardware mechanism performs this classification at runtime and exposes a knob to the software mechanism to provide statistical guarantees that quality will be met on unseen data. [WACAS 2015, ISCA 2016, IEEE Design & Test 2016]

- **Crowdsourcing Quality Determination in Approximate Computing** Apr. 2015–Aug. 2015
  Alternative Computing Technologies(ACT) Lab
  Advisor: Hadi Esmaeilzadeh

  This work provides a crowdsourcing solution that transforms the tradeoff between quality and energy-performance gains from approximation, to the tradeoff between gains and user satisfaction. The solution effectively collects users' opinions to determine a level of quality loss that is acceptable for the majority. [ASPLOS 2016]

- **Approximate Hardware Design** Aug. 2014–Mar. 2015
  Alternative Computing Technologies(ACT) Lab
  Advisor: Hadi Esmaeilzadeh

  This work defines language extensions to Verilog code that provides syntax and semantics necessary for approximate hardware design and reuse. [DATE 2015, IEEE Micro 2015]

- **Memristor Based Adders** Jan. 2014–May 2014
  The University of Texas at Austin
  Advisor: Earl Swartzlander

The work provides effective modeling techniques to create arithmetic units with the emerging memristor technology. [ASILOMAR 2014]

INDUSTRY EXPERIENCE

- **Research Intern.** Microsoft Research May 2018–Aug. 2018
  Working on devising low-latency FPGA-based hardware accelerators for performing advanced analytics on semi-structured data.
- **Architecture Research Intern.** Nvidia May 2017–Aug. 2017
  Created part of high-level user interface that can program specialized hardware design languages to increase user productivity.
- **Research Intern.** Microsoft Research May 2016–Jul. 2016
  Incorporated compression for better usage of memory for Deep Networks being accelerated by FPGAs.
- **Design Engineer.** Silicon Engineering Group, Apple Inc. May 2015–Aug. 2015
  Contributed to the simulation framework and performance evaluation of the architecture.
- **Logic Design Engineer.** Silicon Engineering Group, Apple Inc. May 2013–Aug. 2013
  Contributed to the design and implementation of architectural and design changes of the datapath contributing towards the area and power reduction.
- **Summer Intern.** Photonics Lab, Aston University May 2011–Jul. 2011
  Devised and created a wireless demonstration unit for a low cost optical fiber grating based sensor system.

PROFESSIONAL ACTIVITIES

- Student Poster Session Chair for the 4th Career Workshop for Women and Minorities in Computer Architecture (CWWMCA) co-located with MICRO-51
- **Reviewer.**
  - ACM Transactions on Architecture and Code Optimization (TACO) 2018
  - IEEE Transactions on Computers 2018
  - IEEE Micro on Approximate Computing 2018
  - Design Automation for Embedded Systems (DAEM) 2017
  - ACM Transactions on Architecture and Code Optimization (TACO) 2017
  - IEEE Transactions on Circuits and Systems (TCAS) 2016
  - IEEE Conference on Decision and Control (CDC) 2016
  - IEEE Transactions on Emerging Topics in Computing (TETC) 2016
  - International Symposium on Performance Analysis of Systems and Software (ISPASS) 2016
- **Award Reviewer.**
  - Georgia Tech President's Undergraduate Research Award 2018
  - Georgia Tech President's Undergraduate Research Award 2017
- **Member.**ACM and IEEE

TEACHING EXPERIENCE

Teaching Assistant. Led review sessions, held office hours, answered email/newsgroup queries, designed and graded student homework.

- CS 7001: Graduate Studies Computing, Georgia Tech Fall 2018
- CS 6290 and ECE 6100: Advanced Computer Architecture, Georgia Tech Spring 2015
- ME140L: Mechatronics Laboratory, The University of Texas at Austin Spring 2014
- EE438: Fundamentals of Electronic Circuits, The University of Texas at Austin Fall 2013
- EE338: Analog Electronics, The University of Texas at Austin Spring 2013

STUDENTS MENTORED

- Joon Kyung Kim Dec. 2015 - Aug. 2018
  Worked closely with Joon to develop the compiler for TABLA *which enables automation to generate hardware accelerators for a wide range of machine learning algorithms. Actively advised him on benchmarking the in-database analytics algorithms on the CPU for the DAnA project.*

- Chenkai Shao — Jun. 2016 - May 2017
  Provided guidance on understanding the impact of quantization on the accuracy of various machine learning algorithms. We worked together to recognize the bit-widths suitable for various algorithms and their effect on the hardware accelerator design for TABLA.
- Ranjini Subramaniam — Jun. 2015 - Dec. 2015
  Provided directions for integrating hardware acceleration within the current software stack of data management systems as a part of the initial exploration of DAnA.
- Iswerya Prem, Nikhil Bharat, Sachin Shylaja — Jun. 2015 - Dec. 2015
  Worked closely with the students to understand the commonalities among a wide range of supervised machine learning algorithms, which eventually formed the basis of the template-based hardware architecture of TABLA.

REFERENCES

- **Hadi Esmaeilzadeh.** Associate Professor, University of California, San Diego — hadi@eng.ucsd.edu, +1 (206) 658-3952
- **Doug Burger.** Technical Fellow, Microsoft Corporation — dburger@microsoft.com, +1 (425) 538-1668
- **Vijay Janapa Reddi.** Associate Professor, Harvard University — vj@eecs.harvard.edu, +1 (408) 390-2790
- **Hyesoon Kim.** Associate Professor, Georgia Institute of Technology — hyesoon@cc.gatech.edu, +1 (404) 385-3303
- **Annie Anton.** Professor, Georgia Institute of Technology — aa16@gatech.edu, +1 (919) 418-9317
- **Arun Kumar.** Assistant Professor, University of California, San Diego — arunkk@eng.ucsd.edu, +1 (614) 602-9734