ELE 504 Lab Report 5

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Introduction

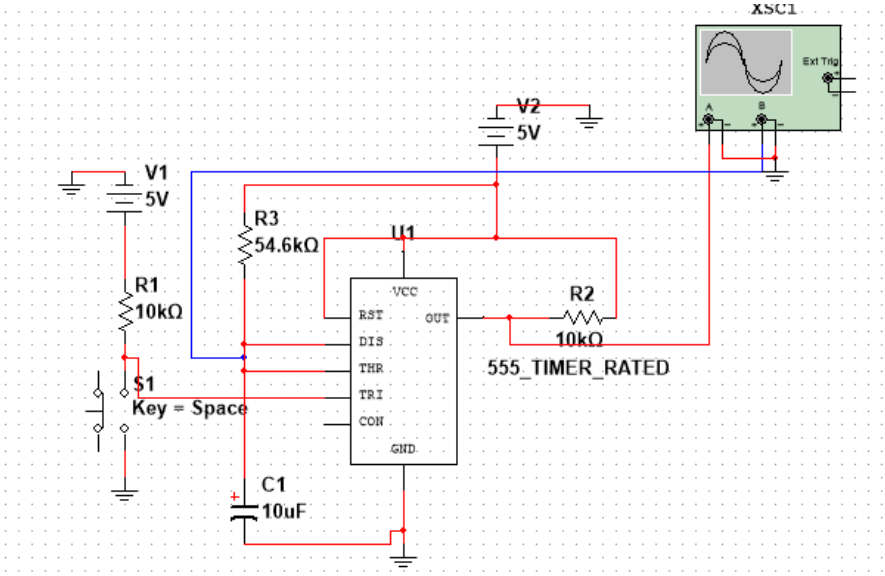
The 555 Timer is a commonly used tool used for many reasons such as clock generation and pulse generation. Pulse generation can be achieved by configuring it to “monostable mode” while an oscillating signal with an adjustable frequency can be achieved using the “astable mode.”This lab takes a look at both configurations of the 555 Timer as well as methods that can be used to achieve a 50% duty cycles in astable mode.

Objective

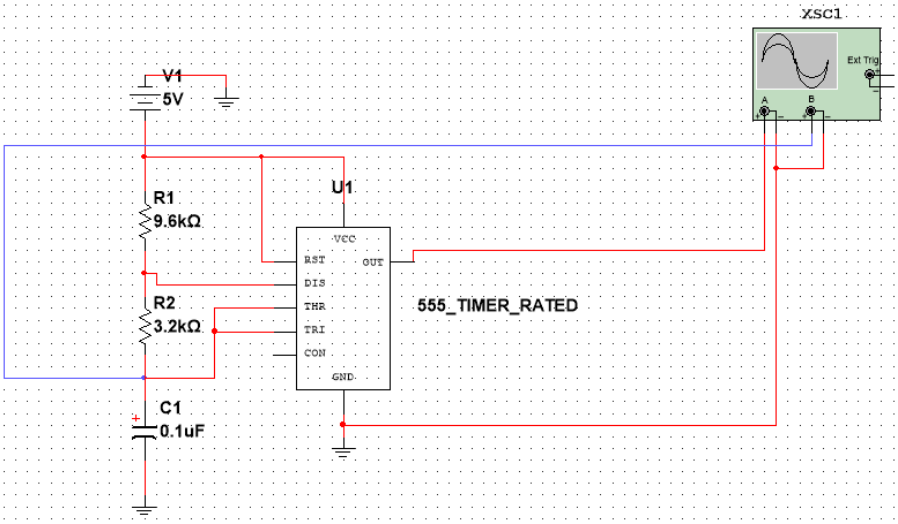
The objective of this project is to design, implement and test pulse and clock generated circuits using the 555 timer integrated circuit device in monostable and astable modes.

Circuit Screenshots

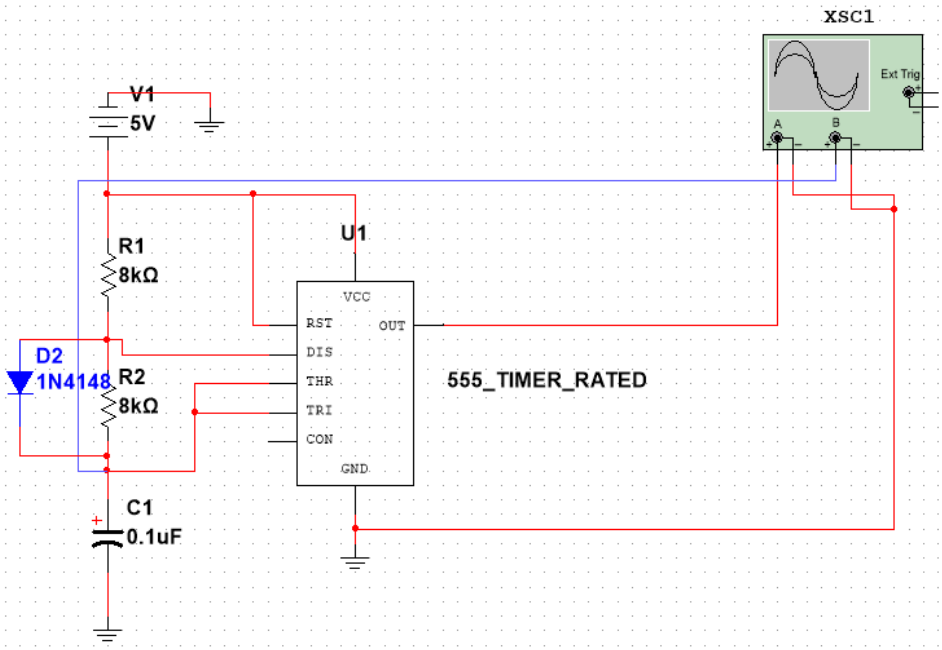
Circuit 1: Monostable Configuration



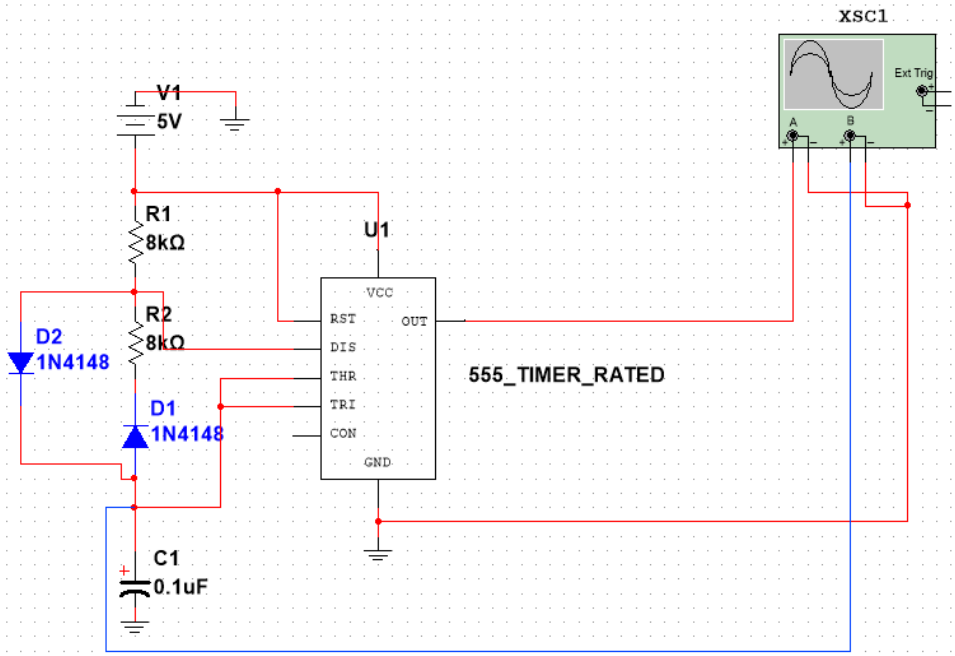
Circuit 2: Astable Configuration



Circuit 3: Astable Configuration with Diode



Circuit 4: Alternate Astable Configuration with two Diodes



Results and Tables

Figure 1: Monostable Mode Vc and Vo waveforms with 5V supply voltage

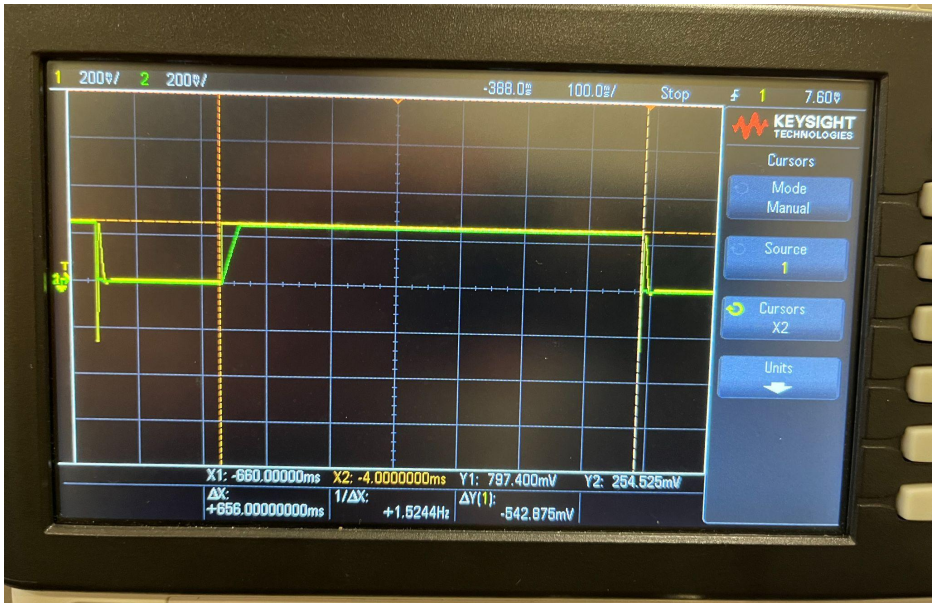


Figure 2: Astable Mode Vc and Vo waveforms with 5V supply voltage (showing period, T)

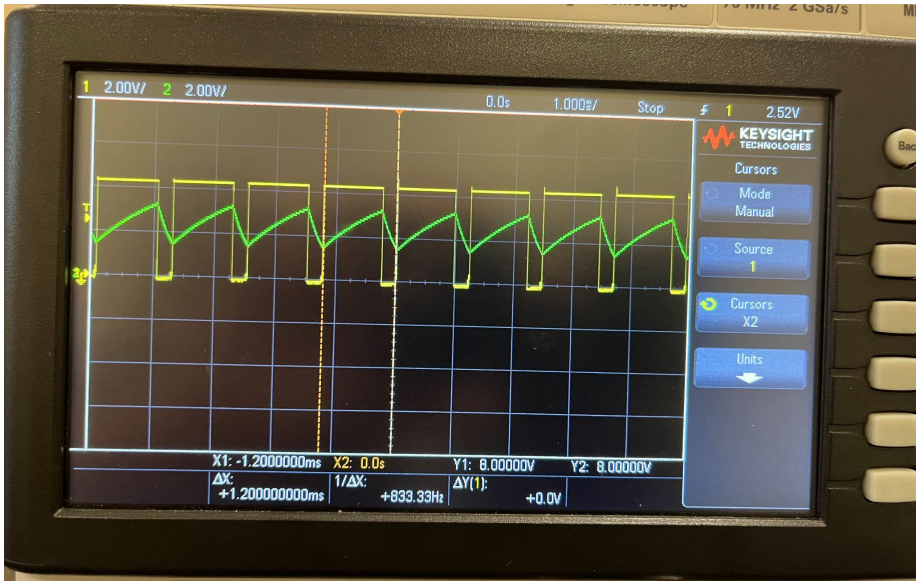


Figure 3: Astable Mode Vc and Vo waveforms with 5V supply voltage(showing period, Th)

Figure 4: Alternate Astable Mode with diode Vc and Vo waveforms

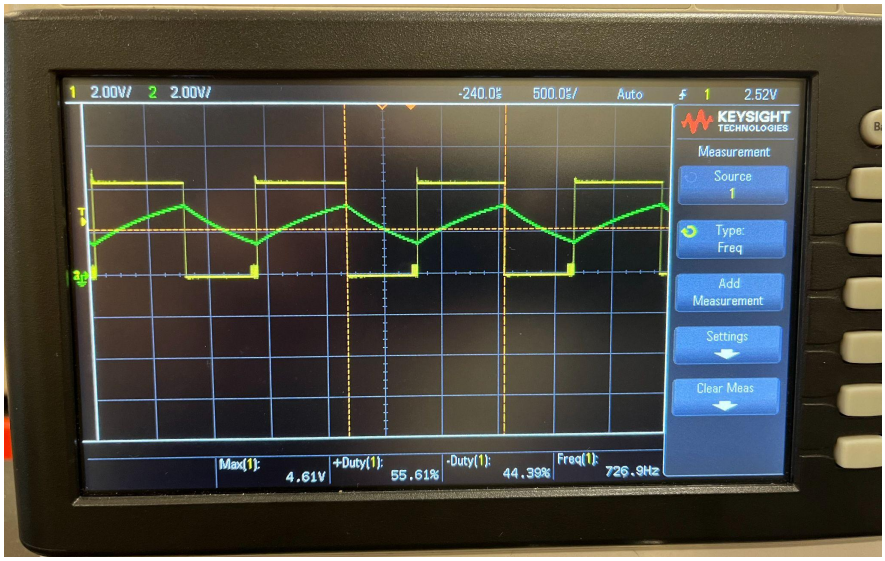
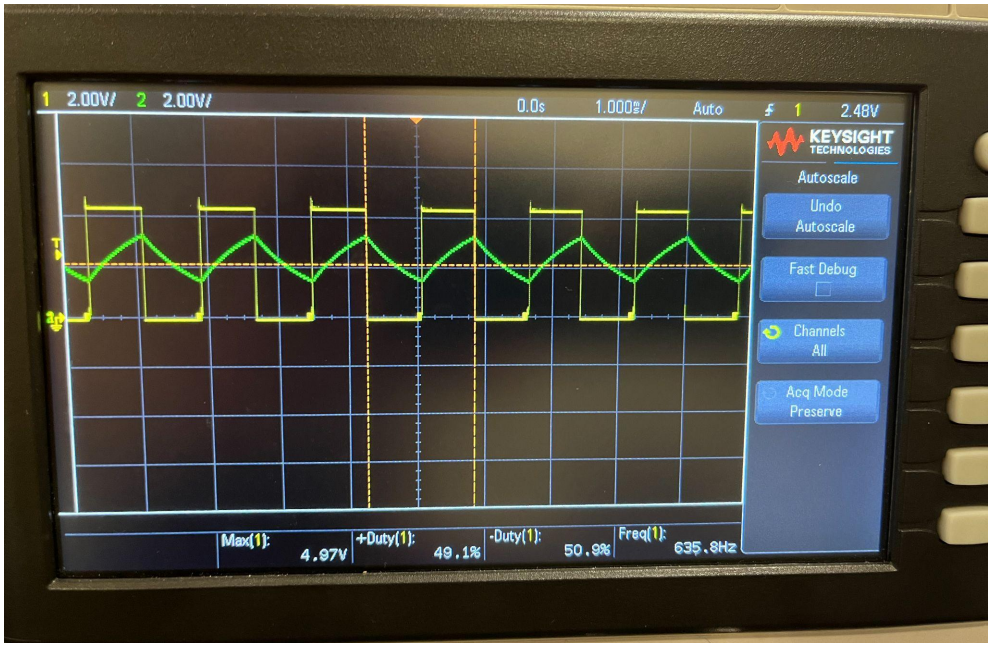


Figure 5: Alternate Astable Mode with two diodes Vc and Vo waveforms



Conclusion

After completion of the experiment, several conclusions can be drawn. Firstly, the 555 Timer was successful in generating a pulse in monostable mode with the correct time period. The desired period for **Circuit 1** was 600ms and 656ms was observed. Secondly, The astable mode circuit in **Circuit 2** was also able to generate a clock signal with a frequency of 833 Hz and with a duty cycle of 78%. This is in line with the prelab analysis where the expected clock frequency was 900 Hz and duty cycle was 80%. **Circuit 3** was also successful in producing the same results as the prelab where duty cycle was relatively close to 50%, as 55.61% was observed. Finally, **Circuit 4** was able to produce a duty cycle of 49.1% which was very close to 50% and more accurate than **Circuit 3**. This also agrees with the prelab analysis where the second diode was expected to minimize the effects that the first diode had on the duty cycle. Overall, all the circuits produced the desired results of the prelab, however there was a small discrepancy of around 100ms in the frequencies which was likely due to the fact that a 10k resistor was used instead of the 9.6k resistor in **Circuit 2**.