CDA 4253/EEL 4935 FPGA System Design

Assignment #5

Description

In this assignment, you will design a simple digital lock to provide an approach for identity authentication. This lock operates in three modes: *programming*, *normal* and *locked*. In the programming mode, a user programs the lock by inputting a sequence of three numbers which are stored in the circuit as the key. In the normal mode, the lock waits for a sequence of three numbers. If this sequence matches what is stored exactly, the lock generates a grant signal. If the number of failed authentication exceeds a threshold, the lock transitions to the locked mode, and it stops the authentication. The following list describes the design interface.

1. Use button `btnC` to reset the circuit.
2. Use button `btnU` to set the circuit into the normal mode.
3. Use button `btnD` to set the circuit into the programming mode.
4. Use `sw3 - sw0` to set a single digit BCD number. Use `btnL` to make the circuit read and store this number.
5. After a sequence of three numbers are read into the circuit, use button `btnR` to store the sequence as the key in the programming mode, or to compare the input sequence against what is stored in the circuit for authentication in the normal mode.
6. Every time a number is read into the circuit by pressing button `btnL`, this number is shown on the 7-segment display.
7. In the normal mode, once the input sequence is authenticated, `led15 - led0` all light up.
8. If authentication attempts fail 3 times consecutively, the circuit transitions to the locked mode. Once the circuit is in the locked state, all leds light off, and the 7-segment display shows `----`.

Upon power-up or reset, the circuit is in the programming mode. Pressing button `btnU` puts the circuit in the normal mode once the circuit is programmed. When the circuit is in the normal mode, pressing button `btnD` anytime puts the circuit back to the programming mode. When the circuit is in the locked mode, it stays in that mode permanently. Pressing button `btnC` has no effect in the locked mode.

Requirements

1. Draw a state diagram for the FSM describing the circuit operations. Your VHDL model should implement this FSM as discussed in class.
2. Draw a block diagram if your VHDL model instantiates components. The structure of your VHDL model must match the block diagram.
3. Implement the design on the Basys3 FPGA boards. For this implementation, you will need to use additional components such hex to 7-segment decoder/display multiplexer from Assignment 2, and the debouncing circuit block as shown in Chu's book.

Design that does not work correctly on Basys3 FPGA boards will get no more than 80/100 points.

Submission

1. Create a folder `hw5-your-name` for this assignment, which holds design project files.
2. Create a README file to explain your work if necessary.
3. To submit, zip the entire folder `hw5-your-name`, and upload `hw5-your-name.zip` file to Canvas.

   Note: Make sure that your zipped file is in the ZIP format to avoid any potential issues in opening your files.

   Note: Make sure that you copy all necessary files into the projects.
4. *Make sure that you do NOT modify your work before the HW grading is finished in case that your original work needs to be examined.*