

MAHBOD AFARIN

Rooms 2132, CSE Department, UC San Diego, CA

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Professional Summary

Postdoctoral Scholar at UC San Diego with over 5 years of experience in hardware accelerators, compiler design, and graph analytics, working across architecture, runtime, and MLIR-based compiler stacks. Demonstrated ability to deliver high-impact research results, with successful technology deployment at Google and publications in top-tier conferences.

Technical Skills

Languages: C/C++, Python, CUDA, OpenMP, OpenCL, SQL

Compiler Design: LLVM, MLIR, LLVM-BOLT, LLVM Machine Outliner

Hardware Design: VHDL, Verilog HDL, SystemC, Xilinx ISE, Altera Quartus, Synopsys Design Compiler

Simulation & Modeling: Multi2Sim, GPGPU-Sim, Mentor Graphics Modelsim, HSPICE, PSPICE, IC Encounter, HSIM, Cadence SoC Encounter, Structural Simulation Toolkit

Education

University of California Riverside

Doctor of Philosophy (Ph.D.) in Computer Science

Jan. 2020 – June 2025

Riverside, California

- Thesis: "*Redundancy Removal for Accelerating Graph Processing Workloads*"

- Advisors: Professor *Rajiv Gupta* & Professor *Nael Abu-Ghazaleh*

- GPA: **3.86/4**

Sharif University of Technology

Master of Science (M.Sc.) in Computer Engineering

Sep. 2015 – Jan. 2018

Tehran, Iran

- Thesis: "*Improving Life Cycle of SIMT Processors for Approximate Computing*" (Thesis Grade: **Excellent**)

- Advisors: Professor *Shaahin Hessabi*

- GPA: **4/4 (19.03/20)** (**ranked 7th among 83 computer engineering students**)

Research Experience

University of California San Diego

Postdoctoral Scholar

Jun. 2025 – Present

San Diego, California

- Member of the *System Energy Efficiency (SEE) Lab* and the *Processing with Intelligence Storage & Memory (PRISM)* Research Center at UC San Diego, under the supervision of Professor *Tajana Rosing*.
- Developing MLIR-based compiler support targeting *Dynamic Programming Processing in Memory Hardware Accelerators*.

Google

Student Researcher

Sep. 2024 – Dec. 2024

Sunnyvale, California

- Member of the *Compiler Optimization* team at **Google** working on *Inter-procedural Identical Basic Block Folding*.
- Developed scalable post-link and inter-procedural identical basic block folding techniques to eliminate redundant basic blocks, reduce binary code size, and maintain performance using profiling-guided analysis.

University of California Riverside

Graduate Research Assistant

Jan. 2020 – Jun. 2025

Riverside, California

- Member of the *Graph Analytics with Scalability and Performance (GRASP)* and the *RIverside Programming Language & Software Engineering (RIPPLE)* centers, supervised by Professor *Rajiv Gupta* & Professor *Nael Abu-Ghazaleh*.
- Developed HW/SW approaches to accelerate dynamic graph workloads, along with designing hardware accelerators.

Sharif University of Technology

Graduate Research Assistant

Dec. 2015 – Jan 2018

Tehran, Iran

- Member of the Very Large Scale Integration Laboratory (VLSI-Lab), supervised by Professor *Shaahin Hessabi*.

- Improved SIMD processor life cycle for approximate computing through techniques that extend hardware longevity.

Publications

[**EuroSys'24**] X. Jiang, **M. Afarin**, Z. Zhao, N. Abu-Ghazaleh, R. Gupta, “Core Graph: Exploiting Edge Centrality to Speedup the Evaluation of Iterative Graph Queries,” 2024 Proceedings of the Nineteen European Conference on Computer Systems (*Acceptance Rate: 15.99%*) (Contributed Equally with the First Author).

[**MICRO'23**] C. Gao, **M. Afarin**, S. Rahman, N. Abu-Ghazaleh, R. Gupta, “MEGA Evolving Graph Accelerator,” 2023 56th Annual IEEE/ACM International Symposium on Microarchitecture (*Acceptance Rate: 22%*) (Contributed Equally with the First Author).

[**ASPLOS'23**] **M. Afarin**, C. Gao, S. Rahman, N. Abu-Ghazaleh, R. Gupta, “CommonGraph: Graph Analytics on Evolving Data,” International Conference on Architectural Support for Programming Languages and Operating Systems. (*Acceptance Rate: 26.66%*)

[**MICRO'21**] S. Rahman, **M. Afarin**, N. Abu-Ghazaleh, R. Gupta, “JetStream: Graph Analytics on Streaming Data with Event-Driven Hardware Accelerator,” 2021 54th Annual IEEE/ACM International Symposium on Microarchitecture. (*Acceptance Rate: 21.74%*)

[**HOPC'23**] **M. Afarin** et al., “CommonGraph: Graph Analytics on Evolving Data (Abstract),” In Proceedings of the 2023 ACM Workshop on Highlights of Parallel Computing.

[**BigData'23**] A. Mazloumi, **M. Afarin**, R. Gupta, “Expressway: Prioritizing Edges for Distributed Evaluation of Graph Queries,” 2023 IEEE International Conference on Big Data.

[**Under Review**] C. Mamatha, **M. Afarin**, R. Gupta, S. Tallam, H. Shen, and X. D. Li., “DeduBB: Binary Code Size Reduction via Post-Link Basic Block De-duplication,” ACM SIGPLAN 2026 International Conference on Compiler Construction.

[**Under Review**] **M. Afarin** et al., “UVVs: Identifying Unchanged Vertex Values in Evolving Graphs via Intersection-Union Analysis,” 40th IEEE International Parallel & Distributed Processing Symposium (IPDPS 2026).

[**Under Review**] C. Gao, **M. Afarin**, X. Yin, N. Abu-Ghazaleh, R. Gupta, “Sagas: Temporally Consistent Sampling of Evolving Graphs,” IEEE International Conference on Big Data.

[**Under Review**] C. Gao, X. Yin, **M. Afarin**, N. Abu-Ghazaleh, R. Gupta, “Indexing Evolving Graphs via Query Evolution Prediction,” ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP 2026).

Awards & Achievements

- Won **UCR Dissertation Completion Fellowship Award** at UC Riverside, 2024.
- Received the **Excellent Service** badge in all three cycles of ASPLOS'24 Artifact Evaluation, 2024 ([Certificate](#)).
- Won **UCR GSA Travel Grant Award** at University of California, Riverside, 2023.
- Won **Dean's Distinguished Fellowship Award** at University of California, Riverside, 2019.
- **Ranked 7th** among 83 Computer Engineering students at Sharif University of Technology (**Top 8%**), 2018.
- Admitted as an **Exceptional Talent** at Sharif University of Technology for M.Sc, 2015.
- **1st Rank**, highest B.Sc GPA among all Computer Engineering graduates at Shahed University, 2015.

Teaching Experience

- Teaching Assistant, **Compiler Design** (Summer'21/22/23 and Spring'21/22), University of California, Riverside, Department of Computer Science & Engineering, Prof. Rajiv Gupta.
- Teaching Assistant, **System on Chip** (Spring'18) **Testability** (Fall'17) **Advanced VLSI** (Spring'17) **VLSI** (Fall'16), Sharif University of Technology, CE Dep., Prof. Shaahin Hessabi.
- Lab Instructor, **Logic Design Lab**, Sharif University of Technology, Department of Computer Engineering, Summer 2017.
- Lab Instructor, **Digital System Design Lab**, Sharif University of Technology, Department of Computer Engineering, Summer 2016, Prof. Maziar Goudarzi.

Professional Services

Audio/Video Chair: ASPLOS'24 Conference

Reviewer: CAL'23, TACO'23, IEEE Transaction on Computers'23, Parallel Computing'23 & 25

Talks: HOPC'23, Society of Women Engineers (UCR, Winter'24), Tulane Uni. (Winter'25), & Binghamton Uni. (Spring'25)

Artifact Evaluation Committee: ASPLOS'25, ASPLOS'24, ISCA'24

References

Professor Tajana Rosing, My Postdoc Supervisor – ([Email](#) | [Homepage](#))

Professor Rajiv Gupta, My Ph.D. Supervisor – ([Email](#) | [Homepage](#))

Professor Nael Abu-Ghazaleh, My Ph.D. Supervisor – ([Email](#) | [Homepage](#))