There is a source file which name is **main.py**
This source code is responsible for generating below files from a
template file:
    -constraints.tcl
    -NoC_hw.tcl
    -qsys_system.tcl
    -synth_qsys.tcl
    -NOC.vhd
    -wrapper.v
template files are located in **Templates** folder, and we use the **quik
engine** for generating these files.
The first four files are writed into **hw_scripts** Folder, and the other
ones are writed into **hw_sources** Folder.

The description of every generated-file:

-Constraints.tcl:
    In this file, specifications which going to generate are listed
    below:
    -DEVICE_FAMILY
    -DEVICE
    the rest of the file would be unchanged.

-NoC_hw.tcl
    In this file, specifications which going to be generated are
    listed below:
    -RowNo
    -ColNo
    -PackWidth
    -DataWidth
    -AddrWidth
    -RoChAddr
    -PhyChAddr
    -ViChAddr
    -PhyRoChAddr
    -RoCh
    -PhyCh
    -ViCh
    -PhyRoCh
    Also this file generates **two avalon streaming interface** as same
    number as **tile number**

-qsys_system.tcl
    In this file, specifications which going to be generated are
    listed below:
    -DEVICE_FAMILY
    -DEVICE
    Also this file instantiate:
        -one **NoC IP**
        -one **clock interface**
        -onchip memory as same number as **processor number**
            • the **size of memories** are variable

> > **-altera avalon fifo** as **fifo sink** for each tile
> > > • the **depth of fifos** are variable
> > **-altera avalon fifo** as **fifo source** for each tile
> > > • the **depth of fifos** are variable
> > -**altera avalon jtag uart**
> > **-altera nios2** for each processor
> > > • the **version of nios2** is variable (**economical or fast**)
> Next step is to generate the connection of these IPs to each other

-synth_qsys.tcl
> In this file, specifications which going to generate are listed below:
> **-DEVICE_FAMILY**
> **-DEVICE**

-NOC.vhd
> In this file, specifications which going to be generated are listed below:
> -**RowNo**
> **-ColNo**
> **-PackWidth**
> **-DataWidth**
> **-AddrWidth**
> **-RoChAddr**
> **-PhyChAddr**
> **-ViChAddr**
> **-PhyRoChAddr**
> **-RoCh**
> **-PhyCh**
> **-ViCh**
> **-PhyRoCh**
> Also this file generates inputs and outputs for each **node** and connects them in a right way

-wrapper.v
> this file generates inputs and outputs of **NOC** and connects them in a right way