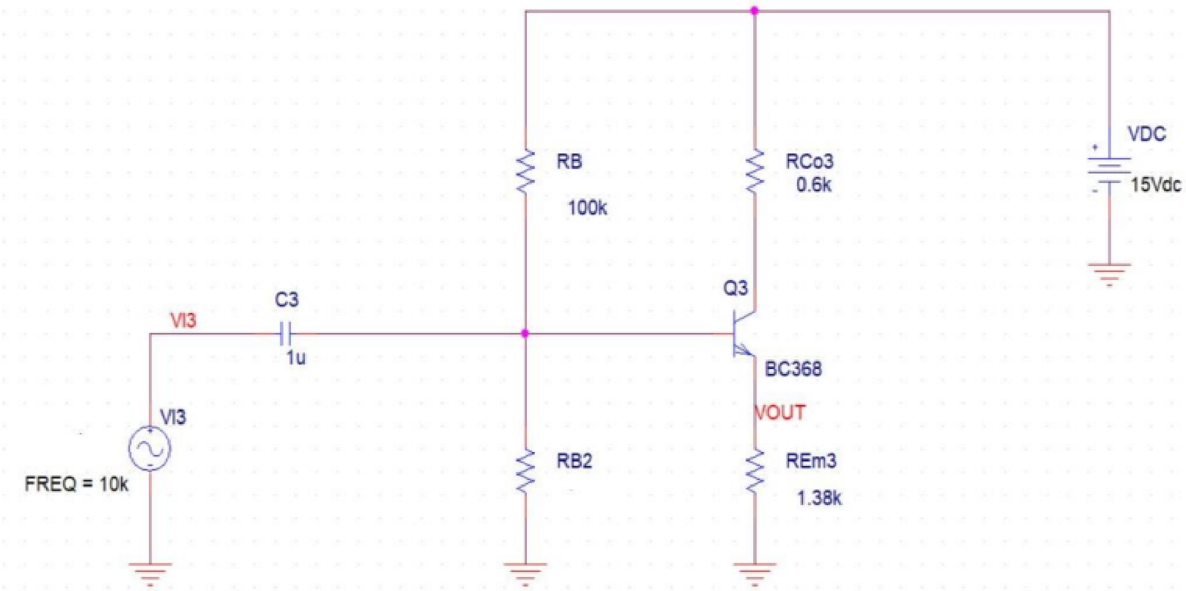
Design and Simulation of a 3-Stage BJT Amplifier using PSpice

Section 1: Designing the 3rd Stage

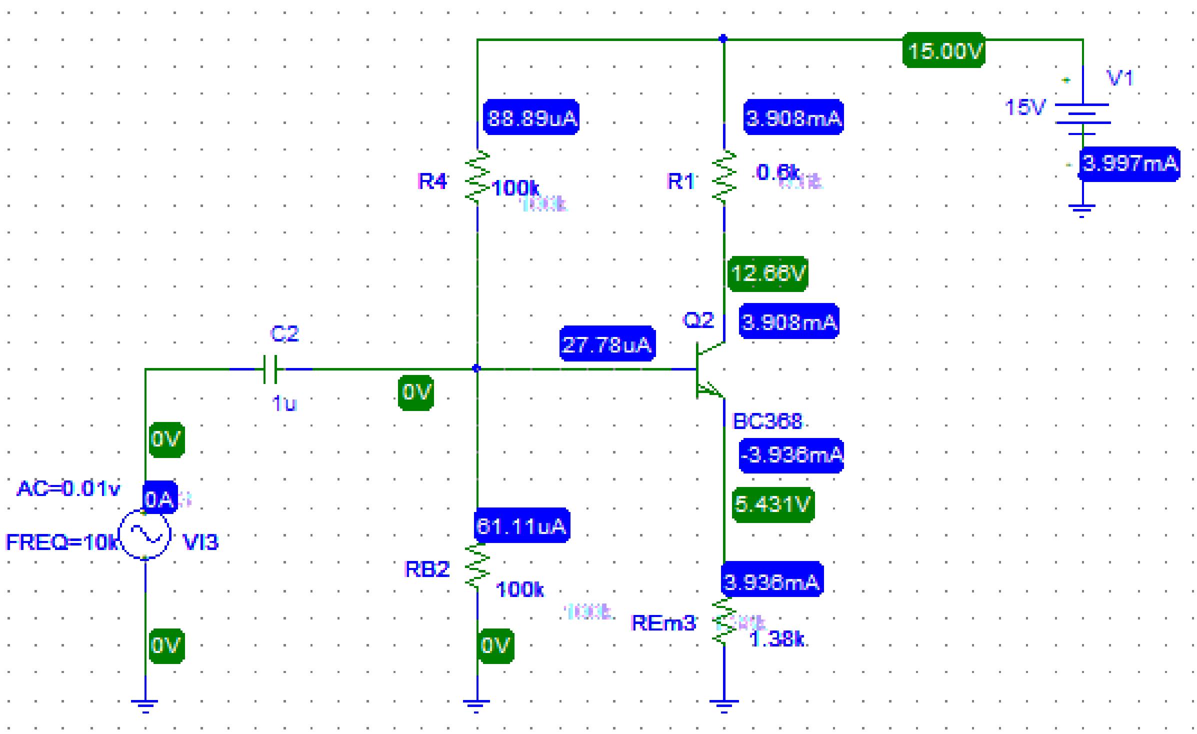


Start with this circuit.

Choose a Desired value for RB2.

Simulate the circuit in PSPICE and obtain the values of I_b, I_c, then calculate the value of β based on them.

Simulation Results:



$RB2$ was chosen to be $100k$.

Based on the simulation results V_{CE} can be calculated as follows:

$V_{CE} = 12.66v - 5.431v = 7.229v$

Because $V_{CE} > V_{CE,sat}$, It can be inferred that the transistor is operating in the active region.

Exercise 1.1) Find the value of β

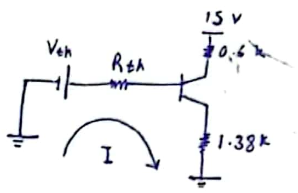
$\beta = \frac{I_c}{I_b} = \frac{3.908mA}{27.78\mu A} = 140.7$

Exercise 1.2) Find the value of $V_{BE_{ON}}$

KVL : $V_{BE} = 6.111v - 5.431v = 0.68v$

Exercise 1.3) Choose the value of R_{B2} such that $I_C = 5mA$.

Theoretical Calculations:



$$V_{th} = \frac{15 R_{B2}}{100 + R_{B2}}$$

$$R_{th} = 100 \| R_{B2}$$

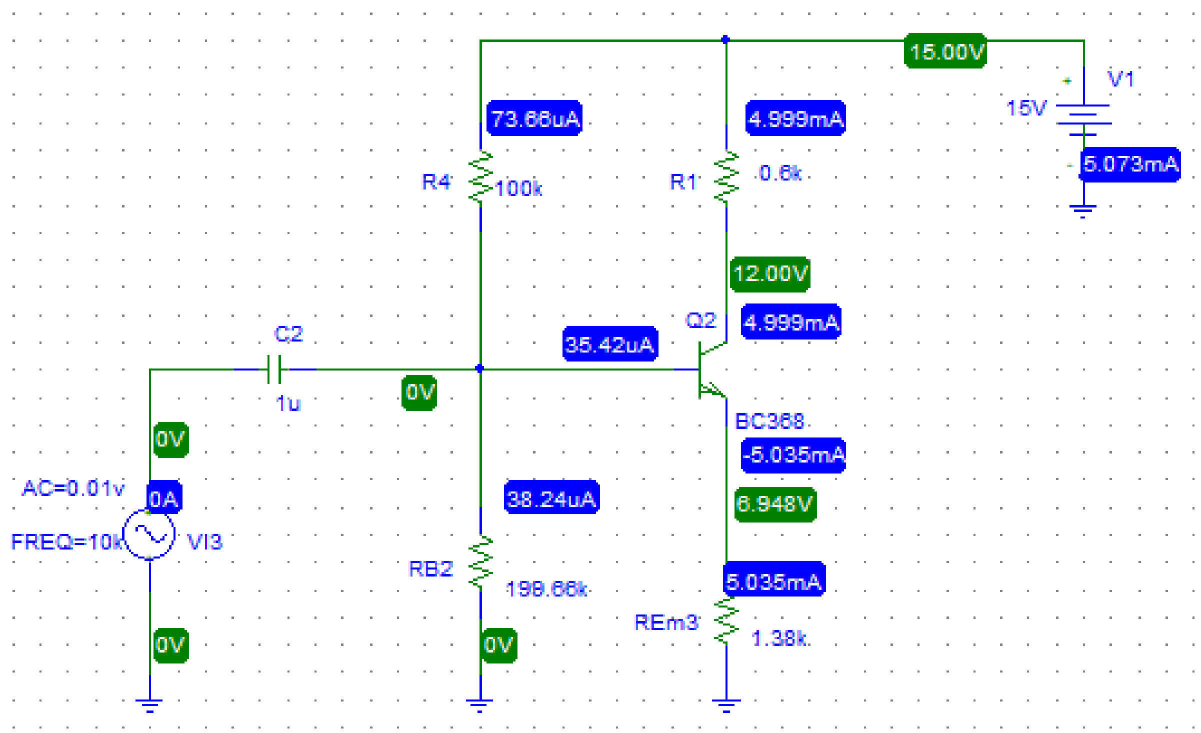
KVL I: $V_{th} - R_{th}\frac{I_c}{\beta} - V_{BE,ON} - 1.38 I_E = 0$

$$\rightarrow \frac{15 R_{B2}}{100 + R_{B2}} - \frac{100 R_{B2}}{100 + R_{B2}} \times \frac{5}{140.7} - 0.68 - \frac{1.38 \times 5}{10.993} = 0$$

$$\rightarrow \frac{11.45 R_{B2}}{100 + R_{B2}} = 7.629$$

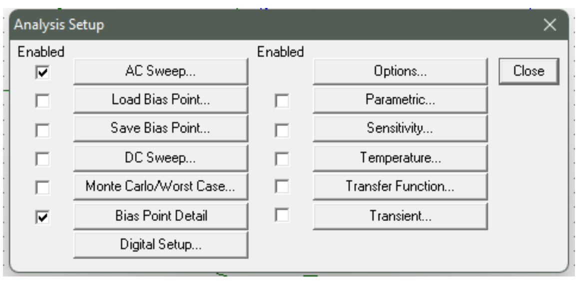
$$11.45 R_{B2} = 762.9 + 7.629 R_{B2} \rightarrow R_{B2} = 199.66\,k\Omega$$

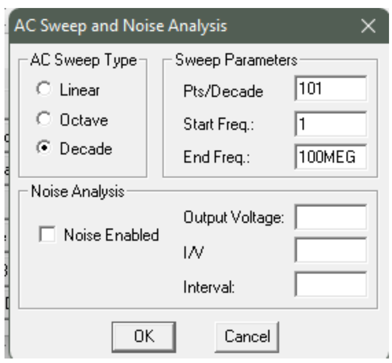
This Result can be confirmed after simulation:

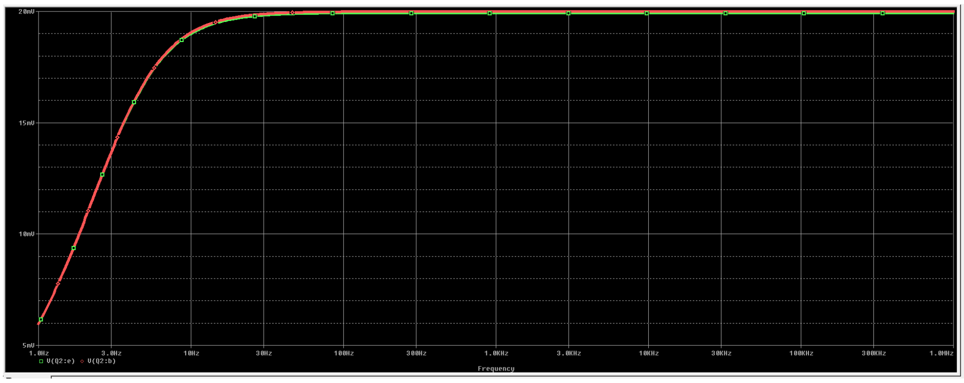


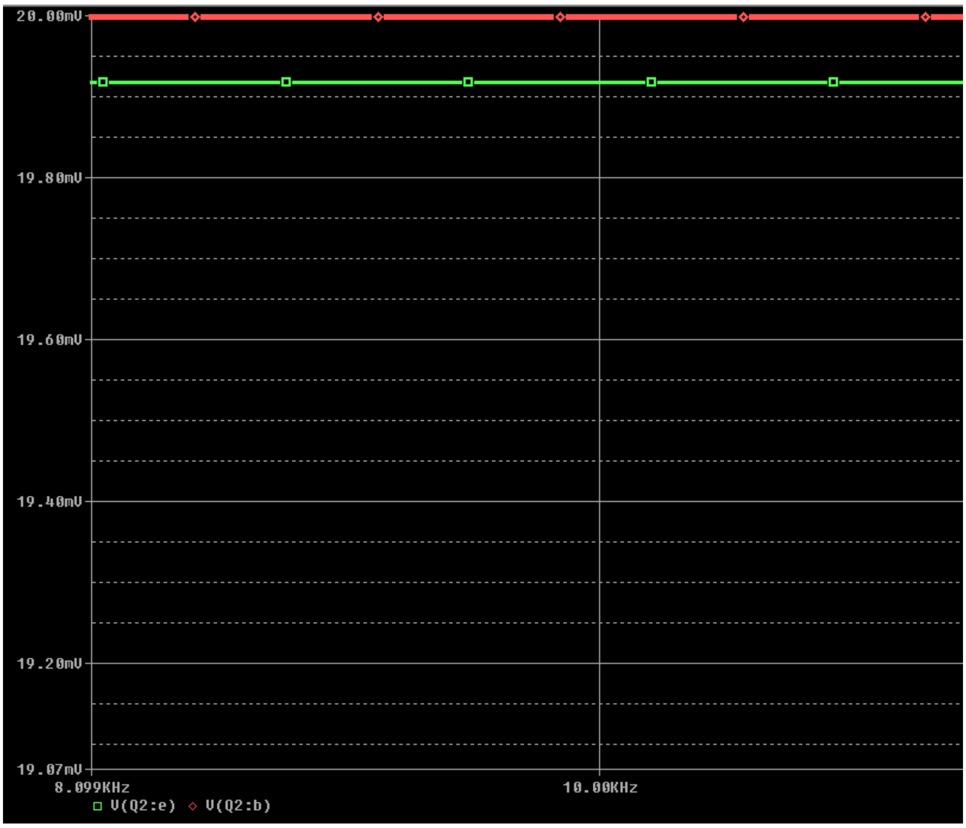
Exercise 1.4) Find A_{vs}

After AC Sweep Simulation:









$$V_s = 20mv, V_{out} = 19.92mv \rightarrow A_{vs} = 0.996$$

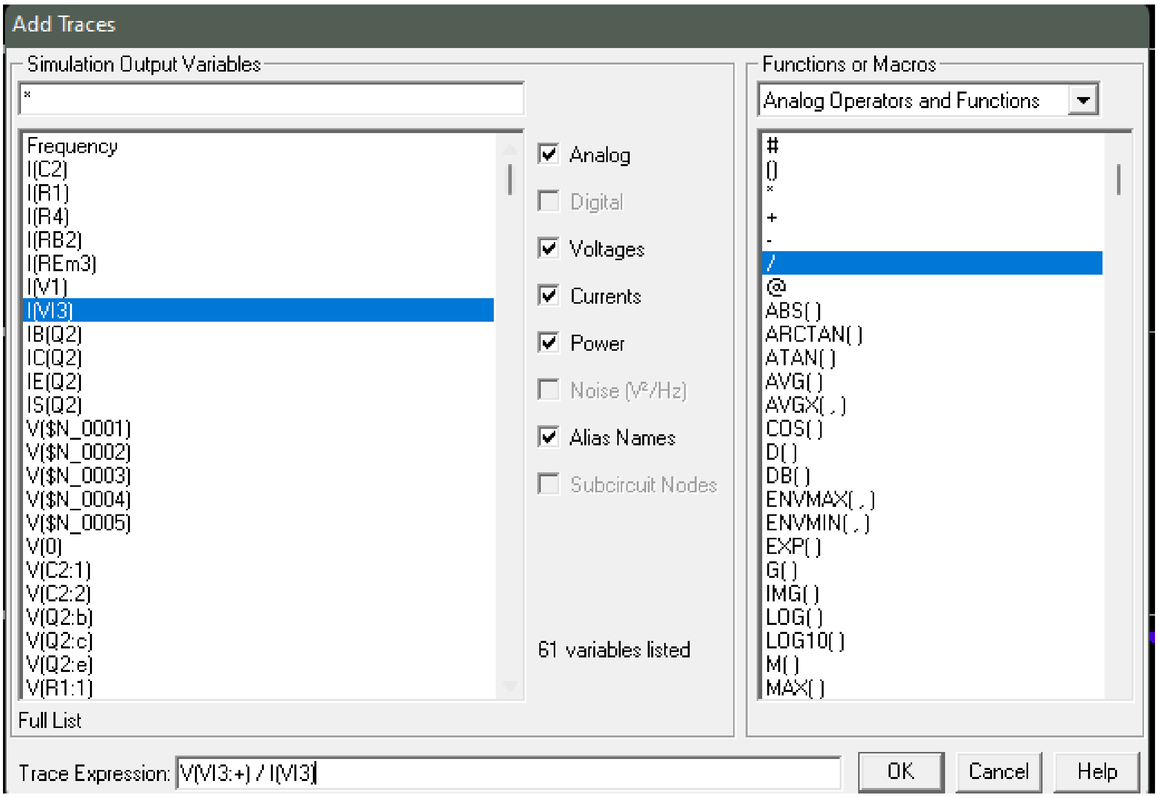
Exercise 1.5) Calculate the Input Impedance

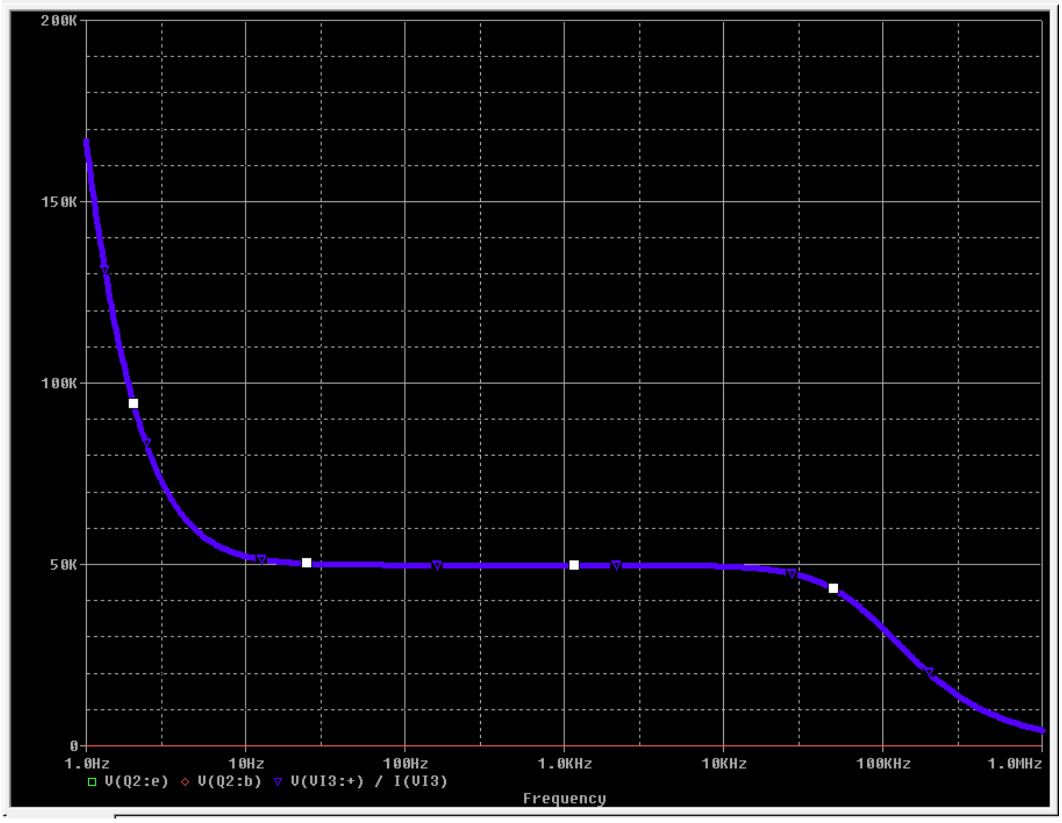
Theoretical Calculations:

$$\left.\begin{array}{l} V_T = 0.025v \\ I_{c3} = 5v \end{array}\right\} \rightarrow g_{m_3} = \frac{I_c}{V_T} = 200\,ms \rightarrow \frac{1}{g_{m_3}} = 5\Omega \rightarrow r_{\pi_3} = \frac{\beta}{g_m} = 703.5\,\Omega$$

$$R_{in} = R_{th_3} \parallel [r_{\pi_3} + (\beta+1)(R_E)] = 66.6 \parallel [0.7 + 141.7 \times 1.38] = 66.6 \parallel 196.2 = 49.7 \text{ k}\Omega$$

Simulation results: 50k



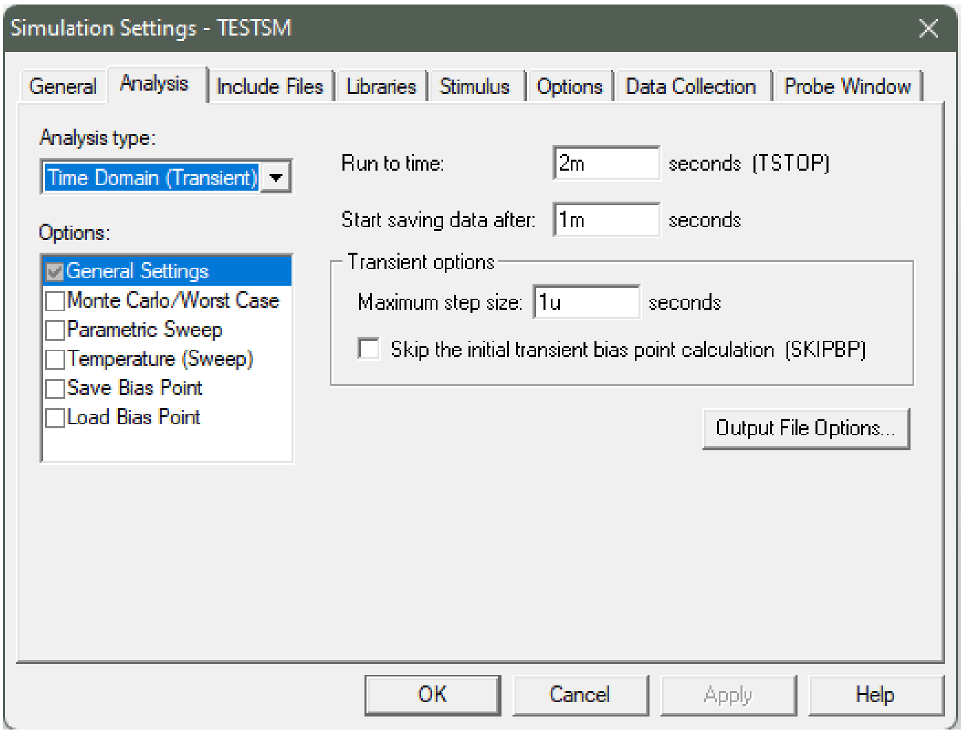


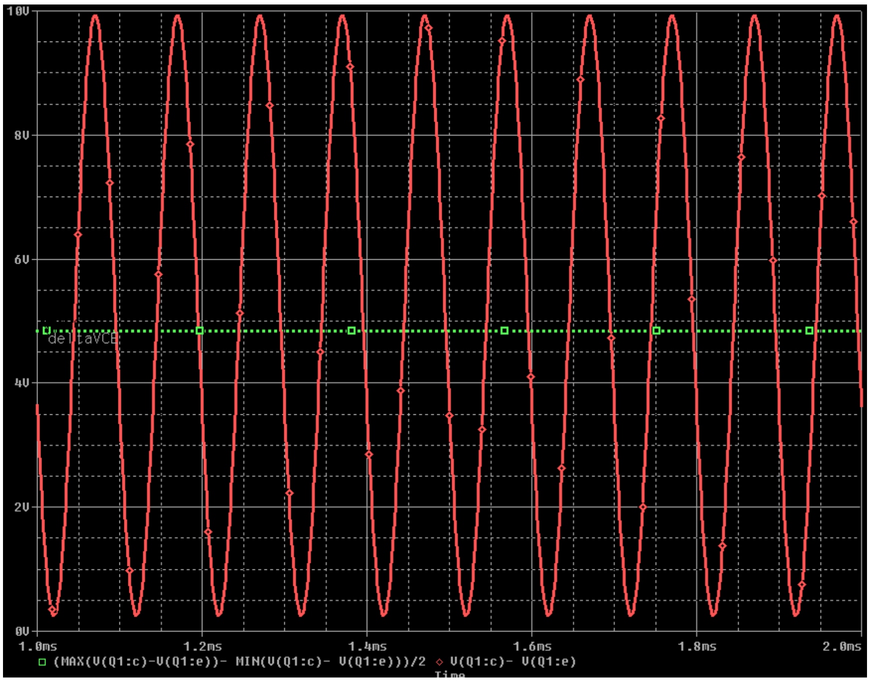
Exercise 1.6) Calculate the Maximum Symmetrical Swing of V_{CE}

Theoretical Calculations:

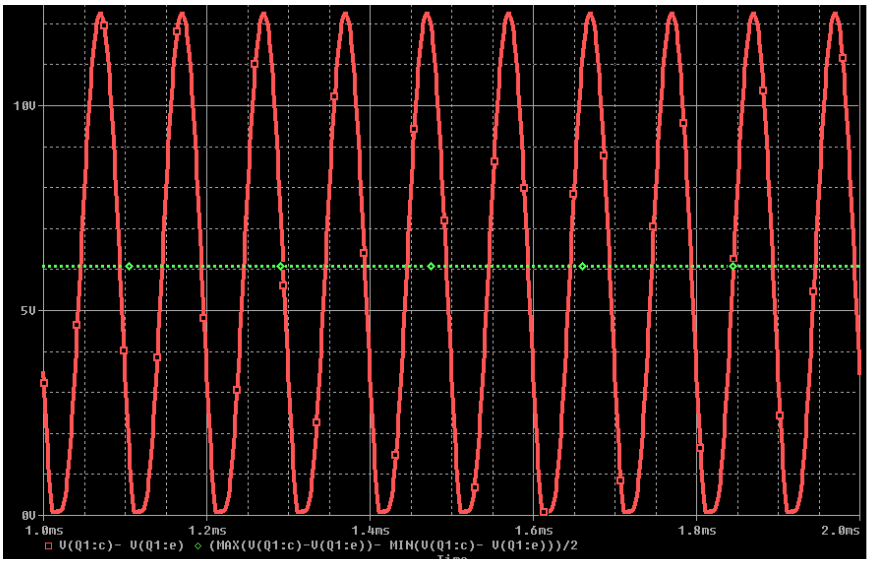
$$\text{swing \#3:} \begin{cases} \Delta_1 = V_{CEQ} - V_{CE,sat} = 4.85\,v \\ \Delta_2 = R_{ac} I_{CQ} = (0.6 + 1.38) \times 4.5 = 9.9\,v \end{cases} \Rightarrow \max \Delta V_{CE3} = \min(\Delta_1, \Delta_2) = 4.85\,v$$

Simulation Results:



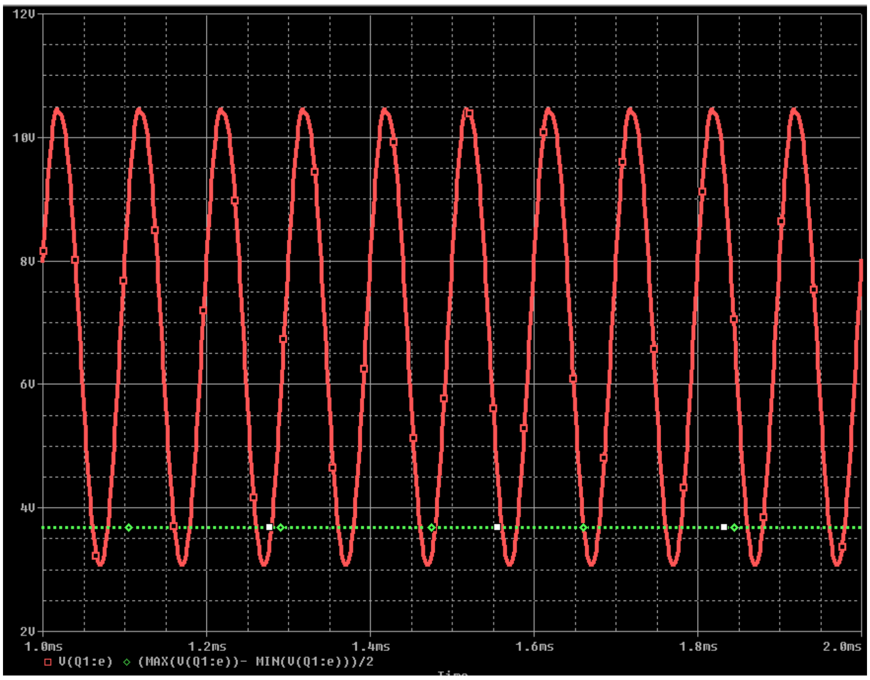


$$\Delta V_{CE} = 4.85v$$

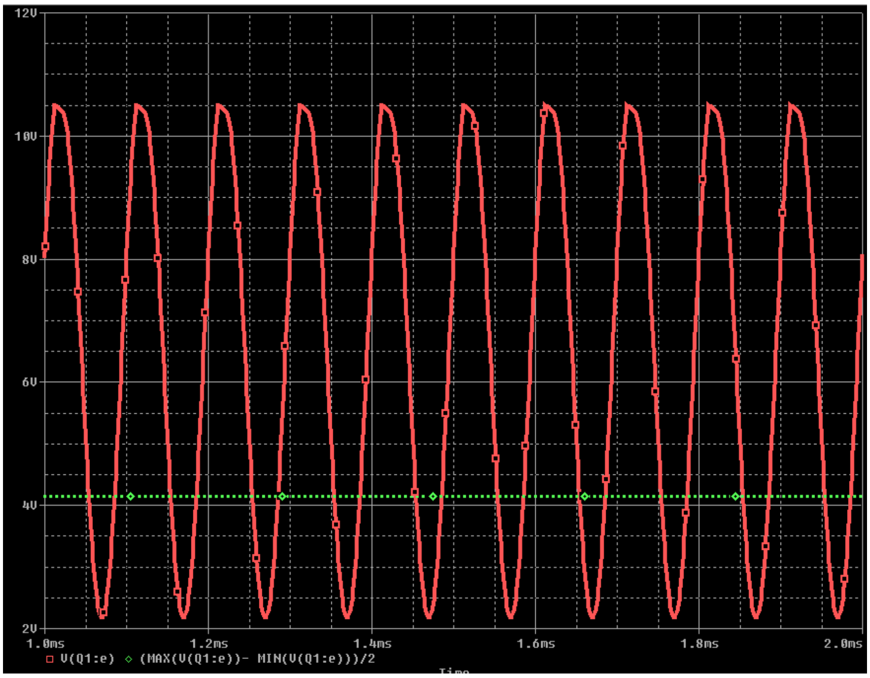


$$\Delta V_{CE} = 6v$$

Exercise 1.7) Calculate the Maximum Symmetrical Swing of the Output



$$\Delta V_o = \Delta V_E = 3.75v$$



$$\Delta V_o = \Delta V_E = 4.1v$$

Exercise 1.8) Calculate the Maximum Symmetrical Swing of the Input

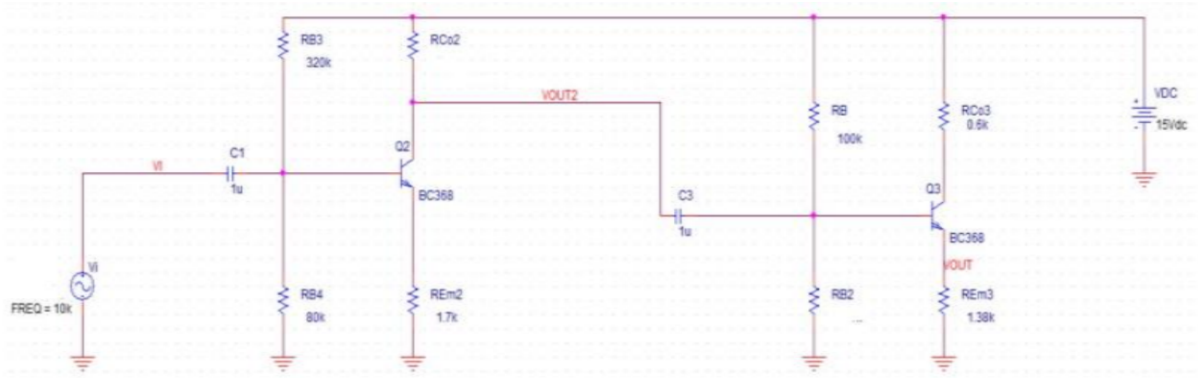
$$\left.\begin{array}{l} \Delta I_c = \dfrac{\Delta V_{ce}}{R_{ac}} , \\ \Delta V_o = \Delta I_c \times R_{Em3} \end{array}\right\} \rightarrow \Delta V_o = \Delta V_{CE} \times \frac{R_{Em3}}{R_{ac}} = \Delta V_{CE} \times \frac{R_{Em3}}{R_{co3}+R_{Em3}} = 4.85 \times \frac{1.38}{1.38+0.6} = 3.38V$$

$$\Delta V_o = A_{vs}\, \Delta V_s \longrightarrow \Delta V_{s_3} = \frac{\Delta V_{o3}}{A_{vs3}} = \frac{3.38}{0.996} = \underline{3.39\,V}$$

Exercise 1.9) What is the reason for using the common collector circuit for the third stage?

It is customary to use the common collector circuit as the last stage because it has a large input impedance and a small output impedance. It is suitable for connecting to the output load, and it also does not have much effect on the gain.

Section 2: Second Stage



Exercise 2.1) Why is the Emitter Degenerated circuit chosen for the second stage in amplifiers?

The Emitter Degenerated circuit is preferred for the second stage due to its ability to maintain stability against fluctuations in β. Moreover, it significantly enhances voltage gain, making it a strategic choice for optimizing amplifier performance.

Exercise 2.2) Choose the value of R_{Co2} such that $I_C = 1mA$ and $3 > |A_v| > 3.1.$

Theoretical Calculations:

$$I_{C2} = 1\,mA \rightarrow g_{m2} = \frac{I_{C2}}{V_T} = 40\,mS \rightarrow \frac{1}{g_{m2}} = 25\,\Omega \rightarrow r_{\pi 2} = \frac{\beta}{g_{m2}} = 3.05\,k\Omega$$

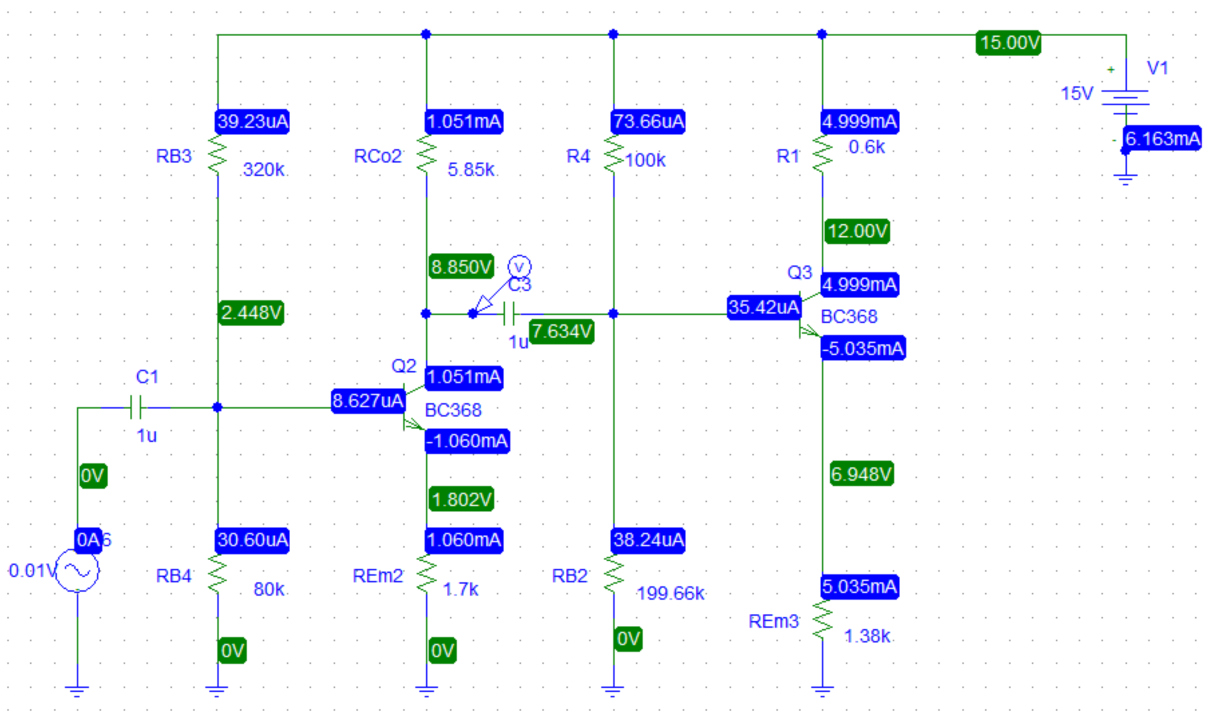
$$A_{v_2} = \frac{-R_{C(tot)}}{R_{E(tot)} + \frac{1}{g_{m2}}} = \frac{-(R_{co2} \parallel R_{in3})}{1.7 + \frac{1}{g_{m2}}} = \frac{-(R_{co2} \parallel 49.7\,k\Omega)}{1.7 + 0.025} = \frac{-(R_{co2} \parallel 49.7\,k\Omega)}{1.725}$$

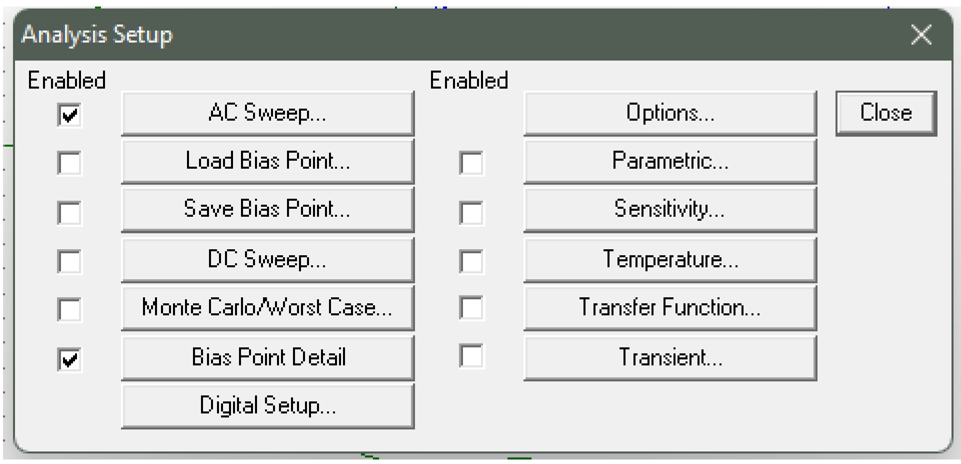
$$3 < |A_{V_2}| < 3.1 \longrightarrow 3 < \frac{R_{co} \parallel 49.7}{1.725} < 3.1 \rightarrow 5.175 < R_{co} \parallel 49.7 < 5.348$$

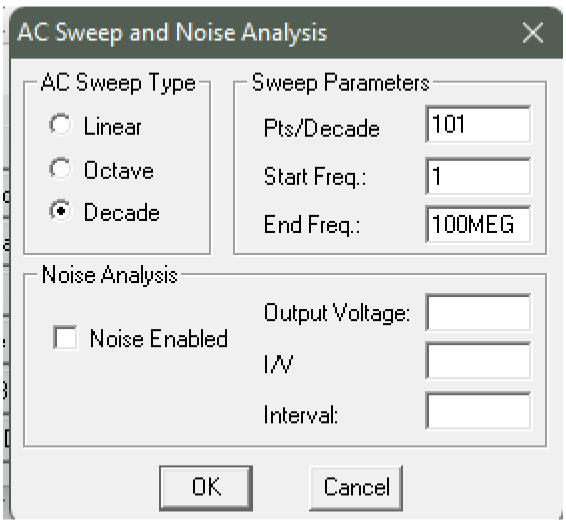
$$\rightarrow 0.187 < \frac{1}{R_{co_2}} + \frac{1}{49.7} < 0.193 \rightarrow 0.1669 < \frac{1}{R_{co2}} < 0.1729 \rightarrow 5.78 < R_{co2} < 5.99$$

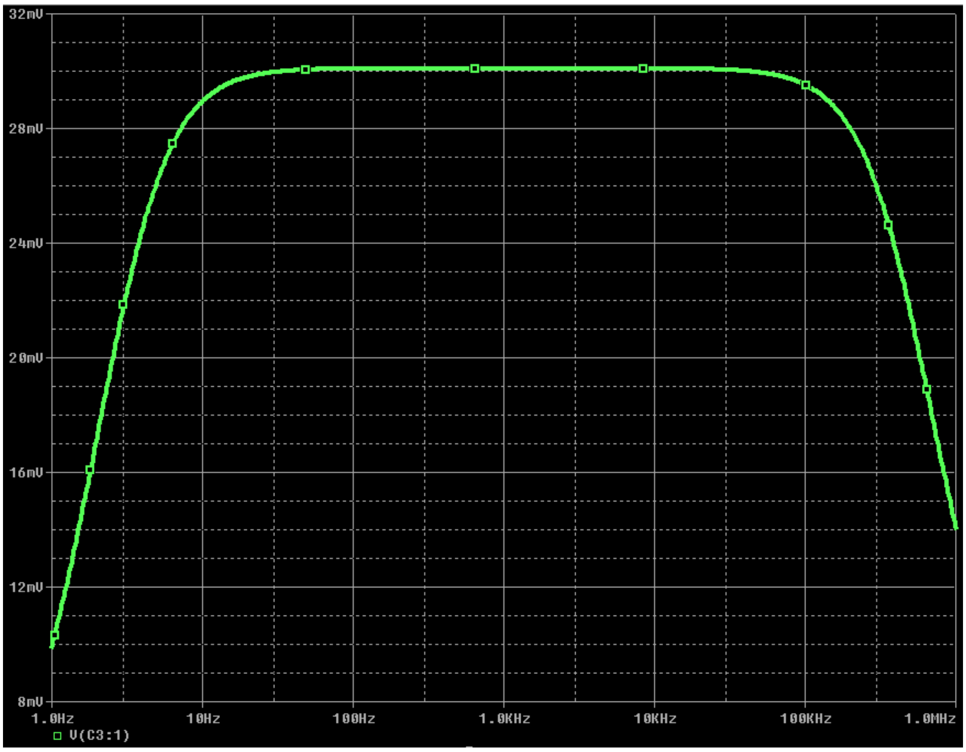
$$R_{co2} = 5.85\,k\Omega$$

Exercise 2.3) Find the voltage Gain


15.00V
V1
15V
6.163mA
39.23uA
1.051mA
73.66uA
4.999mA
RB3
320k
RCo2
5.85k
R4
100k
R1
0.6k
12.00V
8.850V
C3
Q3
4.999mA
2.448V
35.42uA
1u
7.634V
BC368
-5.035mA
C1
Q2
1.051mA
8.627uA
BC368
1u
-1.060mA
0V
6.948V
1.802V
0A
0.01V
30.60uA
1.060mA
38.24uA
5.035mA
RB4
80k
REm2
1.7k
RB2
199.66k
REm3
1.38k
0V
0V
0V


Analysis Setup
Enabled
Enabled
AC Sweep...
Options...
Close
Load Bias Point...
Parametric...
Save Bias Point...
Sensitivity...
DC Sweep...
Temperature...
Monte Carlo/Worst Case...
Transfer Function...
Bias Point Detail
Transient...
Digital Setup...


AC Sweep and Noise Analysis
AC Sweep Type
Linear
Octave
Decade
Sweep Parameters
Pts/Decade
101
Start Freq.:
1
End Freq.:
100MEG
Noise Analysis
Noise Enabled
Output Voltage:
I/V
Interval:
OK
Cancel



$$V_s = 10mv, V_{out} = 30mv \rightarrow A_{vs3} = 3$$

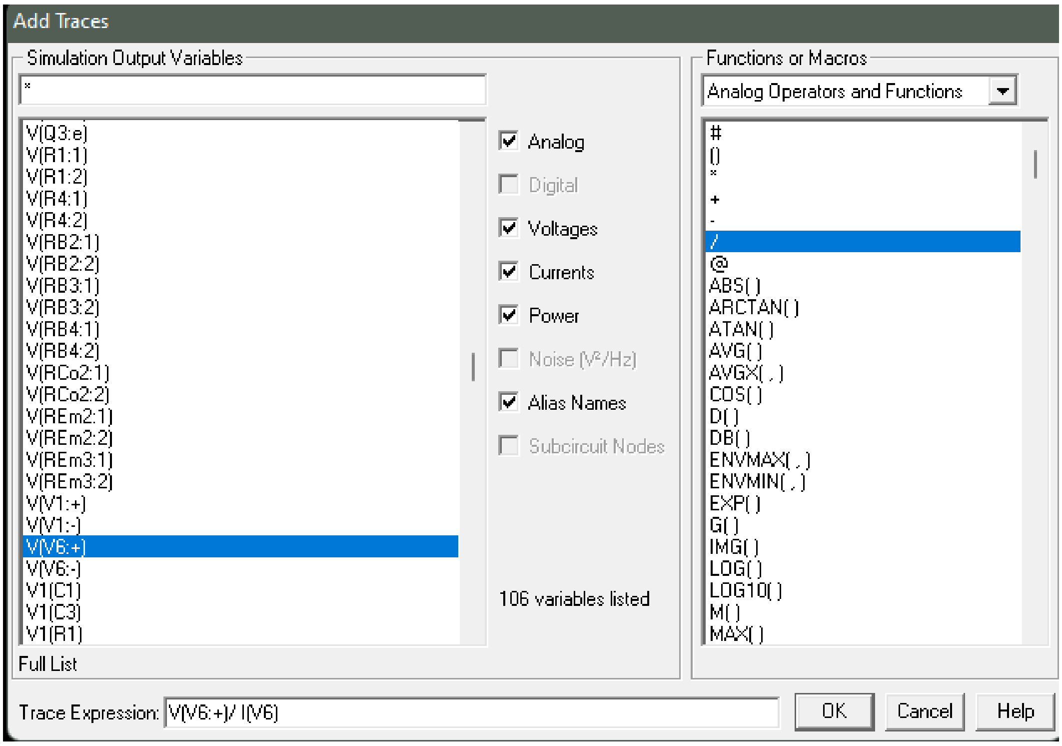
Exercise 2.4) Calculate the Input Impedance

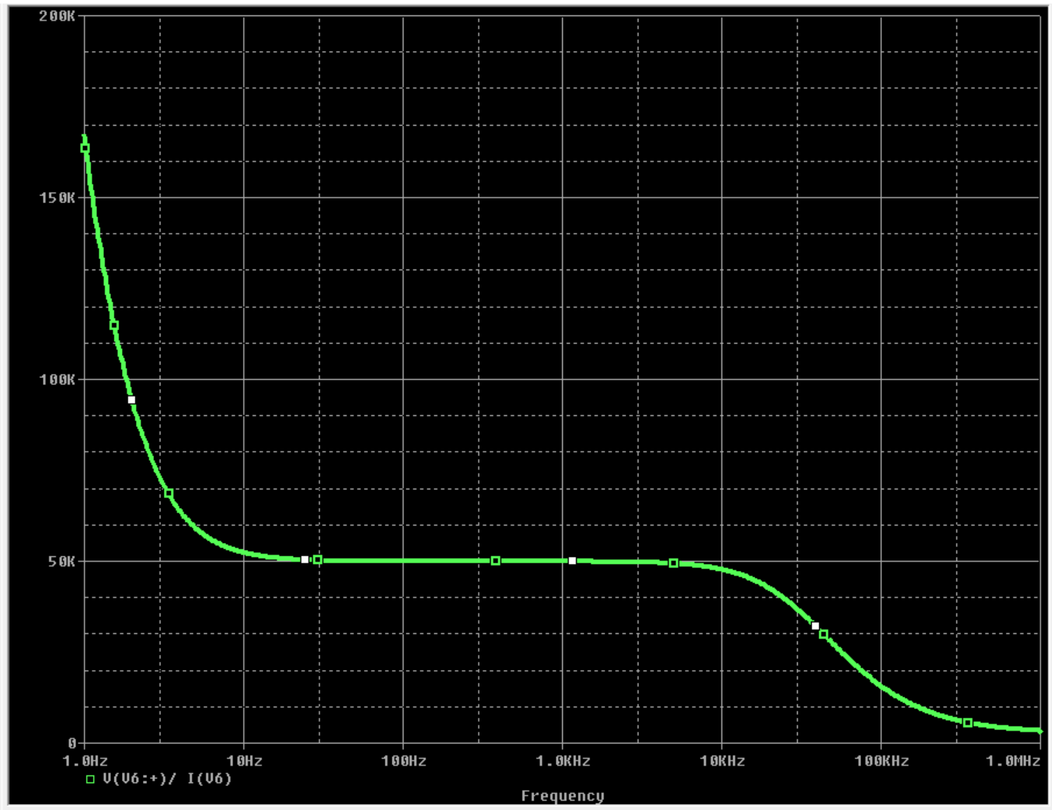
Theoretical Calculations:

$$\beta_2 = \frac{I_{C2}}{I_{B2}} = 122$$

$$R_{in2} = [r_{\pi 2} + (\beta+1)R_{E2}] \,\|\, 320 \,\|\, 80 = [\underbrace{3.05 + (123)(1.7)}_{212.15}] \,\|\, \underbrace{320 \,\|\, 80}_{64} = 49.2\ k\Omega$$

Simulation Result: $R_{in} = 50k$





Section 3: First Stage

Exercise 3.1) Why is the Common Base circuit chosen for the first stage in amplifiers?

The Common Base circuit has low input impedance and usually has high voltage gain. Also it tends to exhibit better high-frequency response compared to other configurations, making it suitable for applications where signal bandwidth is important.

Exercise 3.2) Choose the value of R_{B6} such that $8\Omega > R_{in} > 10\Omega$.

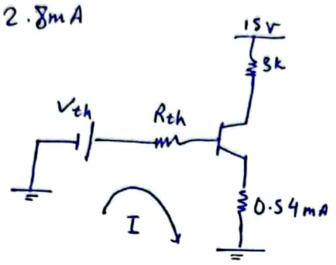
$\beta_1 = 140$

$$R_{in_1} = R_{E_1} \| \frac{1}{g_{m_1}} = 0.54 \| \frac{1}{g_{m1}} \longrightarrow \frac{1}{R_{in1}} = \frac{1}{0.54} + g_{m1} \xrightarrow[R_{in} \times 10^3 \ \Omega^{-1}]{8\Omega < R_{in} < 10\Omega} 100 < \frac{1}{R_{in}} < 125$$

$$\longrightarrow 100 < \frac{1}{0.54} + g_{m1} < 125 \longrightarrow 98.15 < g_{m1} < 125.15 \xrightarrow[\times \frac{1}{40}]{g_m = \frac{I_{CQ}}{V_T}} 2.45 < I_{CQ_1} < 3.13$$

$$\xrightarrow{\text{انتخاب}} I_{CQ_1} = 2.8mA$$

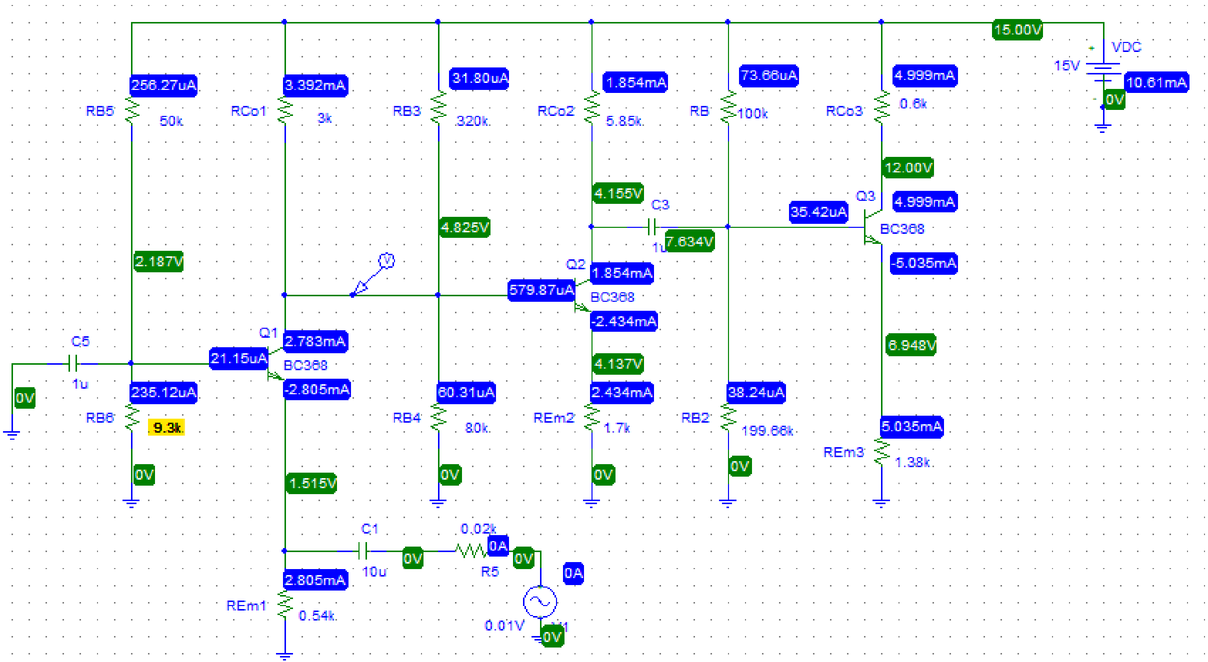
DC analysis

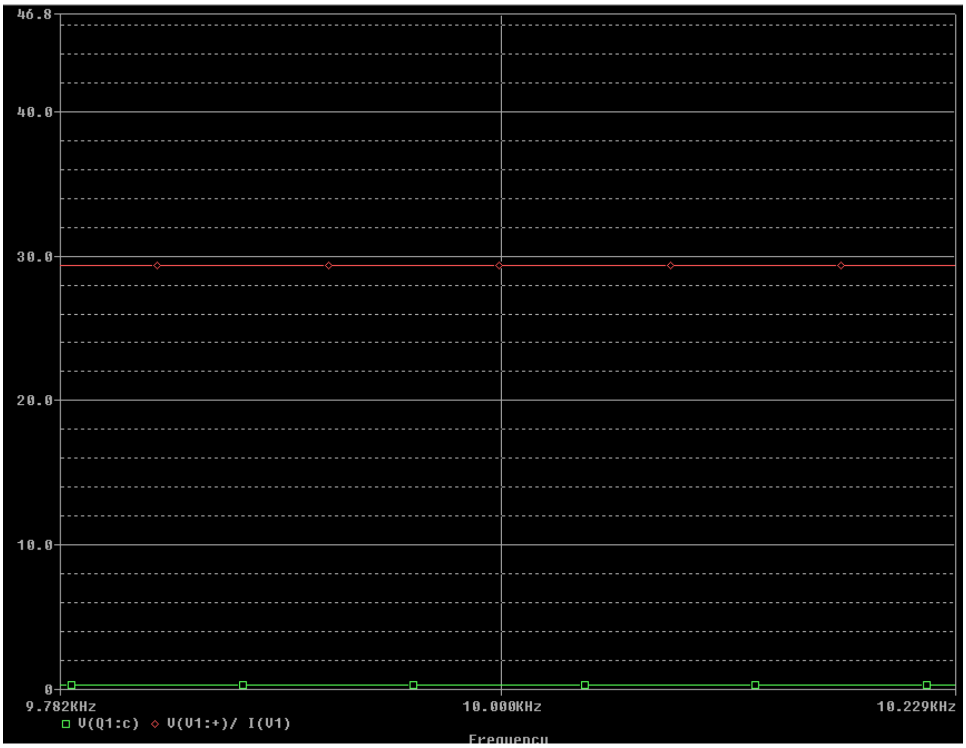


$$V_{th} = \frac{15 R_{B6}}{50 + R_{B6}} \quad , \quad R_{th} = \frac{50 R_{B6}}{50 + R_{B6}}$$

$$\text{KVL I}: \ V_{th} - R_{th} I_{b_1} - V_{BE,ON} - 0.54 I_{C_1} \longrightarrow \frac{15 R_{B6}}{50 + R_{B6}} - \frac{50 R_{B6} \times \frac{2.8}{140}}{50 + R_{B6}} = 0.68 + 0.54 \times 2.8$$

$$\longrightarrow \frac{14 R_{B6}}{50 + R_{B6}} = 2.19 \longrightarrow 14 R_{B6} = 109.5 + 2.19 R_{B6} \longrightarrow 11.81 R_{B6} = 109.5 \rightarrow R_{B6} = 9.27 \ k\Omega$$





$$R_{in1} = 29\Omega - 20\Omega = 9\Omega$$

Exercise 3.3) Choose the value of R_{Co1} such that $A_v > 275.$

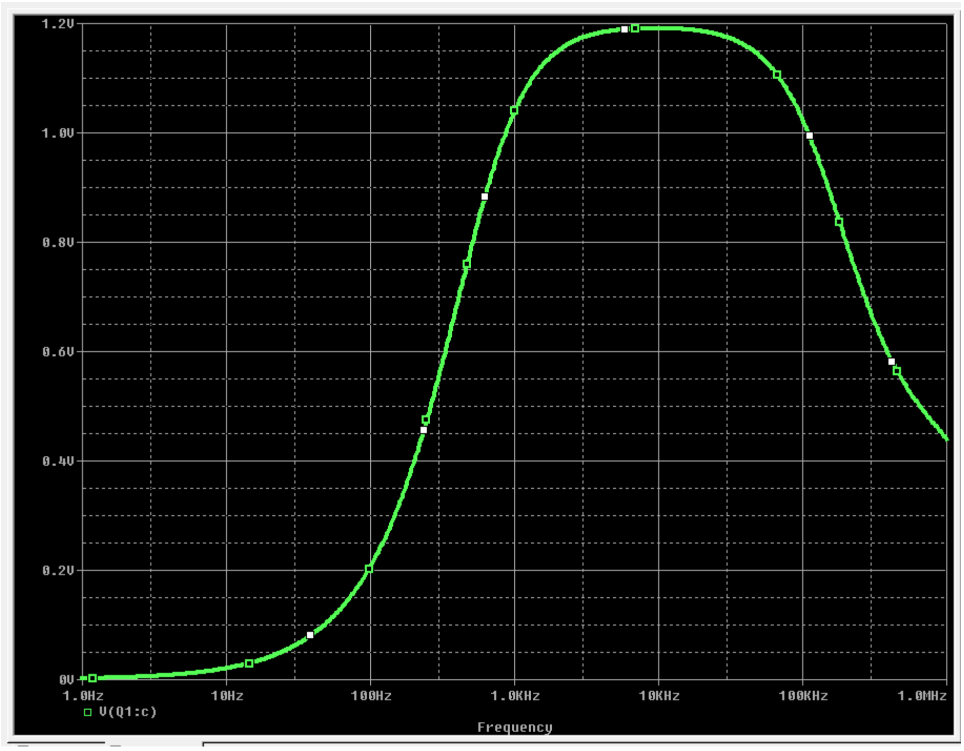
Theoretical Calculation:

$$A_{v_1} = (R_{c_1} \| tot1) \cdot g_{m1} = (R_{co1} \| R_{in2})(112) = (R_{co1} \| 49.2)(112)$$

$$A_v > 275 \rightarrow R_{co1} \| 49.2 > 2.46 \rightarrow \frac{1}{R_{co1}} + \frac{1}{49.2} < \frac{1}{2.46} \rightarrow \frac{1}{R_{co1}} < 0.386$$

$$\rightarrow R_{co1} > 2.58 \xrightarrow{\text{انتخاب}} \underline{R_{co1} = 4k\Omega} \rightarrow A_{v_1} = 120$$

Simulation Results:

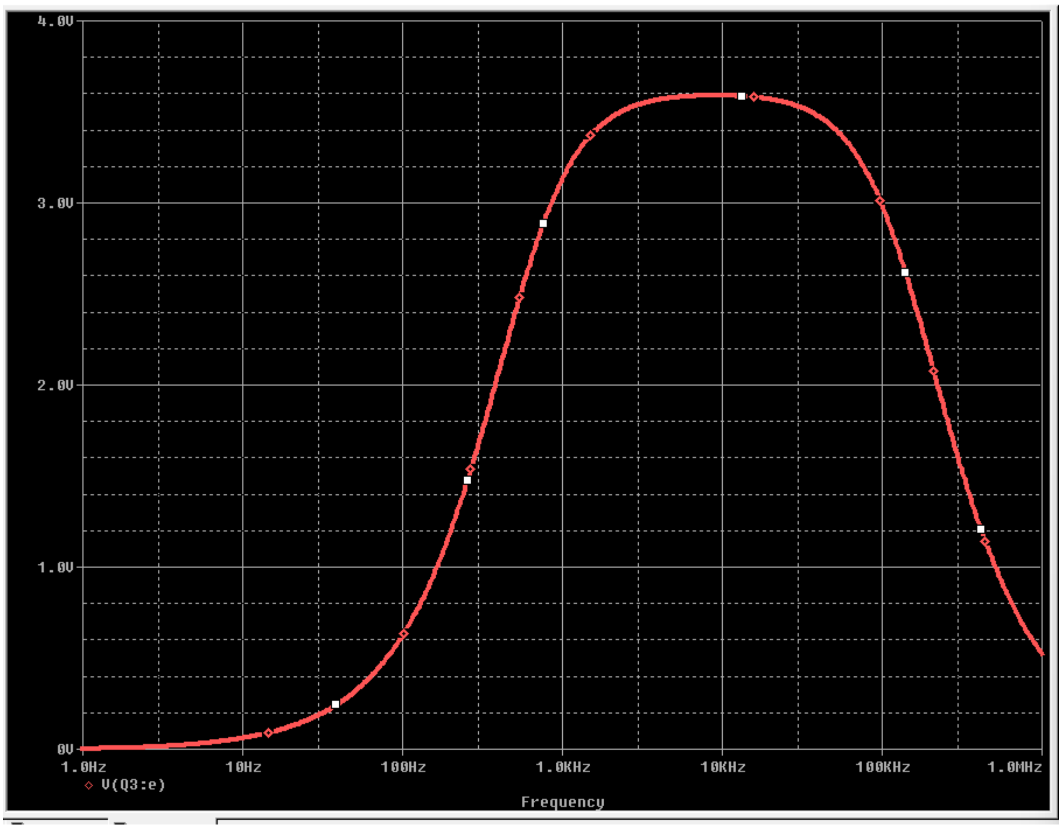


Exercise 3.4) Calculate the value of A_{vs1}

$$A_{vs1} = \frac{R_{in}}{R_s + R_{in}} A_v = \frac{8.78}{8.78 + 20} \times 316.69 = 96.6$$

Exercise 3.5) Calculate the value of $A_{V_{tot}}$

$$A_v = A_{v_1} \times A_{v_2} \times A_{v_3} = 120 \times 3.01 \times 0.996 \simeq 360$$



Exercise 3.7) If we don't use capacitors in the connections between different stages, what problems might we encounter?

1. **Noise and Interference Transmission:** Capacitors are used to allow the passage of AC signals (time-varying signals) and filter out high-frequency noise. Without capacitors in inter-stage connections, electromagnetic noise and disturbances may propagate along the transmission path and affect higher stages.
2. **Impedance Mismatch:** Capacitors can assist in impedance matching between different stages. The absence of capacitors may lead to power transmission losses and energy dissipation in the connections.
3. **Phase Shift:** Capacitors can introduce phase shifts in AC signals, influencing the behavior and frequency response of circuits. Not using capacitors may result in unintended phase shifts.
4. **Optimal Bandwidth Utilization:** In circuits with high frequencies, capacitors play a crucial role in signal transmission. Not using capacitors may restrict the bandwidth of the circuits, reducing efficiency at higher frequencies.