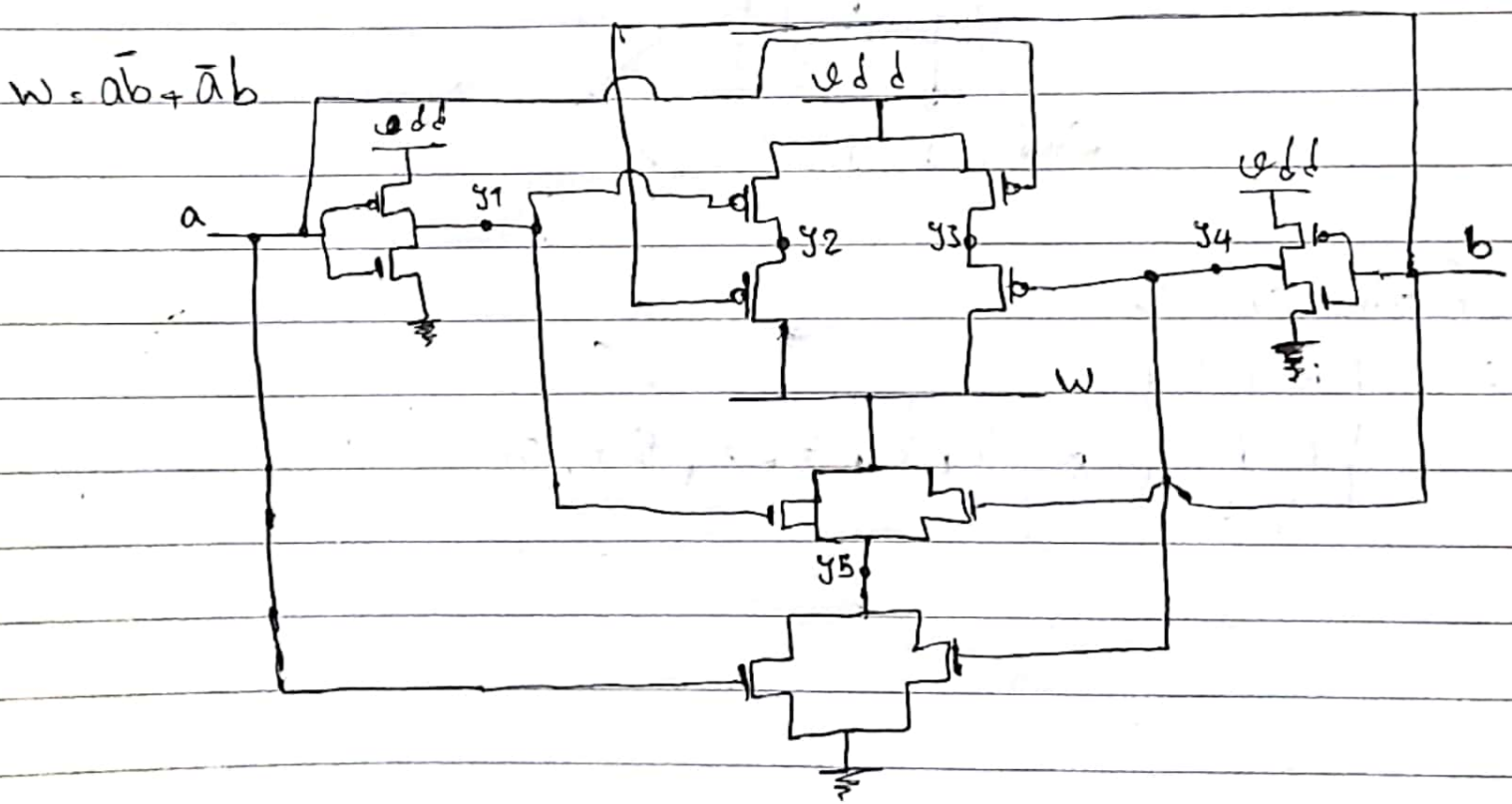
Digital systems _ HW2 _ 86198365 _ Mahdi Bakhal

(1)

$W = a\bar{b} + \bar{a}b$



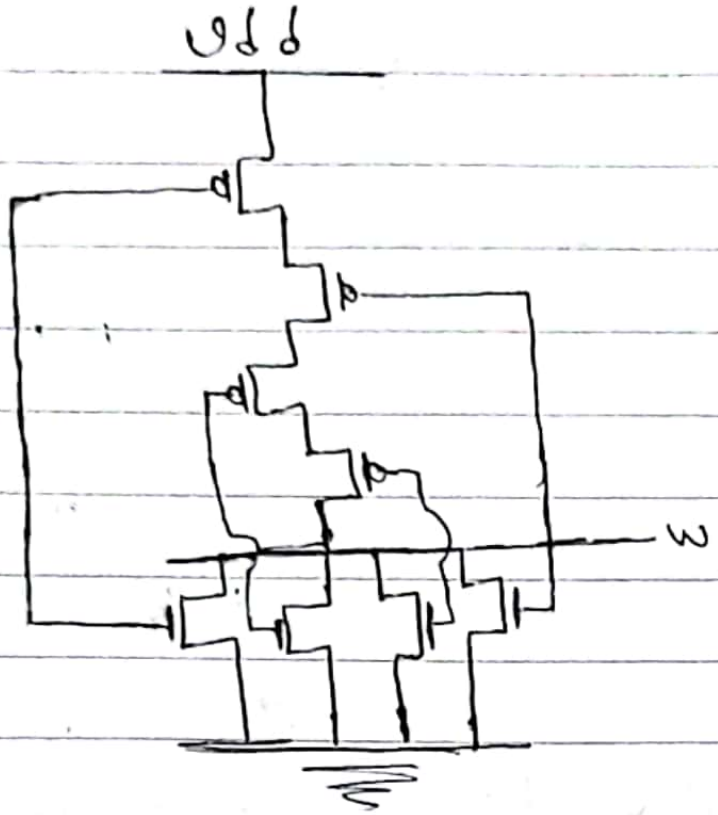
(3)

worst_case delay

To1: {a=0, b=1} → inverter 2pmos: 9 + 18 = 27 ns

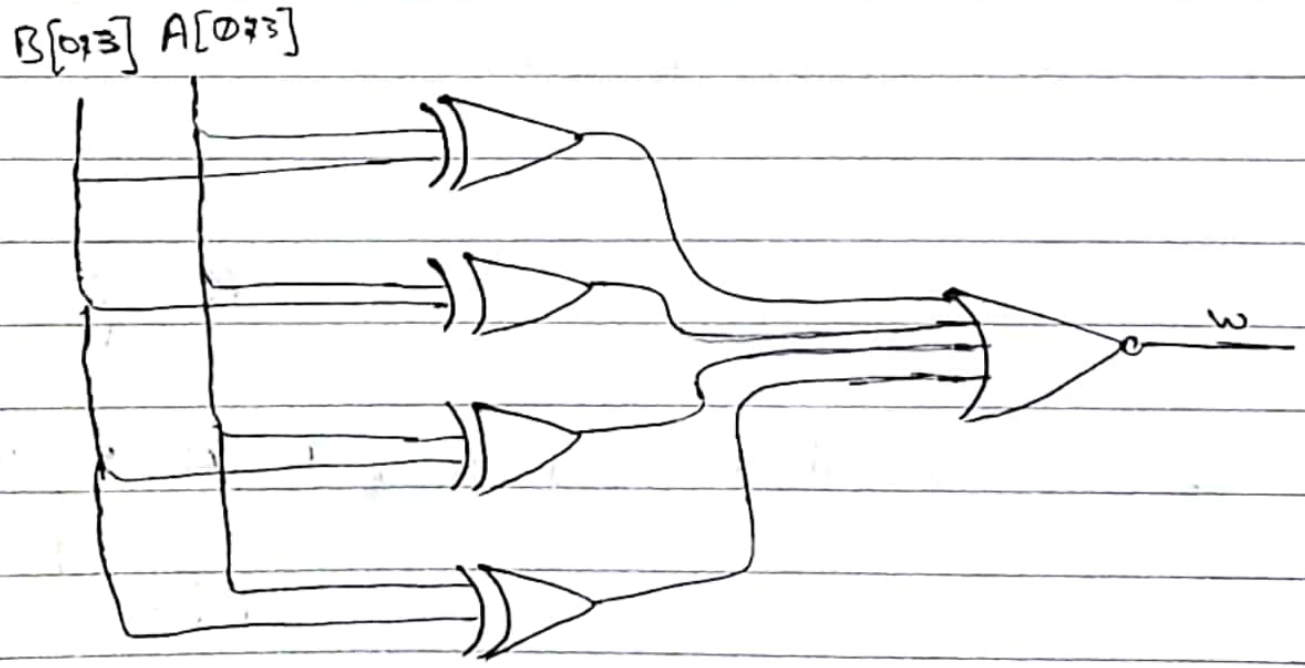
To0: {a=0, b=0} → inverter 2pmos: 7 + 18 = 25 ns

(4.)



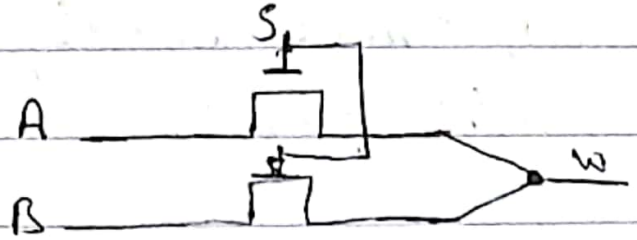
The worst_case scenario occurs when all 4 Pmos transistors want to send Toz as output and because they are in series It takes 36ns.

(5)



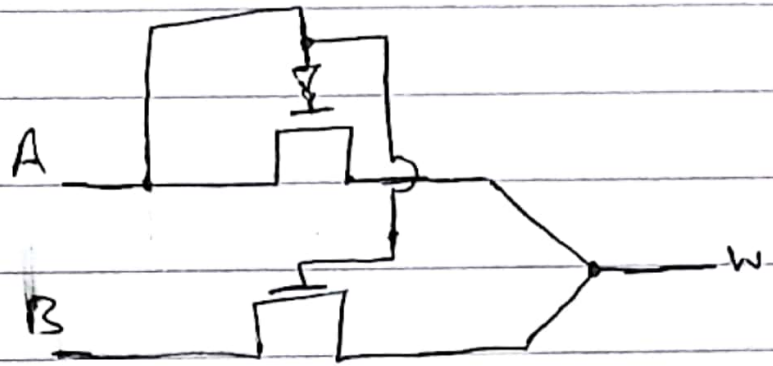
(7)

MUX :



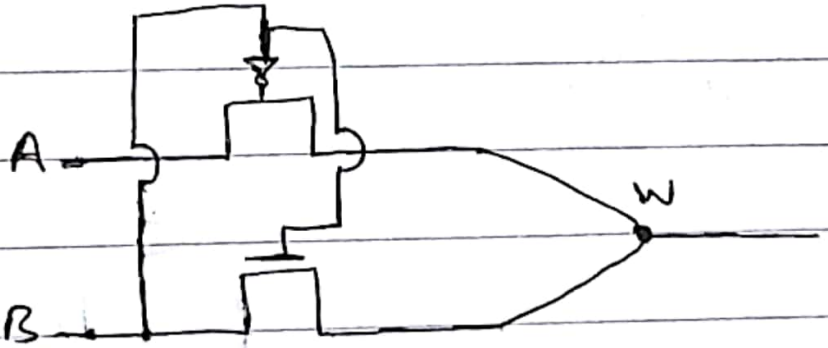
$W = AS + B\bar{S}$

AND :



$W = A\bar{A} + AB = AB$

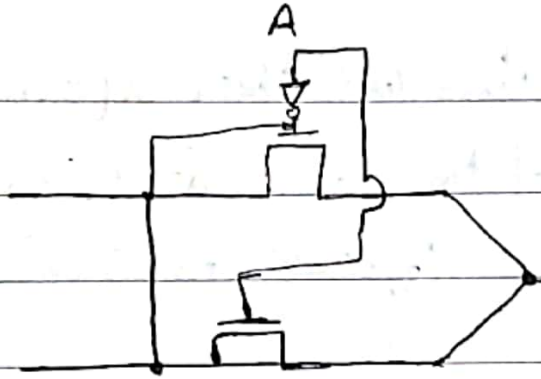
OR :



$W = A\bar{B} + BB = A\bar{B} + B$

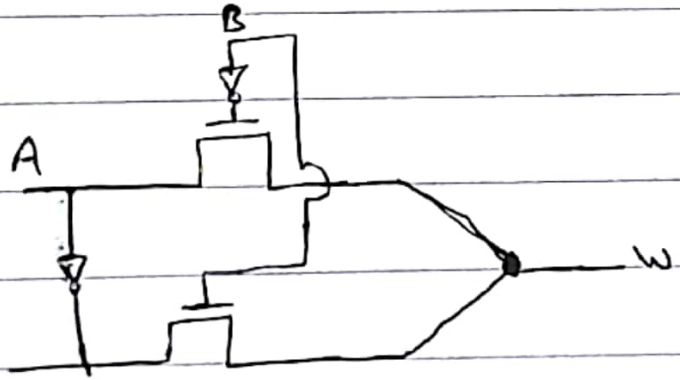
AB	$A\bar{B}$	B	W
00	0	0	0
01	0	1	1
11	0	1	1
10	1	0	1

Not Gate:



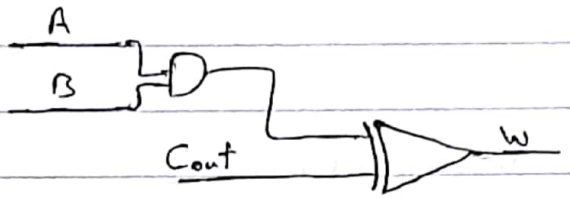
$W = \bar{A}\bar{A} + A\bar{A} = \bar{A} + A\bar{A} = \bar{A}$

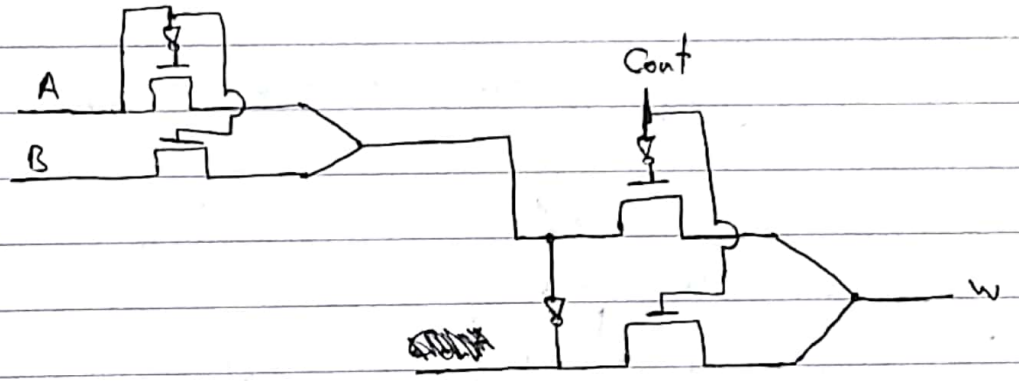
XOR Gate:



$W = A\bar{B} + \bar{A}B$

(8) If we have two numbers and represent those like this: a[0:n] and b[0:n], now we can assume the most significant bit of two numbers as A and B.
To detect overflow we can XOR Cin and Cout together and calculate Cin we can calculate A.B.



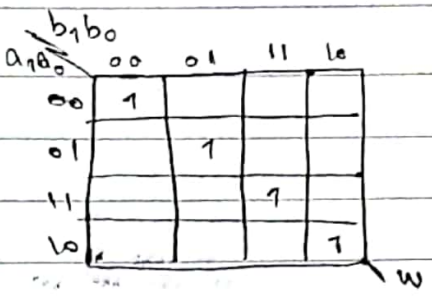


number of transistors = 16

worst_case: { A=1, B=1, Cout=1 } → 9 + 7 + 9 + 9 + 5 = 39 ns

(9)

a_1	b_1	a_0	b_0	w
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

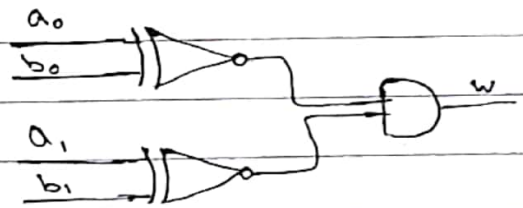


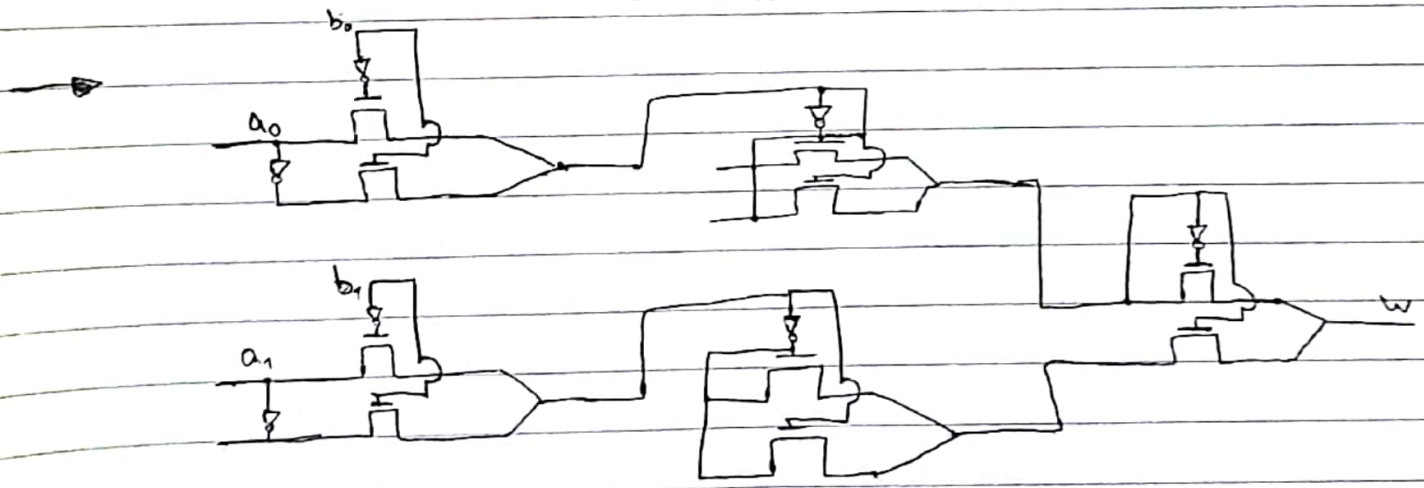
$$w = \bar{a}_1\bar{a}_0\bar{b}_1\bar{b}_0 + \bar{a}_1a_0\bar{b}_1b_0 + a_1a_0b_1b_0 + a_1\bar{a}_0b_1\bar{b}_0$$

$$= \bar{a}_1\bar{b}_1(\bar{a}_0\bar{b}_0 + a_0b_0) + a_1b_1(a_0b_0 + \bar{a}_0\bar{b}_0)$$

$$= (\bar{a}_1\bar{b}_1 + a_1b_1)(\bar{a}_0\bar{b}_0 + a_0b_0)$$

$$= (a_1 \otimes b_1)(a_0 \otimes b_0)$$





number of transistors = 24

Worst_case delay =