Partition into Hybrid Processor/Accelerator System

- Hybrid Design Flow

Compilation

↓

Execution & Profiling

↓

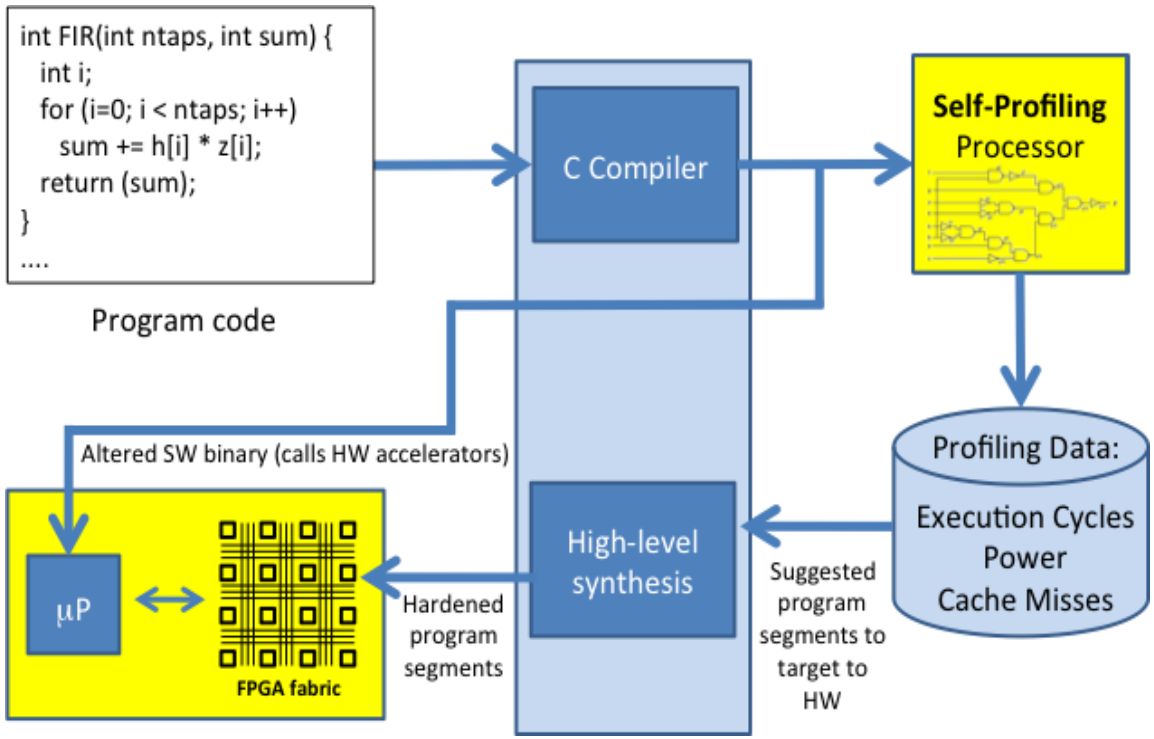
Partition Analysis

↓

LegUp HLS

↓

Hybrid System



- Partition is based on benefits of acceleration

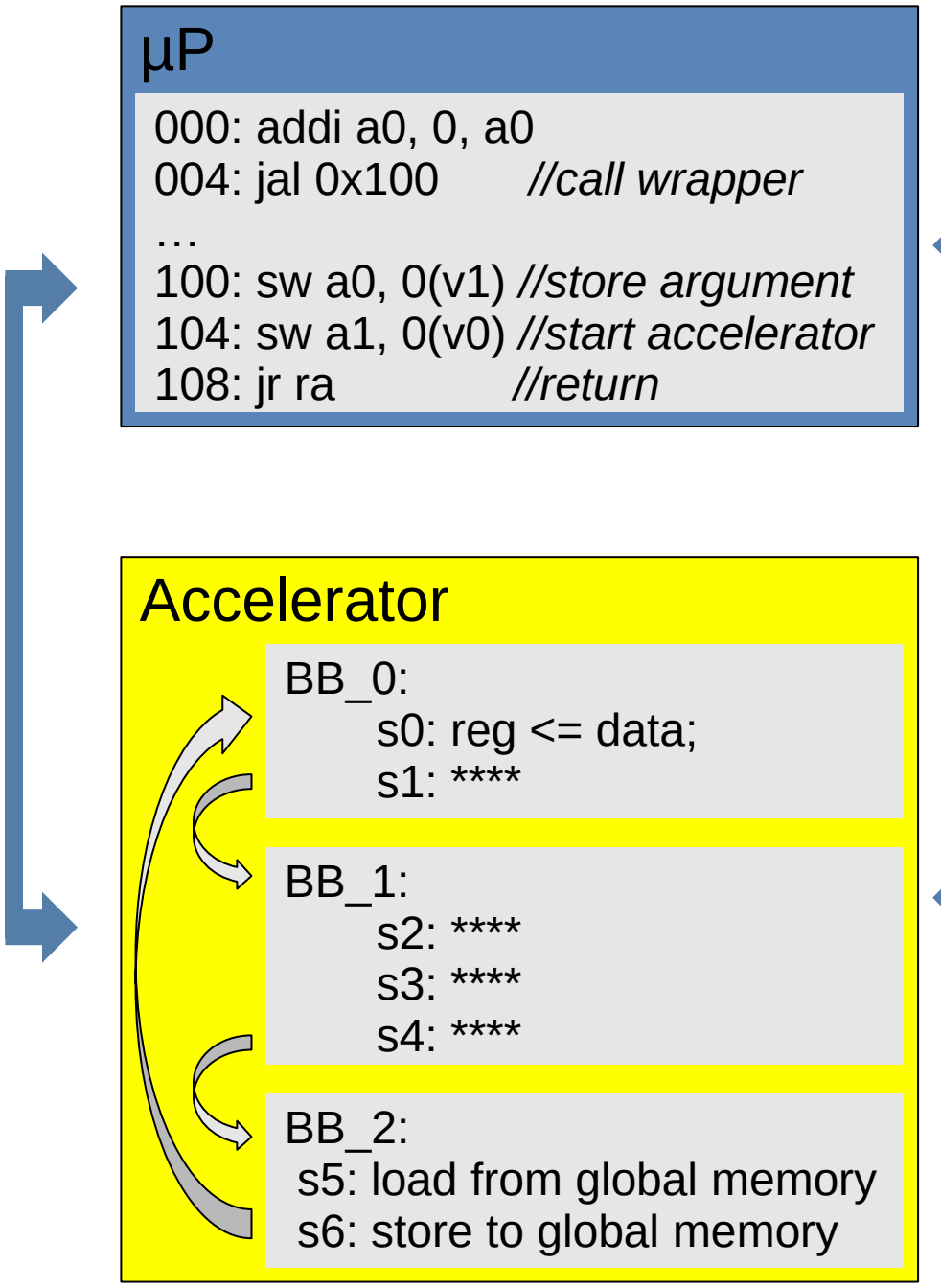
Hybrid System Cycle Prediction

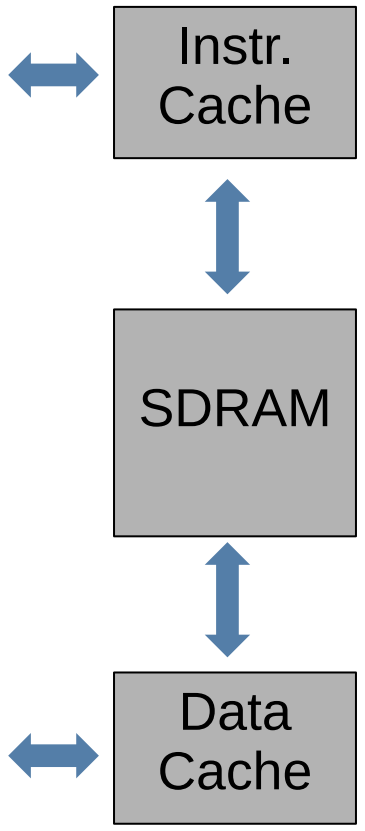
- Slow to profile a hybrid system
  - Synthesize to FPGA programming bit-stream
  - Simulate the system via ModelSim

- Goal
  - Quick/early prediction of the speed benefits of accelerating a function in HW

- Gain = SW cycle / Hybrid Cycle
  - SW cycle: HW profiler
  - Hybrid cycle: Prediction

Hybrid System Execution Flow



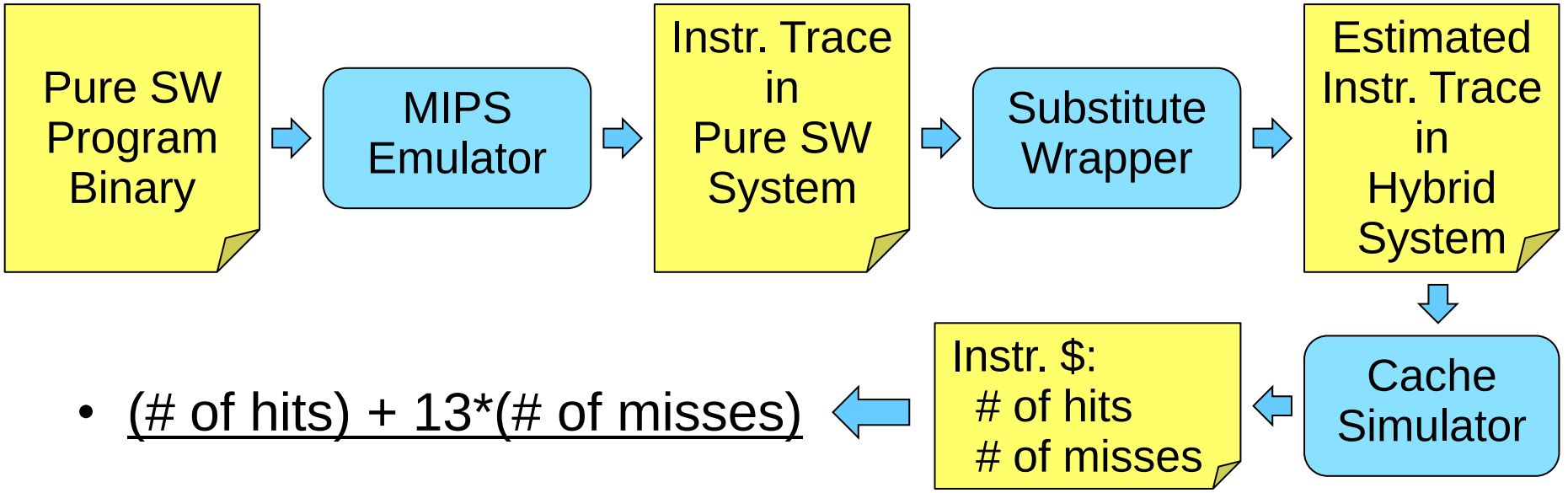


4 Components:

- SW wrapper
  - fetch instruction
  - store arguments
  - trigger start signal
- FSM in accelerator
- Data loads
- Data stores

Component I - SW Wrapper

- Instruction Fetch



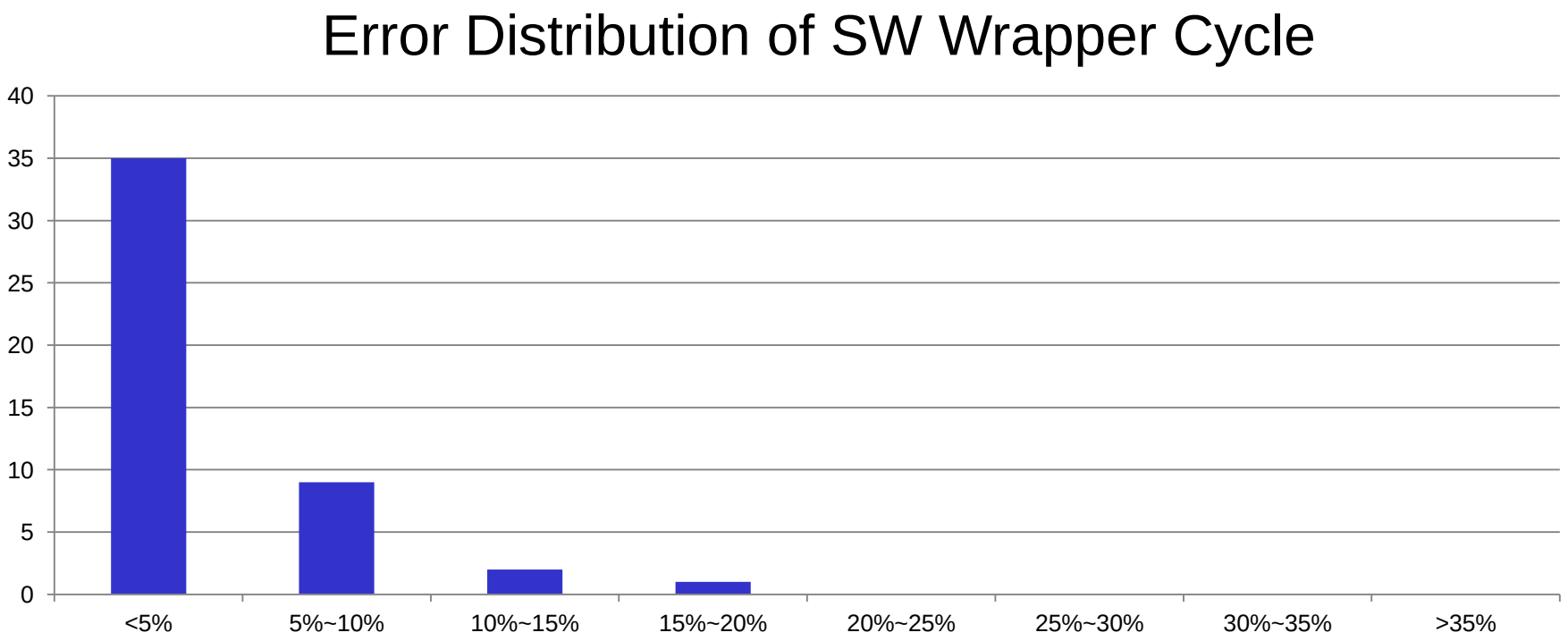
- Argument Overhead
  - ~2 cycles to store each argument
  - 2*(# of arguments)*(# of runs)

- SW/HW Transition
  - Constantly 2 cycle to transit b/w HW & SW
  - 2*(# of runs)

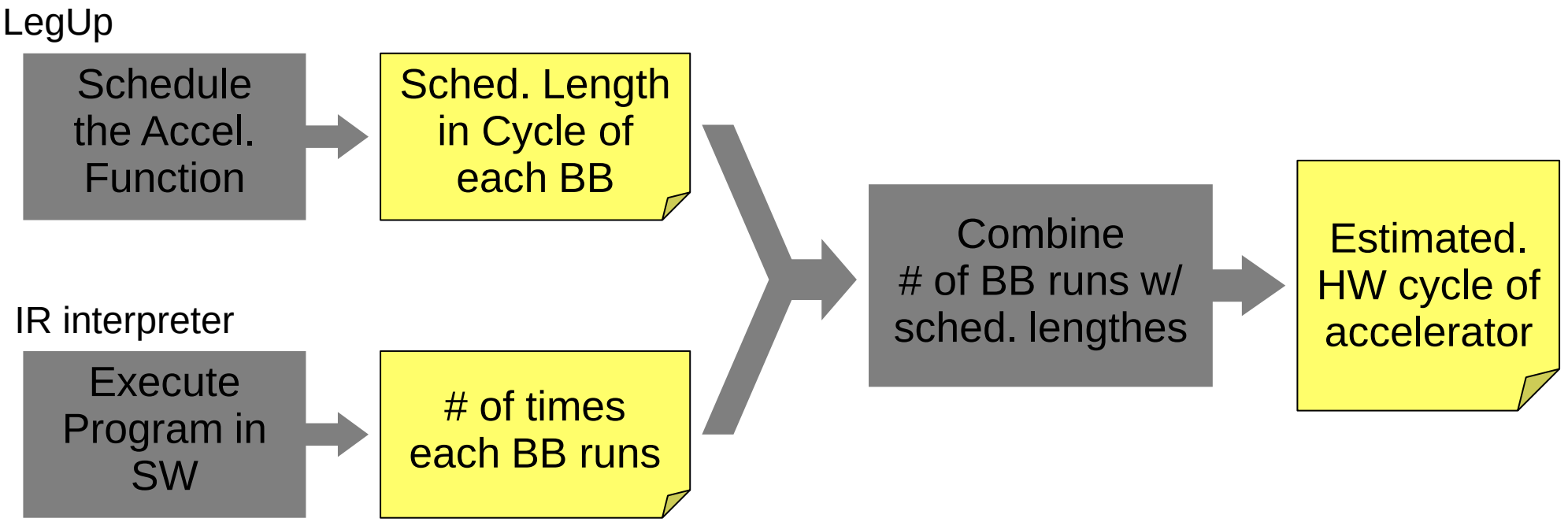
Component I - SW Wrapper

- Contribution to Total Tolerance
  - (actual cycle – estimated cycle) / actual hybrid cycle
  - Average: 3.01%
  - StdDev: 4.04%
- *Note: Total Tolerance =*

  (actual hybrid cycle – predicted hybrid cycle) / actual hybrid cycle

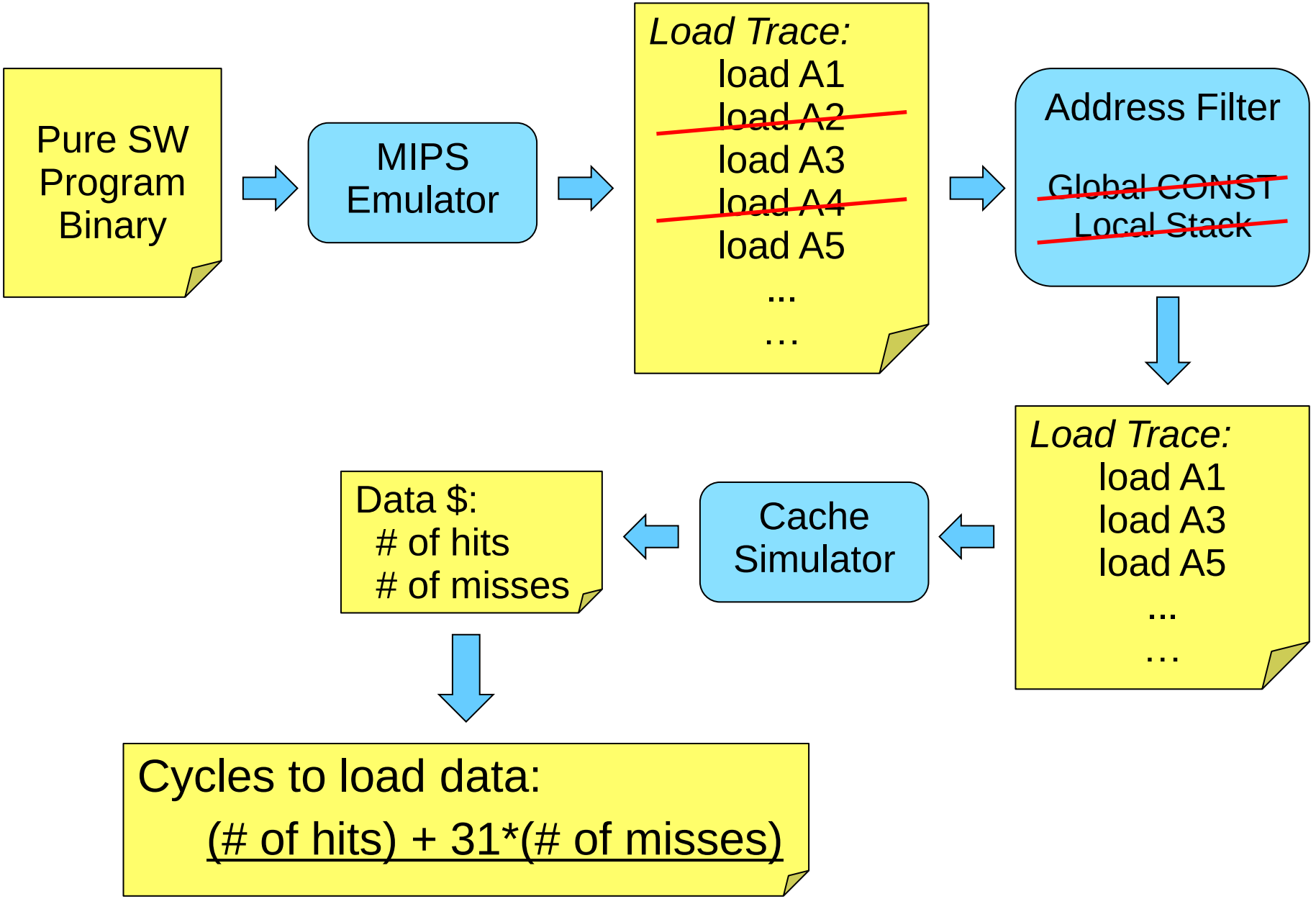


Component II – HW Cycle



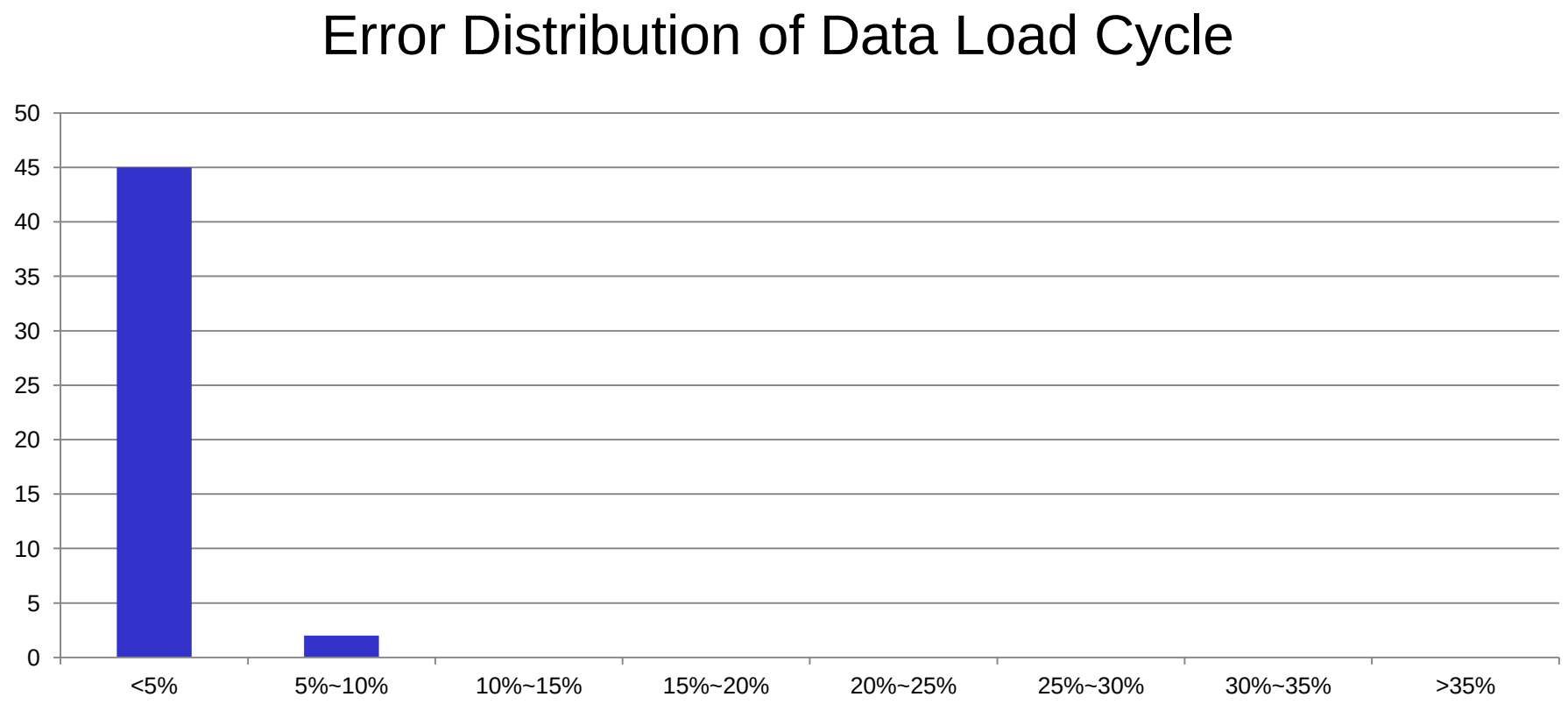
- ∑ foreach BB (sched. length) * (# of runs)
- Accurate if no mem. access
- Contribution to Total Tolerance
  - Average: 0.02%
  - StdDev: 0.16%
- *Note: 1 of 47 tests contributes 1.09% tolerance; all other 46 tests: 0%*

Component III – Data Loads



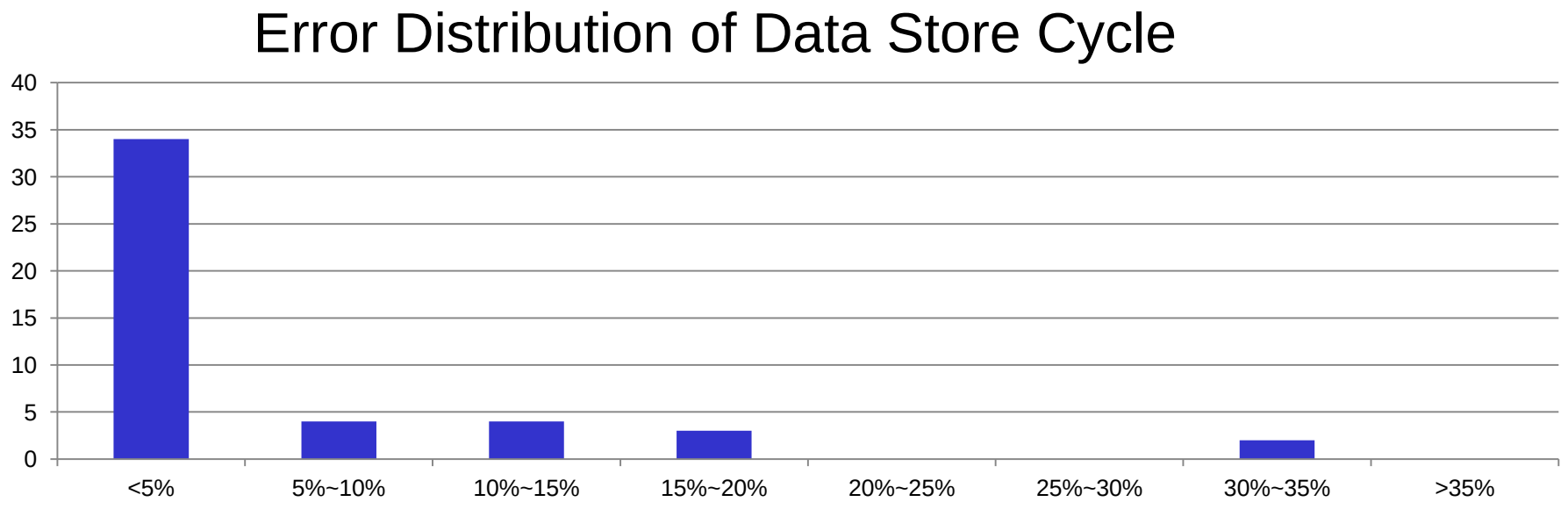
Component III – Data Loads

- Contribution to Total Tolerance
  - Average: 0.97%
  - StdDev: 1.73%



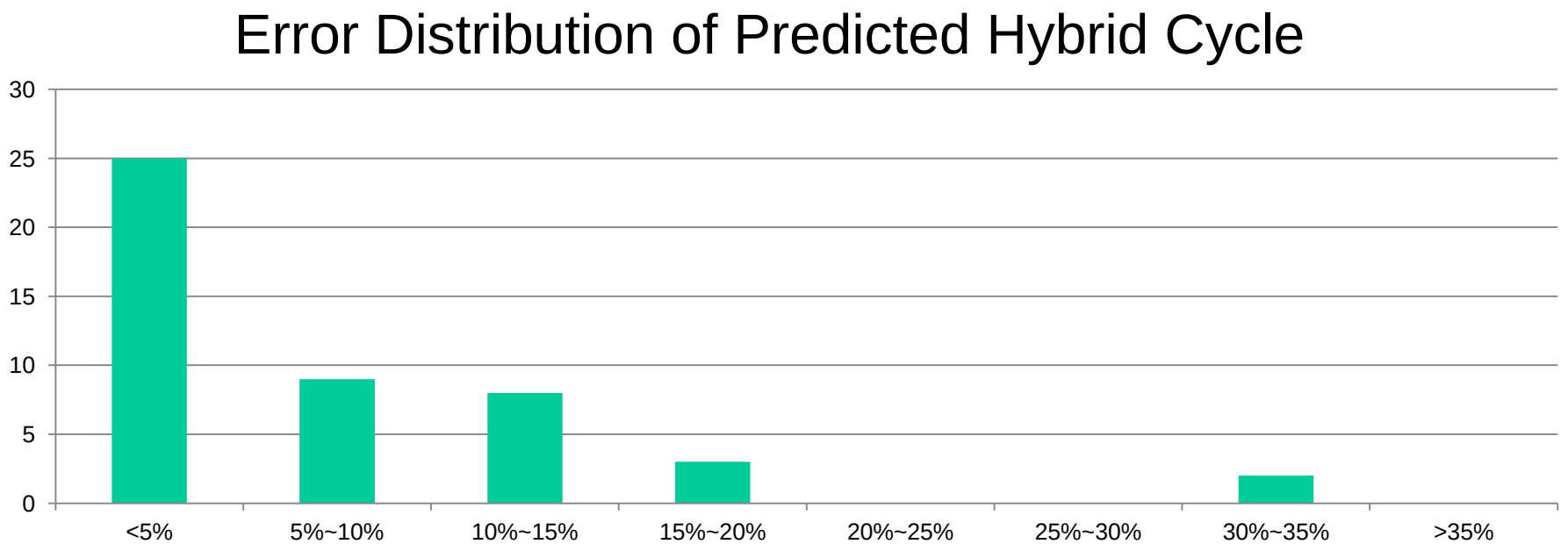
Component IV – Data Stores

- Similar Methodology as Data Loads
  - Generate address trace in the same way as Data Loads
  - Write-through policy of data cache
  - 1.85*(# of stores)
- Contribution to Total Tolerance
  - Average: 5.35%
  - StdDev: 7.86%
  - Most Inaccurate – “Key Contributor” to total tolerance



Final Result – Predicted Hybrid Cycle

- Sum of
  - SW Wrapper Cycle
  - HW Cycle
  - Data Load Cycle
  - Data Store Cycle
- Average: 7.21%
- StdDev: 7.79%



“Key Contributor” to Tolerance – Data Store Cycle

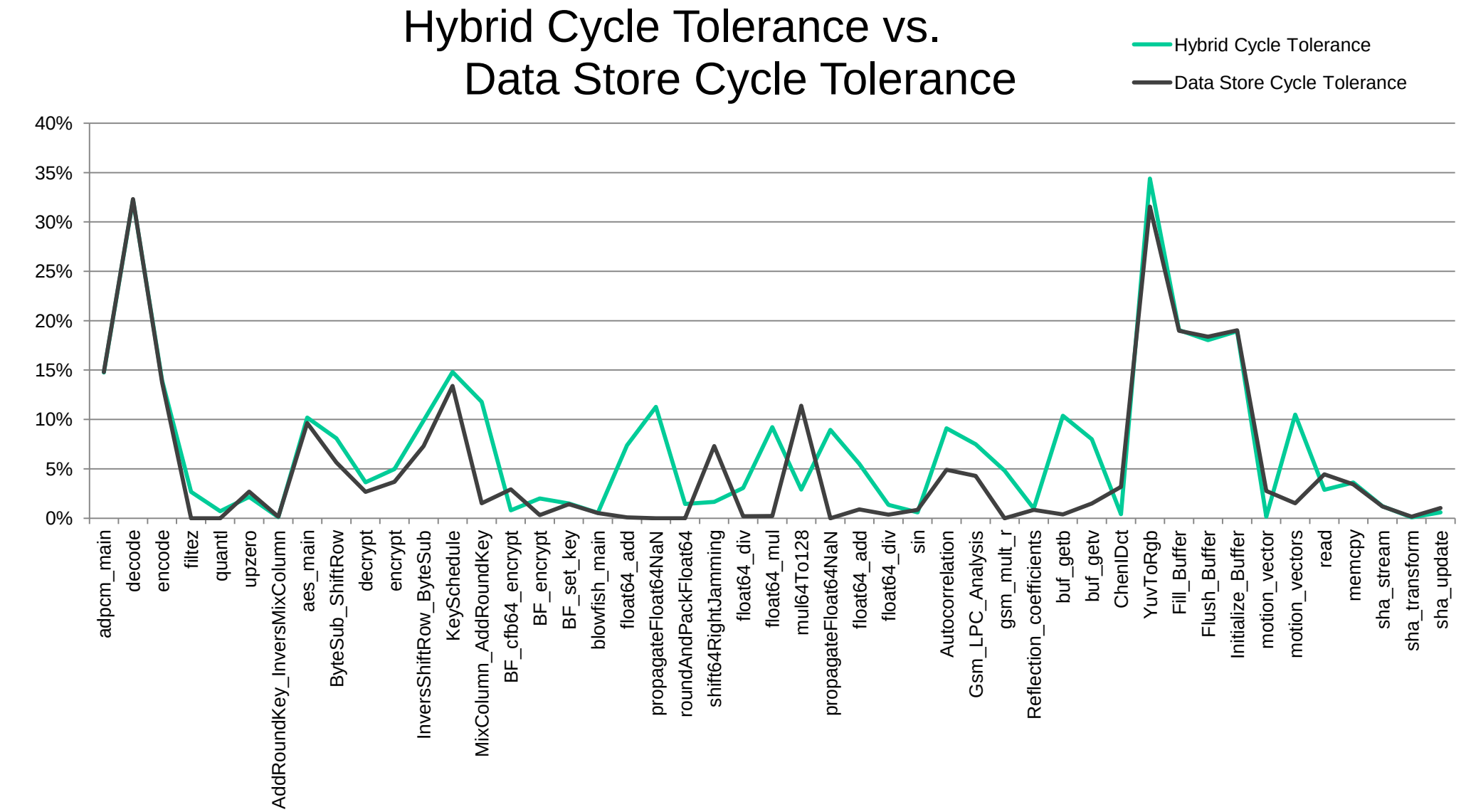
- The only 2 tests that have tolerance greater 20%
- Data Store Cycle = 1.85 * (# of stores)

	Function A	Function B
Hybrid Cycle Tolerance	32.26%	34.39%
Tolerance Contributed by Data Store Cycle	32.32%	31.56%
Estimated # of Stores	4000	18432
Actual # of Stores	4100	18624
Estimated Store Cycles	7400	34099
Actual Store Cycles	22445	110524
Varying Coefficient	5.47	5.93

- Open-Row architecture in the SDRAM on DE-II
  - ~1 cycle to store data in currently open row
  - A lot more cycles to store data in a different row

“Key Contributor” to Tolerance – Data Store Cycle

- Most of the tolerances come from data store cycle estimation



THANK YOU !