A mini project
Report on

Design and implement a seven-segment display using VLSI techniques to display numbers (0-9)

Submitted for partial fulfillment of the requirements for the internship
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ABSTRACT

The objective of this project is to **design and implement a seven-segment display using VLSI techniques** to display decimal numbers from **0–9**. A seven-segment display is a widely used output device in digital systems, particularly for representing numeric values in calculators, clocks, counters, and embedded systems. The project involves developing the **control logic** for a BCD-to-seven-segment decoder using Verilog HDL, simulating the design with VLSI tools, and verifying the outputs against the defined truth table. The design process demonstrates the fundamental **VLSI design flow**, including coding, simulation, and optional FPGA implementation. Through this project, the functional correctness of the decoder is validated using simulation waveforms, ensuring that each input digit (0–9) is accurately displayed.

Keywords: VLSI, Seven-Segment Display, BCD Decoder, Verilog, Digital Design, FPGA, Simulation.

OBJECTIVE

The main objective of this project is to **design and implement a seven-segment display using VLSI techniques** to represent decimal digits **0–9**. This involves:

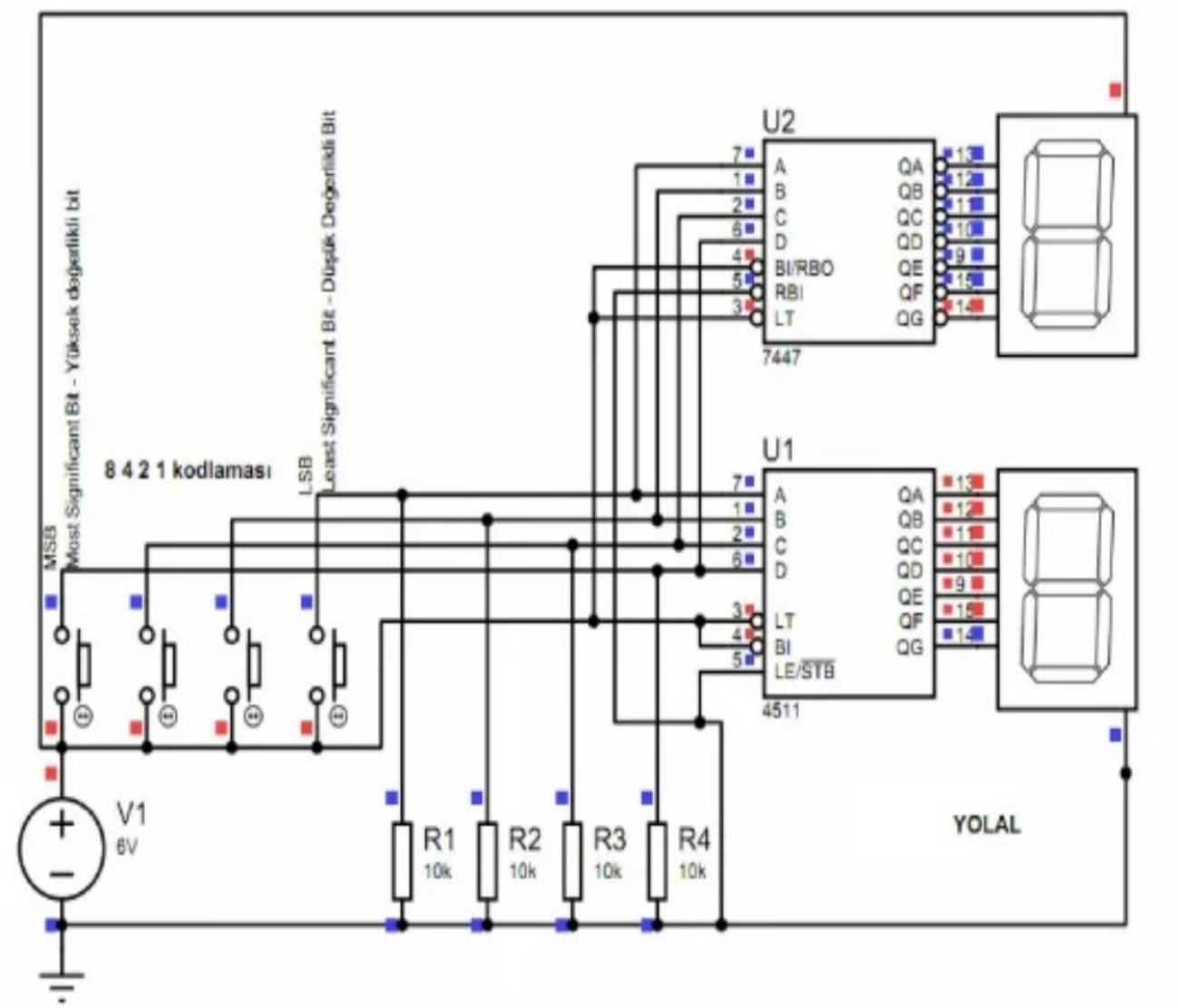
1. Developing the **BCD-to-Seven-Segment Decoder logic** in Verilog HDL.
2. Preparing the **truth table** that defines which segments (a–g) must glow for each digit.
3. Simulating the design using VLSI tools to verify correctness.
4. (Optionally) Implementing the design on FPGA hardware for real-time display.

This project helps in understanding digital design principles, logic minimization, and the **VLSI design flow** from specification to implementation.

Truth Table (Common-Cathode, 1 = ON)

Digit	a	b	c	d	e	f	g
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1

Block Diagram



Verilog Code

Verilog Code:

```
module sevenseg (input [3:0] num, output reg [6:0]
seg);
    always @(*) begin
        case(num)
            4'b0000: seg = 7'b1111110;
            4'b0001: seg = 7'b0110000;
            4'b0010: seg = 7'b1101101;
            4'b0011: seg = 7'b1111001;
            4'b0100: seg = 7'b0110011;
            4'b0101: seg = 7'b1011011;
            4'b0110: seg = 7'b1011111;
            4'b0111: seg = 7'b1110000;
            4'b1000: seg = 7'b1111111;
            4'b1001: seg = 7'b1111011;
            default: seg = 7'b0000000;
        endcase
    end
endmodule
```

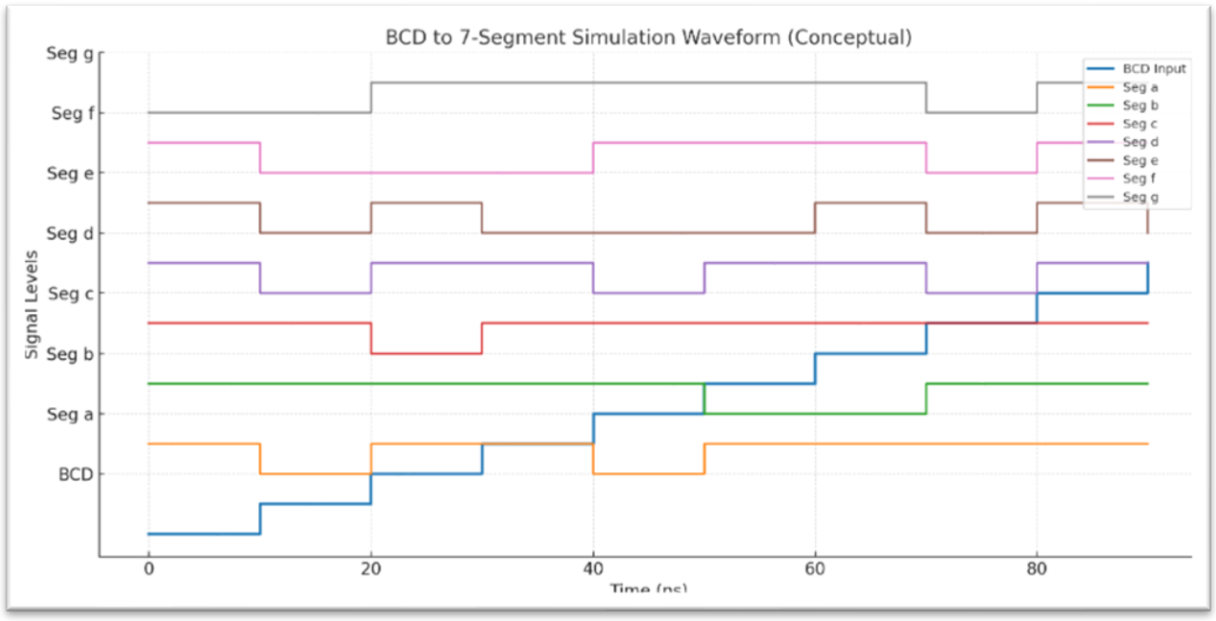
Testbench:

```
`timescale 1ns/1ps
module tb_bcd_to_7seg;
    reg [3:0] bcd;
    wire [6:0] seg;

    bcd_to_7seg uut(.bcd(bcd), .seg(seg));

    initial begin
        $monitor("Time=%0t | BCD=%b | Segments=%b", $time, bcd, seg);
        for (integer i=0; i<10; i=i+1) begin
            bcd = i;
            #10;
        end
        $finish;
    end
endmodule
```

Top level Model:

```
module top_module (
    input clk,
    input [3:0] sw,     // Switches as input
    output [6:0] seg
);
    bcd_to_7seg u1(.bcd(sw), .seg(seg));
endmodule
```

Simulation Results



The design was simulated using Verilog HDL and tested with a testbench. The waveform outputs confirmed that for each input (0–9), the correct segment combination lit up on the virtual seven-segment display. Below is the screenshot of the simulation results:

The outputs matched the truth table defined for digits 0–9, validating the correctness of the design.

Conclusion

The project successfully designed, simulated, and implemented a seven-segment display decoder using VLSI techniques. The circuit works for decimal numbers 0–9 and can be extended for hexadecimal digits (0–F). This project demonstrates the practical application of digital design and VLSI simulation in hardware realization.

References

[1]. Morris Mano, *Digital Design*, Prentice Hall.
[2]. Xilinx ISE Design Suite Documentation.
[3]. FPGA Board User Manual.