3x8 Decoder:

Source code:-

```verilog
1   module dc_3x8(
2   input [2:0] i,
3   output [7:0] y
4   );
5
6   assign y[0] = ~i[0] & ~i[1] & ~i[2];
7   assign y[1] =  i[0] & ~i[1] & ~i[2];
8   assign y[2] = ~i[0] &  i[1] & ~i[2];
9   assign y[3] =  i[0] &  i[1] & ~i[2];
10  assign y[4] = ~i[0] & ~i[1] &  i[2];
11  assign y[5] =  i[0] & ~i[1] &  i[2];
12  assign y[6] = ~i[0] &  i[1] &  i[2];
13  assign y[7] =  i[0] &  i[1] &  i[2];
14
15  endmodule
```

Testbench:-

```verilog
1 `timescale 1ns/1ps
2 `include "dc_3x8.v"
3
4 module tb_dc3x8;
5
6 reg [2:0] i;
7 wire [7:0] y;
8
9 dc_3x8 DUT(
10 .i(i),
11 .y(y)
12 );
13
14 initial begin
15     $dumpfile("dc3x8.vcd");
16     $dumpvars(0,tb_dc3x8);
17 end
18
19 initial begin
20     $monitor("Time=%g i=%b | y=%b",$time,i,y);
21         i=3'b000; #10;
22         i=3'b001; #10;
23         i=3'b010; #10;
24         i=3'b011; #10;
25         i=3'b100; #10;
26         i=3'b101; #10;
27         i=3'b110; #10;
28         i=3'b111; #10;
29     $finish;
30 end
31 endmodule
```
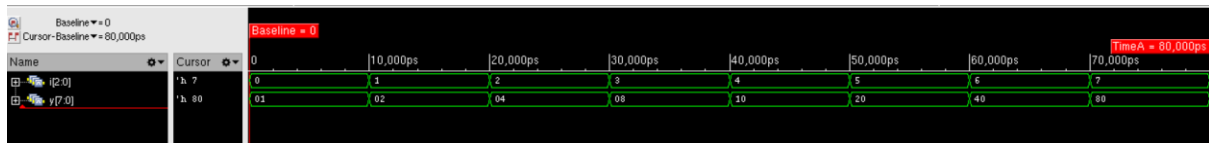
Output:-

```
Time=0 i=000 | y=00000001
Time=10 i=001 | y=00000010
Time=20 i=010 | y=00000100
Time=30 i=011 | y=00001000
Time=40 i=100 | y=00010000
Time=50 i=101 | y=00100000
Time=60 i=110 | y=01000000
Time=70 i=111 | y=10000000
Simulation complete via $finish(1) at time 80 NS + 0
./tb_dc3x8.sv:29        $finish;
```

Waveform:

Schematic:-