merge sort is an example of divide sommer appropries Each having one Element divided into N sublist, A list of one Element is considered sorted to Poroduce sorted list. 17/24 Merge sont

one: Explain the Parallel sorting Algorithm Bubble and Merge sort? Bent the American According on - Bubble apport: in Descending order - compare Adjucent Element - In Every Passo largest the got their Actual Poss and the is not consider in the 95 UU 55 44 11 22 33 44 55 sosted Array are 1122 33 4455

6. HPC Applications one: write wheat note on Parallel De Explain BFG (DFG in Detail. (6-5) 355 ODPS estands for Day QBES stands for Breadth First sourth First Search @ DES USE STACK @BFG USE QUELLE Data structure Data astructure 3 Also known as FIROSOND. 3 Also known as LIFO Select @ DRG maversing Data (BFG search levelvise Root Node to Crowl Node in a tree or Graph. (5) Ex: (Eral G D Application: @ Apolication: - Finding shorted Path - Peer - to-Peer Nu - Chess Example: Example: Destep 1: enterd: 3 visited []] Q 3 visited 1 (anene initially actack & vival mitially queuegvisited Armay arry are emply are empty.

@ Jaunch Coda Kemal: - Launch CUDA Remal by host Bennal monece Arid, block >>> Cargument list goids contains po of Blocks. I and this blocks contains po of threads Croido

sue: Explain the procedure to write 3.

launch a CUDA Remal?

- CUDA Remal la a Function. Dwrite CODA hermal: gobal void remal som clargument lists - hoost -- devicereturn type is void. and write parameters. It kernaling - we can also use host & device - If the particular function is consider as device then use device If the use sehest then hemal Acress only host Memory. -No support static var & ptr.

Application PA of PA Paralle I 3 Desice GPU Device [313] [318] application code contains set of lines. I here can be executed in sequential spanales segmential Part Executed in CPU & Parallel Part executed in GPU In CODA CIC++ Application Randomly Executed in sequential code and Parallel code. sequential code Executed in Host ensalled code Executed in Device perice contain no. of blocks. contain no of threads blocks created Parallel code. Those Ad

Logical Unit: Anthonetic operations operations ALU DRAIT store infort in Longer DRAM is slower DRAM -cache: - store rempleany Data QUE Explain in detail CUDA Programming in QUDAstands for compute Unitred Architecture Device - CUDA is a Library (Parkage) develop by Nvidea. works with clott language - CUDA is passelled computing Platen -CUDA

que what is cuda? / cuda c?

- cuda sotandes for compute Unified - CUDA is a library (Package)

develop by Nvidea. - CUDA works with elett language. - CUDA is Parallel Computing Platform Architecture: CUT AW PLU Pul CPU Cache CUDA Libraries CUDA Drivers CXPU ALU AU AU ALU ALU ALL ALL 1- - CPU stands for central Proce Unit - CPU required More Memory than PU is slower than GPU - CPU Not suitable for Parallel Instruction computing. CPU contains work librarius, CU

cu:- cu costando for controlling. - ALU estando for Anithmeticas logical operations.

Load the data into ALU. : - DRAM sotore inform in Lo -DRAM - DRAM is solower. : - estore Temperary Data. -cache

CPU -- CPU estands for central Processing

- CPU required More Memory than CPU

- CPU Not suitable for Parallel compute

Instruction Computing.

- CPU contains CUDA Libraries, CUDA Driber

- In CPU There Rese several Parts:

- CPU is Most - mall data size.

5. CUDA Architecture ene: what is app Architecture explain in - GPU stands for Graphical Processing Unit - apu required less Menopry than con CEPU & Faster than CPU (central Pr Dirit) GPU souitable for Parallel Instruction Processing. - app to Device - Huge Appoint of Data. Control ALU ALU ALU Cache Central ALV ALV ALV carne Control Cathe control cache W: + ALU stands for Arithmetic Logical Unit - ALU Perform Arithmetic Operations, miles companieson opens, logical operations. - Lord the data into ALU. AM ! store information in Longer Time DRAM DRAM is slower her: - ostore Temperary Data