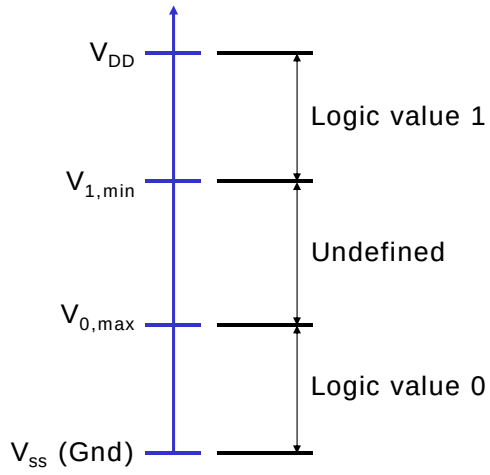
ECE380 Digital Logic

Implementation Technology:

NMOS and PMOS Transistors,
CMOS logic gates

Logic values as voltage levels

- V_{ss} is the minimum voltage that can exist in the system. We will use V_{ss}=0V.
- V_{DD} is the power supply voltage. We will use V_{DD} =+5V. V_{DD} =+3.3V is also common.
- Exact levels of $V_{0,max}$ and $V_{1,min}$ depend on the implementation technology

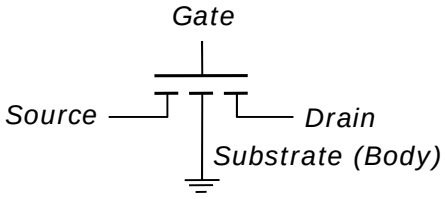


Transistor switches

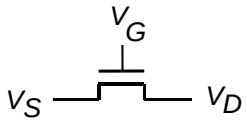
- Logic circuits are built with transistors
- We will assume a transistor operates as a simple switch controlled by a logic signal x
- The most popular type of transistor for implementing a simple switch is the ***metal oxide semiconductor field effect transistor*** (MOSFET)
- Two types of MOSFETs
  - N-channel (***NMOS***)
  - P-channel (***PMOS***)
- Early circuits relied on NMOS or PMOS transistors, but not both
- Current circuits use both NMOS and PMOS transistors in a configuration called ***complementary MOS*** (CMOS)

NMOS transistor as a switch

A simple switch controlled by the input x

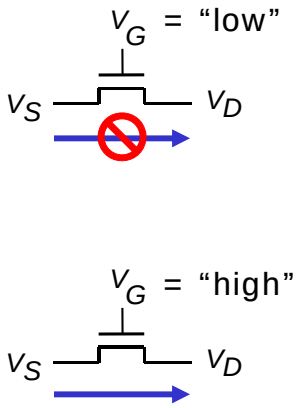


NMOS transistor



Simplified NMOS symbol

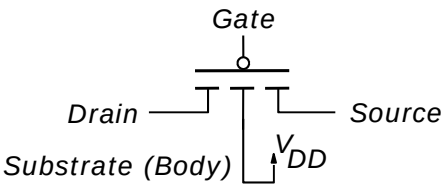
NMOS transistor as a switch



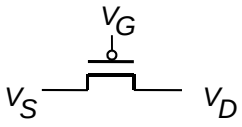
- The transistor operates by controlling the voltage V_G at the gate terminal
- If V_G is low, there is no connection between the source and the drain terminals. The transistor is ***turned off***.
- If V_G is high, the transistor is ***turned on*** and acts as a closed switch between the source and drain terminals.

PMOS transistor as a switch

A simple switch controlled by the input x

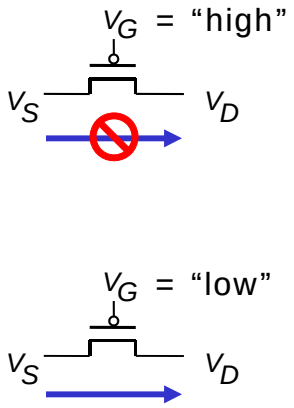


PMOS transistor



Simplified PMOS symbol

PMOS transistor as a switch



- The transistor operates by controlling the voltage V_G at the gate terminal
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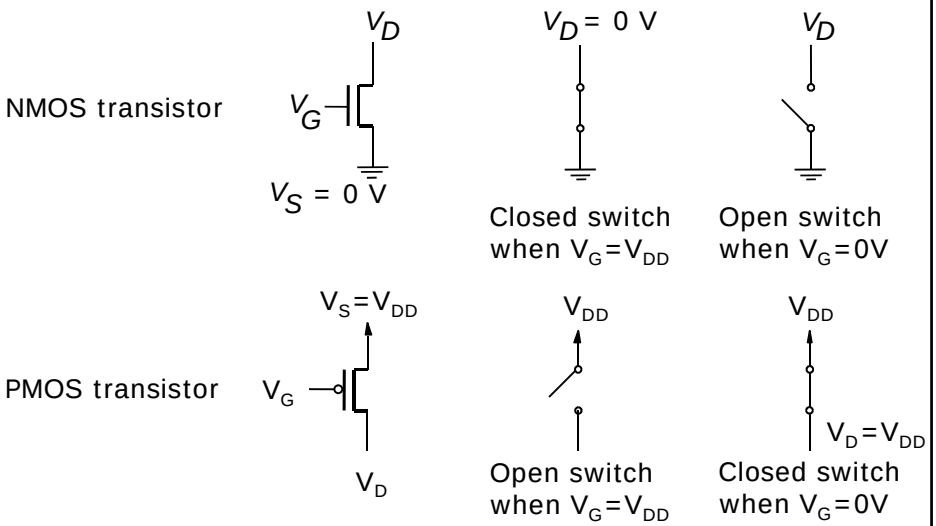
NMOS and PMOS in logic circuits



NMOS and PMOS in logic circuits

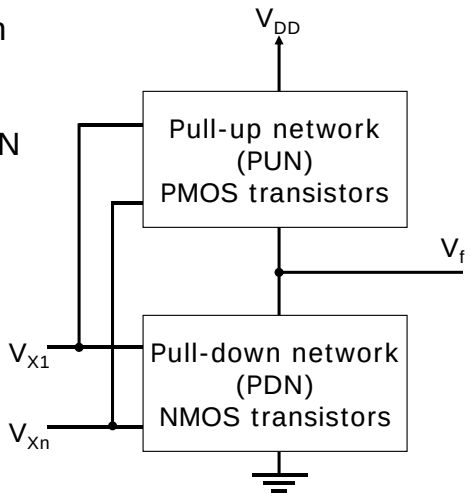
- When the NMOS transistor is turned on, its drain is ***pulled down to Gnd***
- When the PMOS transistor is turned on, its drain is ***pulled up to V_{DD}***
- Because of the way transistors operate:
  - An NMOS transistor cannot be used to pull its drain terminal completely up to V_{DD}
  - A PMOS transistor cannot be used to pull its drain terminal completely down to Gnd
- Therefore, NMOS and PMOS transistors are commonly used in pairs in CMOS circuits

CMOS logic gates

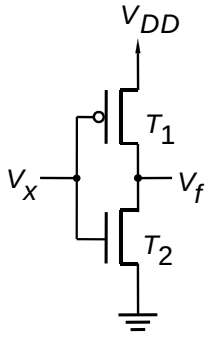
- A CMOS logic gate involves NMOS transistors in a ***pull-down network*** (PDN) and PMOS transistors in a ***pull-up network*** (PUN)
- The functions realized by the PDN and PUN networks are complements of one another
- The PDN and PUN have equal numbers of transistors, which are arranged so that the two networks are duals of one another
  - Wherever the PDN has NMOS transistors in series, the PUN has PMOS transistors in parallel, and vice versa

CMOS logic gates

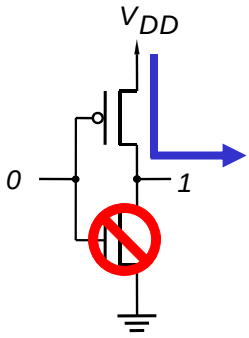
- For any given valuation of the input signals, either the PDN pulls V_f down to Gnd or the PUN pulls V_f up to V_{DD}

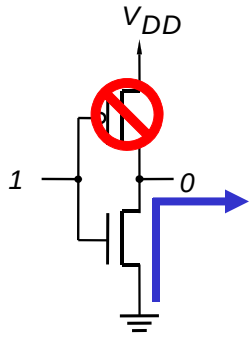


CMOS NOT gate



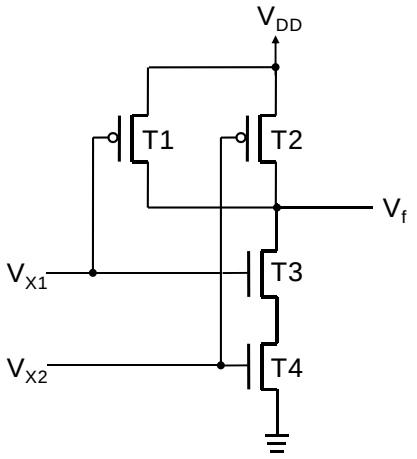
x	T1	T2	f
0	On	Off	1
1	Off	On	0





2 transistors

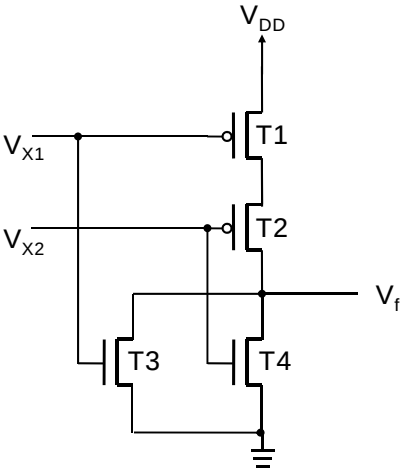
CMOS NAND gate



X1	X2	T1	T2	T3	T4	f
0	0	On	On	Off	Off	1
0	1	On	Off	Off	On	1
1	0	Off	On	On	Off	1
1	1	Off	Off	On	On	0

4 transistors

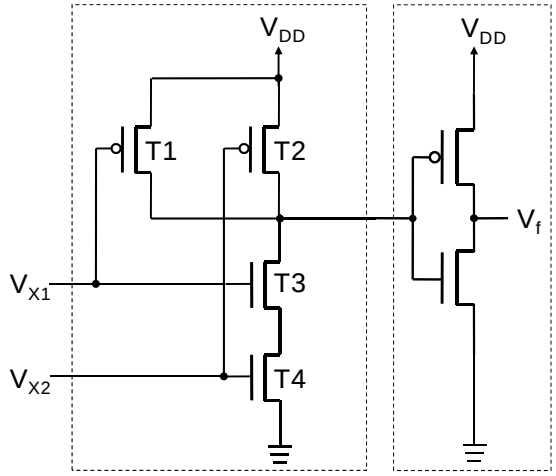
CMOS NOR gate



X1	X2	T1	T2	T3	T4	f
0	0	On	On	Off	Off	1
0	1	On	Off	Off	On	0
1	0	Off	On	On	Off	0
1	1	Off	Off	On	On	0

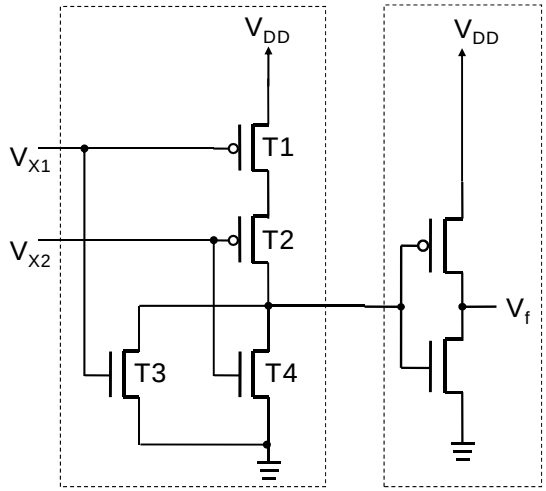
4 transistors

CMOS AND gate



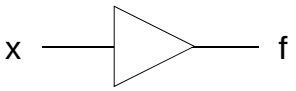
6 transistors

CMOS OR gate



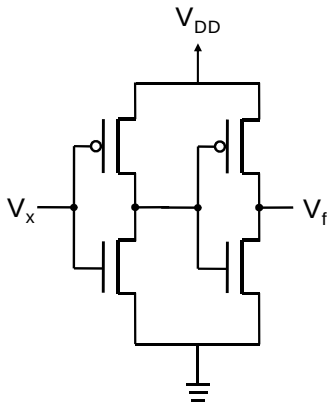
6 transistors

CMOS non-inverting buffer



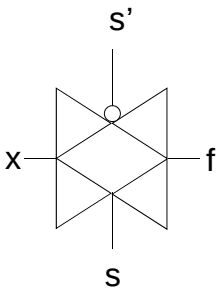
f=x

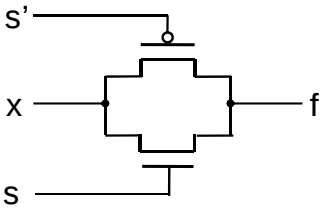
A non-inverting buffer



4 transistors

CMOS transmission gate

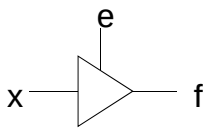




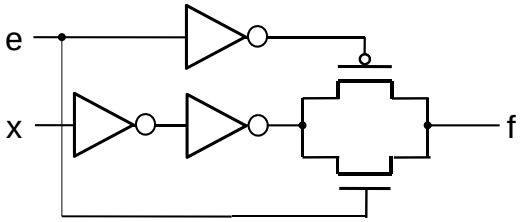
s	*f*
0	Z
1	x

2 transistors

CMOS tri-state buffer



e	*x*	*f*
0	0	Z
0	1	Z
1	0	0
1	1	1



8 transistors