ID1330 : Applied Digital Logic Design Experiment

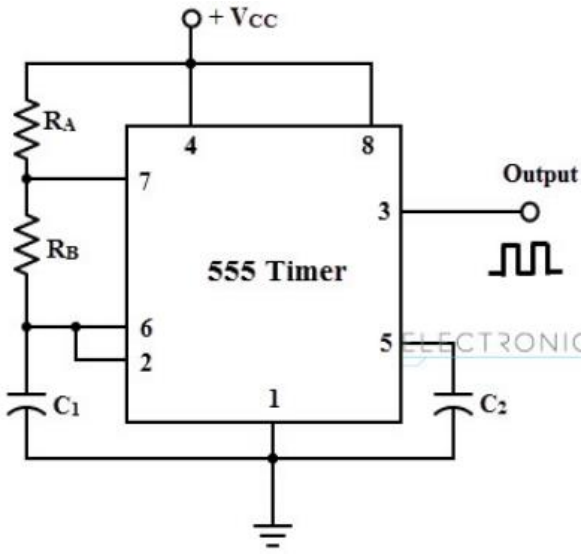
1. Design a clock divider circuit which provides input to a shift register and display the output on the oscilloscope.
2. Design a 4 bit adder circuit which takes inputs from the shift register and displays the output on a 7 segment display.
3. Design a complete system integrating the clock divider circuit along with the adder circuit and display the output on a 7 segment display.

List of equipments

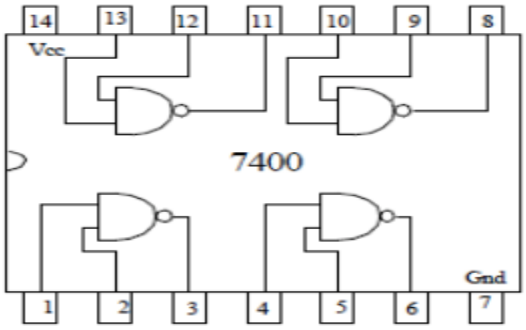
1. IC 7400 – 2 input NAND Gate
2. IC 7486 – 2 input XOR Gate
3. IC 7447 – Decoder
4. IC 7474 – D Flipflop
5. IC 74x194 – 4 bit bidirectional universal shift register
6. IC 7483 - 4 bit parallel Adder
7. 555 Timer
8. Common Anode 7 segment Display
9. Resistors, Capacitors
10. Bread Board
11. DC power supply
12. Oscilloscope

Pin Diagram of Basic ICs

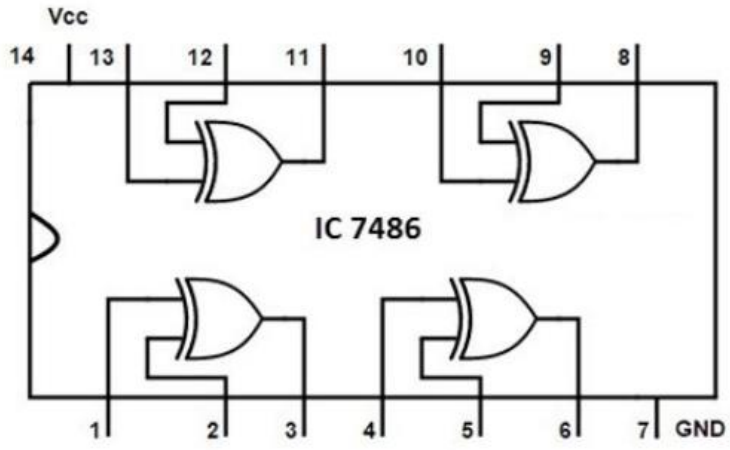
1. 555 Timer



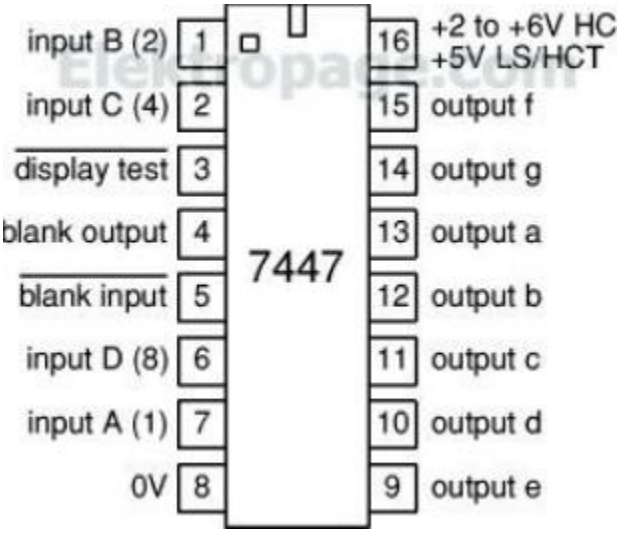
2. IC 7400 2-input NAND Gate



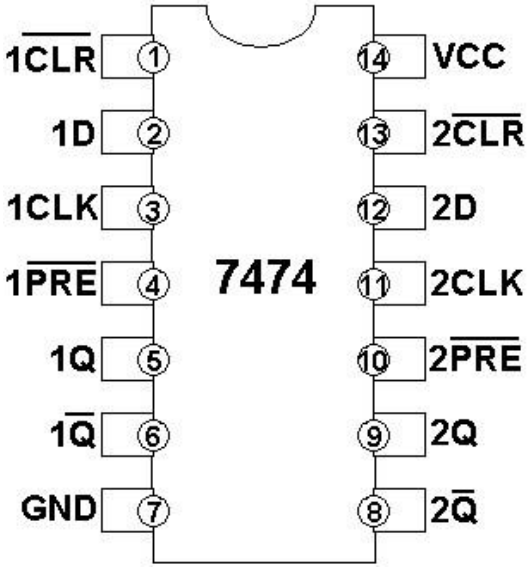
3. IC 7486 2-input XOR Gate



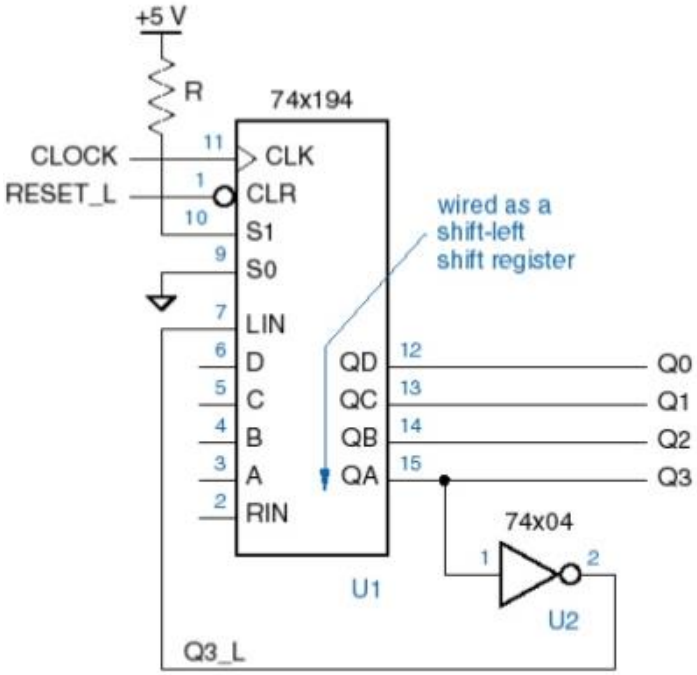
4. IC 7447 Decoder



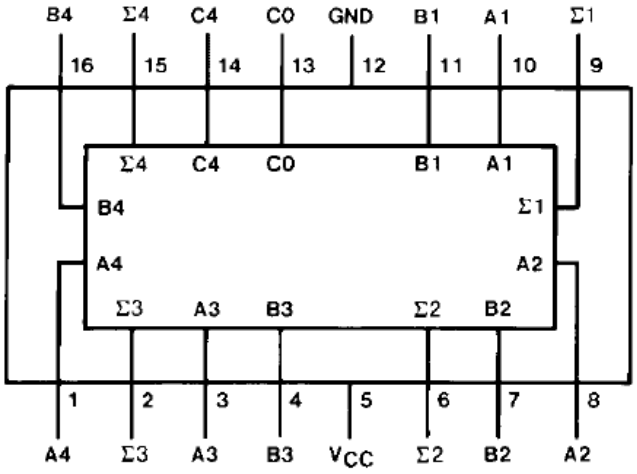
4. IC 7474 – D Flipflop



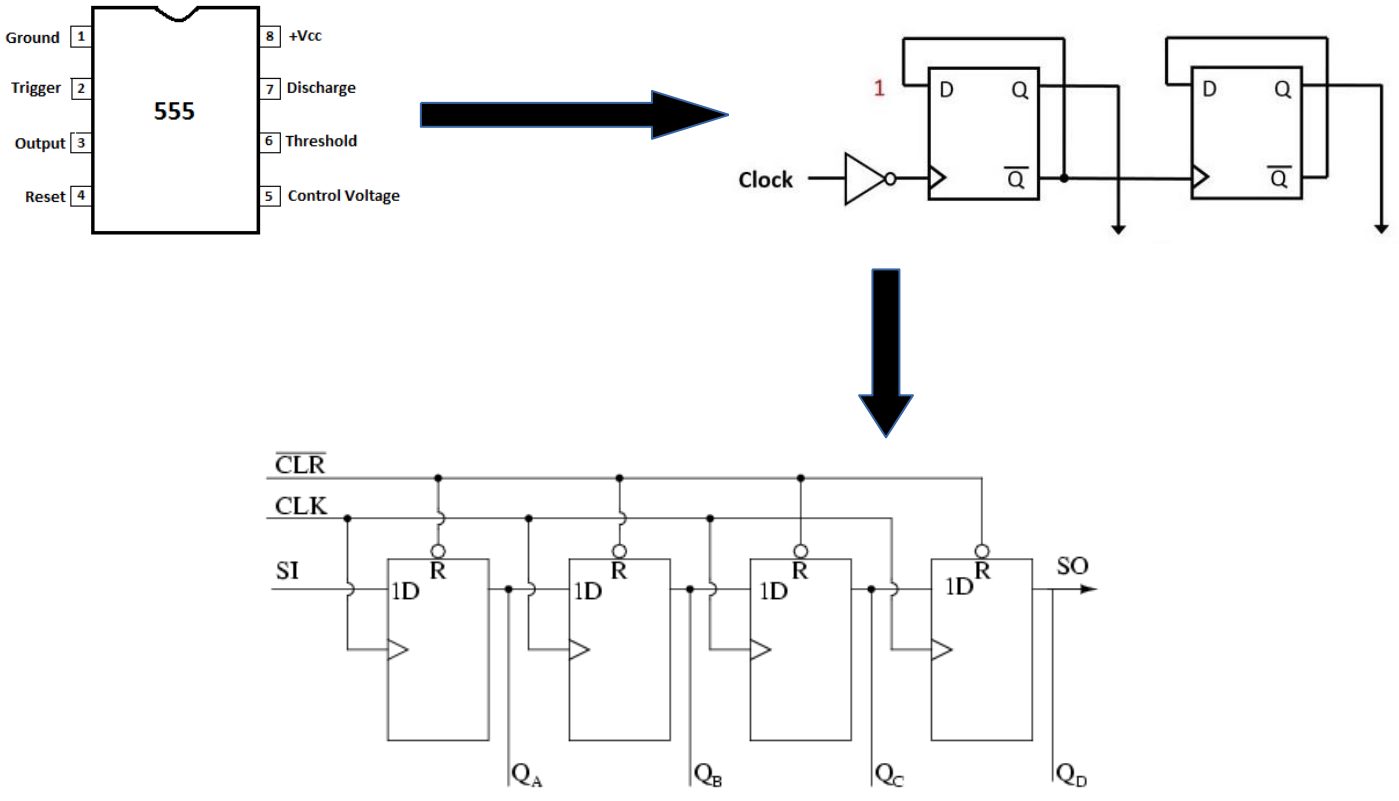
5. IC 74x194 – Shift Register



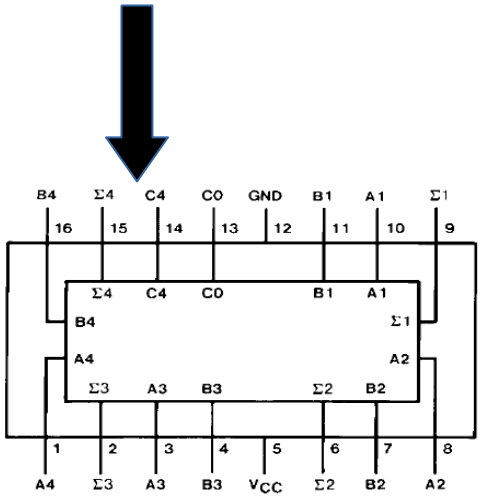
6. IC 7483 – 4 bit Adder

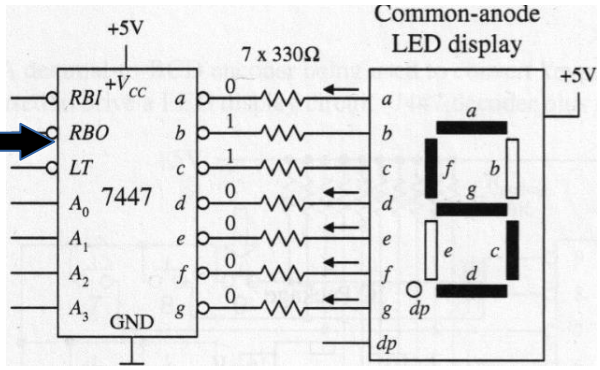


Circuit Diagram



Serial-in/ Parallel out shift register details


B4 Σ4 C4 C0 GND B1 A1 Σ1
16 15 14 13 12 11 10 9
Σ4 C4 C0 B1 A1
B4 Σ1
A4 A2
Σ3 A3 B3 Σ2 B2
1 2 3 4 5 6 7 8
A4 Σ3 A3 B3 VCC Σ2 B2 A2


+5V
7 x 330Ω
Common-anode
LED display
+5V
RBI
RBO
LT
A0
A1
A2
A3
7447
+Vcc
GND
a
b
c
d
e
f
g
dp
0
1
1
0
0
0
0