ID1330: Applied digital logic design

Exam set: 3 : Marks: 20

1. (i) Write the name of the flip-flops for fig (a) and fig(b)

flip-flop

A	B	Q	Q+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	-
1	1	1	-

fig:(a)

flip-flop

A	B	Q	Q+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

fig:(b)

(ii) Use k-maps to solve fig (a) and fig (b) and draw the circuit

(iii) What will be output of the following circuits, Fig (c) and (d)?

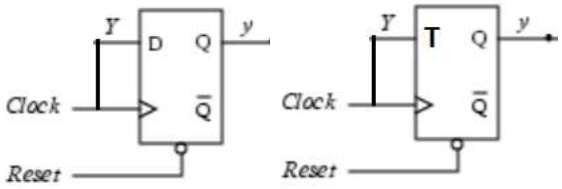
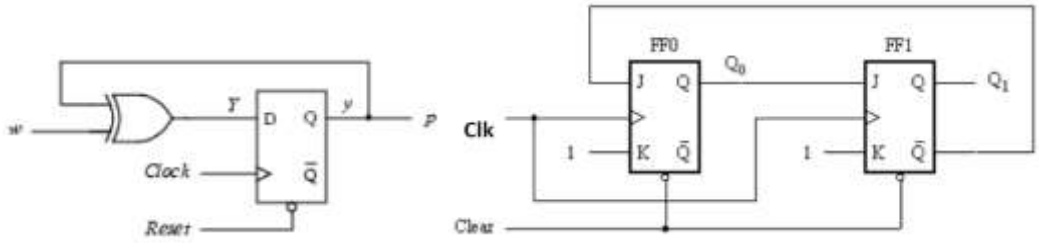


Fig (c) Fig (d)

2. (i) Design a flip-flop based simple circuit, (a) which will generate a signal that is the divide the clock signal by 2 and (b) which will generate a signal that is the multiply the clock signal by 2.

(ii) Derive the state (truth) transition table of the following circuits (if you have consider previous state is also an input, initial states p=0 & Q_0 =0 and Q_1 =0)



(iii) Derive the state table and state equation of following circuit ?