Applied Digital Logic Design

BOOLEAN LAWS

T1 : Commutative Law

(a) $A + B = B + A$

(b) $A\,B = B\,A$

T2 : Associative Law

(a) $(A + B) + C = A + (B + C)$

(b) $(A\,B)\,C = A\,(B\,C)$

T3 : Distributive Law

(a) $A\,(B + C) = A\,B + A\,C$

(b) $A + (B\,C) = (A + B)\,(A + C)$

T4 : Identity Law

(a) $A + A = A$

(b) $A\,A = A$

T5 : Negation Law

(a) $\overline{(\overline{A})} = \overline{A}$

(b) $\overline{(\overline{A})} = A$

T6 : Redundancy Law

(a) $A + A\,B = A$

(b) $A\,(A + B) = A$

T7 :

(a) $0 + A = A$

(b) $1\,A = A$

(c) $1 + A = 1$

(d) $0\,A = 0$

T8 :

(a) $\overline{A} + A = 1$

(b) $\overline{A}\,A = 0$

T9 :

(a) $A + \overline{A}\,B = A + B$

(b) $A\,(\overline{A} + B) = A\,B$

T10 : De Morgan's Theorem

(a) $\overline{(A + B)} = \overline{A}\ \overline{B}$

(b) $\overline{(A\,B)} = \overline{A} + \overline{B}$

UNIVERSIAL LOGIC GATES : SIGNOFICNCE

Normal	Universal	Additional
NOT	NAND	XOR
AND	NOR	XNOR
OR		

- **NOT : 2 transistors (PMOS top and NMOS bottom)**

(R-C circuit) at Input "0": PMOS ON, charge "C" i.e. output to "1", at Input "1": NMOS ON, discharge "C" i.e. output to "0",

- **Input-output transfer characteristics**

Output delay with input: speed limitation

- **OR : realization with NAND or NOR**

Area: NOR < NAND

Dynamic Power: NOR < NAND

Delay (Speed): NAND>NOR

TARGET:

- **Area & Power Minimization**
- **Speed Maximization**
- **Logic optimization (No of gate minimization**

- NOT/AND /OR : realization with NAND or NOR : Universal
- NOT, NAND and NOR: CMOS realization with help of **De Morgan's Theorem**
- Example : NAND($\overleftrightarrow{A.B}$)~ $\overleftrightarrow{A}$.+$\overleftrightarrow{B}$: ***4 transistors***

NMOS section (Bottom) = A.B

PMOS section (Top) = $\overleftrightarrow{A}$.+$\overleftrightarrow{B}$

NOR($\overleftrightarrow{A+B}$)~ $\overleftrightarrow{A}.\overleftrightarrow{B}$: ***4 transistors***

NMOS section (Bottom) = A+B

PMOS section (Top) = $\overleftrightarrow{A}.\overleftrightarrow{B}$

OR and AND: 6 transistors , 4 nos NOR/NAND and 2 nos NOT

- NAND & NOR: CMOS (PMOS mobility< NMOS Mobilty)

Area: Same

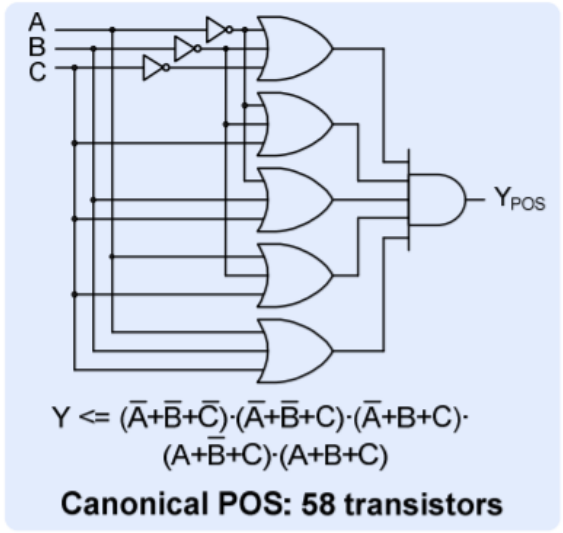
Dynamic Power: NOR < NAND

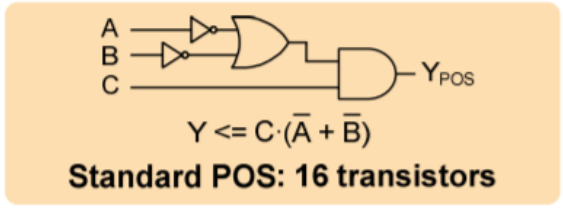
Delay (Speed): NAND>NOR

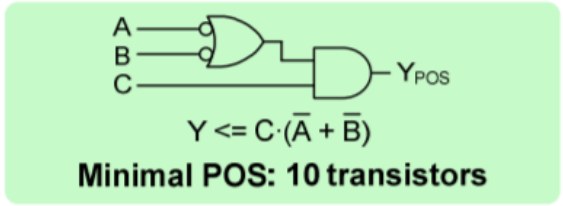
Function : Optimization and logic realization

$$Y = \overline{(A + \overline{B})(\overline{B + C})}$$

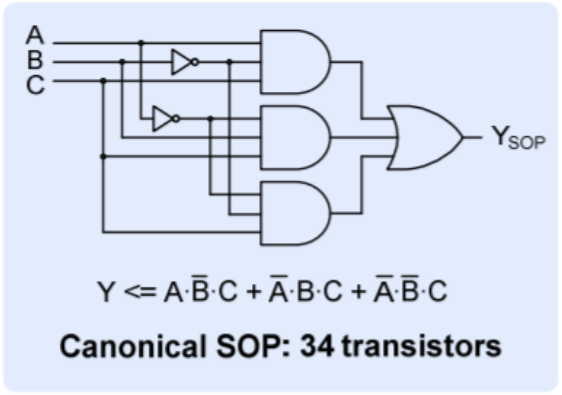
=A+C

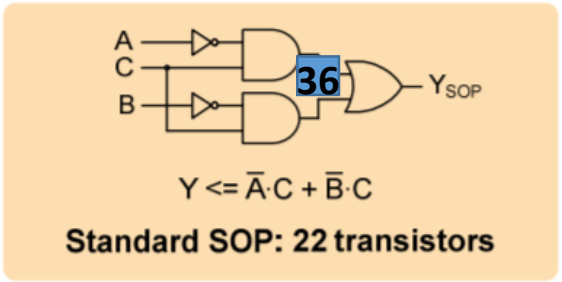


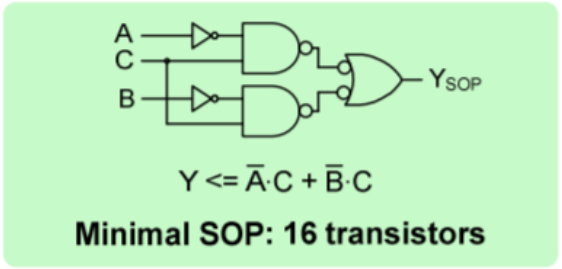




A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0







AND and Then OR (SOP), with “1”
OR and Then AND (POS) with “0”

K-maps rule

- Minimize Boolean expressions of 3, 4 variables very easily using K-map without using any Boolean algebra theorems.

- K-map can take two forms Sum of Product (SOP) and Product of Sum (POS) according to the need of problem.

- K-map is table like representation but it gives more information than TRUTH TABLE. We fill grid of K-map with 0's and 1's then solve it by making groups.

- **Steps to solve expression using K-map-**
- Select K-map according to the number of variables.
- Identify minterms or maxterms as given in problem.
- For SOP put 1's in blocks of K-map respective to the minterms (0's elsewhere).
- For POS put 0's in blocks of K-map respective to the maxterms(1's elsewhere).
- Make rectangular groups containing total terms in power of two like 2,4,8 ..(except 1) and try to cover as many elements as you can in one group.
- From the groups made in step 5 find the product terms and sum them up for SOP form.

K-maps rule

- Few Link: http://www.ee.surrey.ac.uk/Projects/Labview/minimisation/karrules.html
- http://www.ee.ic.ac.uk/pcheung/teaching/ee1_digital/Lecture5-Karnaugh%20Map.pdf
- https://www.seas.upenn.edu/~cit595/cit595s10/lectures/kmap.pdf
- http://www.pitt.edu/~kmram/0132/lectures/karnaugh-maps.pdf

- Tutorial with solved question: TA send soon

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