ECE380: Digital Logic **Sample Exam 1**

The exam will be closed book and closed notes. The following questions are representative of the type of questions that will be on the exam. A sheet showing Boolean theorems will be provided. You will be allowed one information sheet (front side only) with any additional information you choose to put on it. Your name must be on this sheet and it must be turned in with the exam. No calculators will be allowed. There will be 15 problems on the exam: 10 multiple choice (similar to samples 1-5) and 5 written (similar to samples 6-12).

1. Rewrite the following function in SOP form.

   F(a,b,c,d,e)=(a+c')(a+d)(ab'c+e)

   a) a+ab'd+ae+c'de
   b) ab'c+ae+c'de, from 12b and 12a
   c) ab'c+ab'd+ae+c'
   d) a'bc+ae+c'de
   e) a+ae+c'de

2. Which of the following Boolean expressions are false?

   a) (x+y)(x+z)=x+yz, true from 12b
   b) (x+y)(x'+z)=x'y+xz, true by truth table (or K-map) comparison
   c) xy+x'=x'+y, true from 16a
   d) x+(y+z)=(x+y)+z, true from 11b
   e) none of the above

3. For the following Boolean expressions, which equalities are true?

   F1=wy'+w'x'y'+w'yz
   F2=wxy'+x'y'+w'yz
   F3=wy'+x'y'z'+w'x'z+w'y'z
   F4=w'xy'+wy+yz'

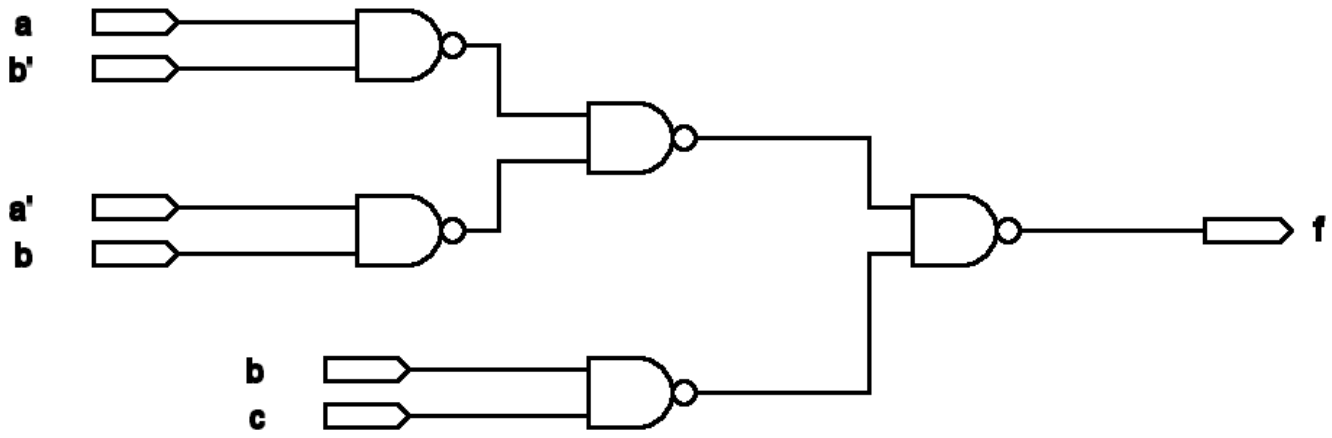
   a) F1=F2
   b) F1=F3 and F2=F4
   c) F1=F2=F3
   d) F3=F4
   e) none of the above

4. How many literals and variables does the following function have in this form?

   F=a'bc+a'bcd+c'd'

   a) 4 literals, 9 variables
   b) 4 variables, 4 literals
   c) 4 variables, 9 literals
   d) 9 variables, 9 literals
   e) none of the above

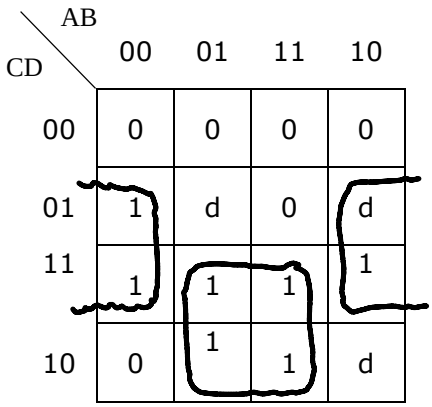
5. For the circuit:

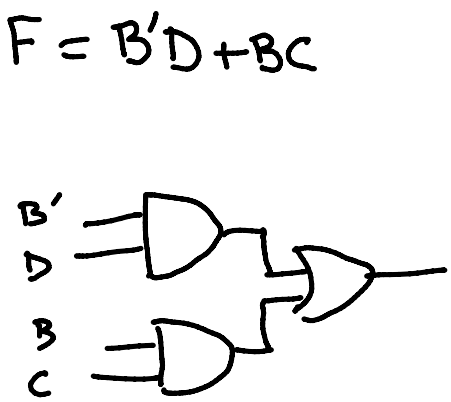


a) f=ab+a'b'+bc
b) f=(a⊕b)(bc)'
c) f=a⊕b⊕c
d) f=0
e) none of the above

6. Draw the minimum cost AND-OR implementation for F. Input variables are available in true and complement forms.

F(A,B,C,D)= Σm(1,3,6,7,11,14,15)+D(5,9,10)





7. Write the VHDL ENTITY and ARCHITECTURE constructs for the circuit described by the equations below. Do not simplify.

   F=(A+B')(C+A'B)'
   G=AB'+C(A'+B)

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ENTITY prob7 IS
   PORT (A,B,C : IN   BIT;
         F,G   : OUT  BIT);
END prob7;
ARCHITECTURE LogicFunc OF prob7 IS
BEGIN
    F <= (A OR NOT B) AND NOT (C OR (NOT A AND B));
    G <= (A AND NOT B) OR (C AND (NOT A OR B));
END LogicFunc;
```

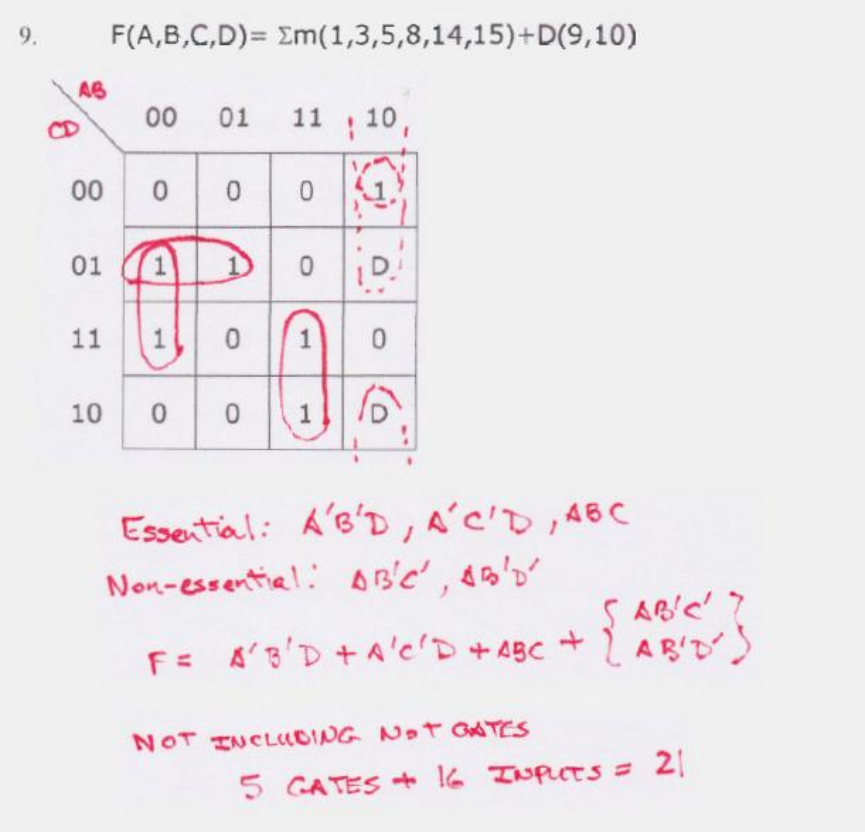
8. Give the MAXTERM notation of the following function.

   f=ab+a'bc'+a'c

   f=ΠM(0,4,5)

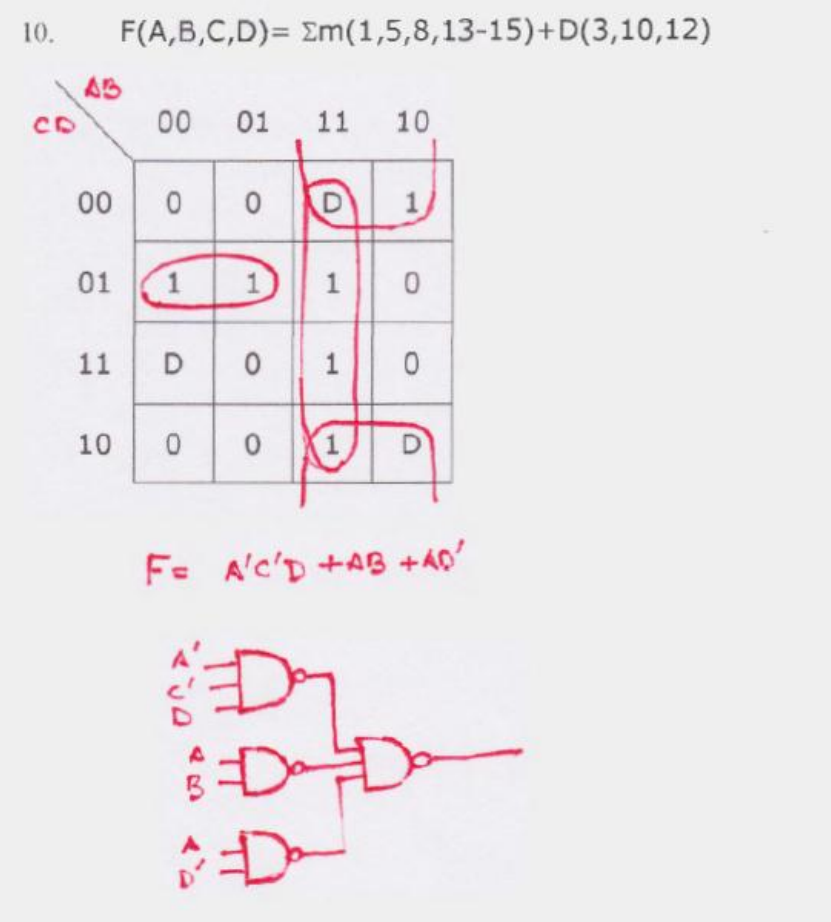
9. Identify the essential and nonessential prime implicants for the function given below. What is the minimum cost SOP expression? What is the COST?

   F(A,B,C,D)= Σm(1,3,5,8,14,15)+D(9,10)



10. Draw the minimum NAND-NAND implementation for F.

F(A,B,C,D)= Σm(1,5,8,13-15)+D(3,10,12)

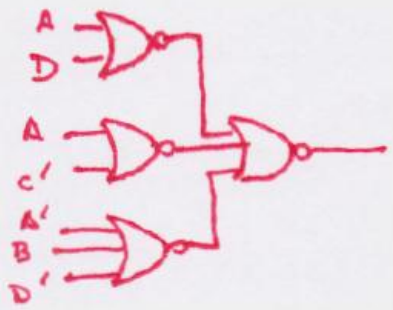


11. Draw the minimum NOR-NOR implementation for F in problem 10.

11. $F(A,B,C,D)= \Sigma m(1,5,8,13\text{-}15)+D(3,10,12)$

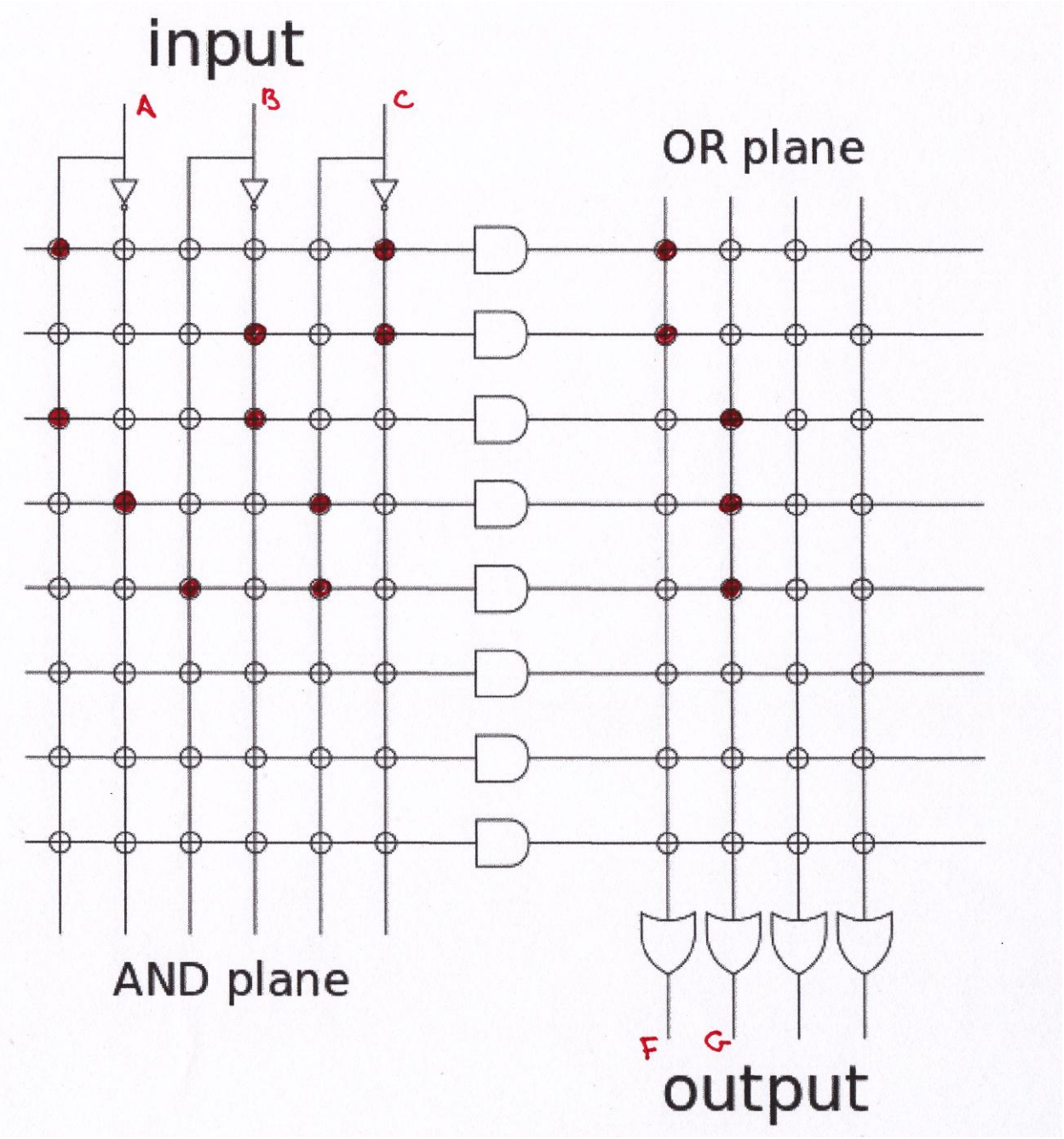
CD \ AB	00	01	11	10
00	0	0	D	1
01	1	1	1	0
11	D	0	1	0
10	0	0	1	D

$F = (A+D)(A+C')(A'+B+D')$



12. Draw the schematic diagram for a programmed PLA that implements the functions below.

F=(A+B')(C+A'B)'
G=AB'+C(A'+B)


input
A
B
C
OR plane
AND plane
F
G
output

Axioms of Boolean algebra

1a. $0 \cdot 0 = 0$
1b. $1 + 1 = 1$
2a. $1 \cdot 1 = 1$
2b. $0 + 0 = 0$
3a. $0 \cdot 1 = 1 \cdot 0 = 0$
3b. $1 + 0 = 0 + 1 = 1$
4a. If $x = 0$ then $x' = 1$
4b. If $x = 1$ then $x' = 0$

Single-Variable theorems

5a. $x \cdot 0 = 0$
5b. $x + 1 = 1$
6a. $x \cdot 1 = x$
6b. $x + 0 = x$
7a. $x \cdot x = x$
7b. $x + x = x$
8a. $x \cdot x' = 0$
8b. $x + x' = 1$
9. $x'' = x$

Two & three variable properties

10a.	$x \cdot y = y \cdot x$	*Commutative*
10b.	$x + y = y + x$	
11a.	$x \cdot (y \cdot z) = (x \cdot y) \cdot z$	*Associative*
11b.	$x + (y + z) = (x + y) + z$	
12a.	$x \cdot (y + z) = x \cdot y + x \cdot z$	*Distributive*
12b.	$x + y \cdot z = (x + y) \cdot (x + z)$	
13a.	$x + x \cdot y = x$	*Absorption*
13b.	$x \cdot (x + y) = x$	
14a.	$x \cdot y + x \cdot y' = x$	*Combining*
14b.	$(x + y) \cdot (x + y') = x$	
15a.	$(x \cdot y)' = x' + y'$	*DeMorgan's*
15b.	$(x + y)' = x' \cdot y'$	*Theorem*
16a.	$x + x' \cdot y = x + y$	
16b.	$x \cdot (x' + y) = x \cdot y$	