

CS2323 Homework 1

CS18BTECH11001

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Q1. Given,

$$\text{Total no. of accesses} = 10^6$$

$$\text{Total Execution Time of program} = 1000ns$$

L1 CACHE :

Given,

$$\text{Leakage Power} = 0.2W$$

$$\text{Dynamic access energy for each access} = 0.217 \text{ nJ}$$

$$\text{Hitrate} = 95\% = 0.95$$

$$\text{Dynamic energy} = (\text{Dynamic access energy for each access}) \times (\text{no. of accesses})$$

$$\Rightarrow \text{Dynamic energy} = (0.217) \times (10^6) = 217000 \text{ nJ}$$

$$\text{Leakage energy} = (\text{Leakage power}) \times (\text{Execution time})$$

$$\Rightarrow \text{Leakage energy} = (0.2) \times (1000) = 200 \text{ nJ}$$

$$\text{Total energy} = \text{Dynamic energy} + \text{Leakage energy}$$

$$\Rightarrow \text{Total energy} = 217000 + 200 = 217200 \text{ nJ}$$

$$\therefore \text{Fraction of energy for L1 CACHE} = \frac{\text{Dynamic energy} \times 100}{\text{Total Energy}} = \frac{217000 \times 100}{217200} = 99.9079$$

L2 CACHE :

Given,

$$\text{Leakage Power} = 6.9W$$

$$\text{Dynamic access energy for each access} = 1.47 \text{ nJ}$$

$$\text{Hitrate} = 100\%(\text{All the misses from L1 CACHE will hit L2 CACHE}) = (1-0.95) \times 1 = 0.05$$

$$\text{Dynamic energy} = (\text{Dynamic access energy for each access}) \times (\text{no. of accesses})$$

$$\Rightarrow \text{Dynamic energy} = (1.47) \times (0.05 \times 10^6) = 73500 \text{ nJ}$$

$$\text{Leakage energy} = (\text{Leakage power}) \times (\text{Execution time})$$

$$\Rightarrow \text{Leakage energy} = (6.9) \times (1000) = 6900 \text{ nJ}$$

$$\text{Total energy} = \text{Dynamic energy} + \text{Leakage energy}$$

$$\Rightarrow \text{Total energy} = 73500 + 6900 = 80400 \text{ nJ}$$

$$\therefore \text{Fraction of energy for L2 CACHE} = \frac{\text{Dynamic energy} \times 100}{\text{Total Energy}} = \frac{73500 \times 100}{80400} = 91.4179$$

Q2. On Increasing the associativity, the no of blocks per set increases which decreases the conflict between two addresses. So, conflict misses decreases but compulsory misses doesn't change which causes marginal decrease in miss rate.

Q3 (a) **CACHE 1 :**

<i>Block Address</i>	<i>Binary Block Address</i>	<i>Tag</i>	<i>Set Index</i>	<i>Hit/Miss</i>
0	00000000	000	000	Miss
63	00111111	001	111	Miss
1	00000001	000	000	Hit
62	00111110	001	111	Hit
2	00000010	000	000	Hit
61	00111101	001	111	Hit
3	00000011	000	000	Hit
60	00111100	001	111	Hit
4	00000100	000	000	Miss
59	00111011	001	110	Miss
5	00000101	000	001	Hit
58	00111010	001	110	Hit
6	00000110	000	001	Hit
57	00111001	001	110	Hit
7	00000111	000	001	Hit
56	00111000	001	110	Hit
8	00001000	000	010	Miss
55	00110111	001	101	Miss
9	00001001	000	010	Hit
54	00110110	001	101	Hit
10	00001010	000	010	Hit
53	00110101	001	101	Hit
11	00001011	000	010	Hit
52	00110100	001	101	Hit

$$Hit\ ratio = \frac{18}{24} = 0.75$$

CACHE 2 :

<i>Block Address</i>	<i>Binary Block Address</i>	<i>Tag</i>	<i>Set Index</i>	<i>Hit/Miss</i>
0	00000000	000	000	Miss
63	00111111	111	111	Miss
1	00000001	001	000	Miss
62	00111110	110	111	Miss
2	00000010	010	000	Miss
61	00111101	101	111	Miss
3	00000011	011	000	Miss
60	00111100	100	111	Miss
4	00000100	100	000	Miss
59	00111011	011	111	Miss
5	00000101	101	000	Miss
58	00111010	010	111	Miss
6	00000110	110	000	Miss
57	00111001	001	111	Miss
7	00000111	111	000	Miss
56	00111000	000	111	Miss
8	00001000	000	001	Miss
55	00110111	111	110	Miss
9	00001001	001	001	Miss
54	00110110	110	110	Miss
10	00001010	010	001	Miss
53	00110101	101	110	Miss
11	00001011	011	001	Miss
52	00110100	100	110	Miss

$$Hit\ ratio = \frac{0}{24} = 0$$

(b) **CACHE 1 :**

<i>Block Address</i>	<i>Binary Block Address</i>	<i>Tag</i>	<i>Set Index</i>	<i>Hit/Miss</i>
0	00000000	000	000	Miss
64	01000000	010	000	Miss
128	10000000	100	000	Miss
192	11000000	110	000	Miss
1	00000001	000	000	Miss
65	01000001	010	000	Miss
129	10000001	100	000	Miss
193	11000001	110	000	Miss
11	00001011	000	010	Miss
75	01001011	010	010	Miss
139	10001011	100	010	Miss
203	11001011	110	010	Miss
9	00001001	000	010	Miss
137	10001001	100	010	Miss
201	11001001	110	010	Miss
73	01001001	010	010	Miss

$$Hit\ ratio = \frac{0}{16} = 0$$

CACHE 2 :

<i>Block Address</i>	<i>Binary Block Address</i>	<i>Tag</i>	<i>Set Index</i>	<i>Hit/Miss</i>
0	00000000	000	000	Miss
64	01000000	000	000	Hit
128	10000000	000	000	Hit
192	11000000	000	000	Hit
1	00000001	001	000	Miss
65	01000001	001	000	Hit
129	10000001	001	000	Hit
193	11000001	001	000	Hit
11	00001011	011	001	Miss
75	01001011	011	001	Hit
139	10001011	011	001	Hit
203	11001011	011	001	Hit
9	00001001	001	001	Miss
137	10001001	001	001	Hit
201	11001001	001	001	Hit
73	01001001	001	001	Hit

$$Hit\ ratio = \frac{12}{16} = 0.75$$

Q4. Processor P1 :

$$Execution\ Time = \frac{\sum_{i=1}^n IC_i \times CPI_i}{Clock\ frequency}$$

$$\Rightarrow Execution\ Time = \frac{\left(\frac{30}{100} \times 2 + \frac{20}{100} \times 2 + \frac{35}{100} \times 4 + \frac{15}{100} \times 4\right) \times 10^6}{2.2 \times 10^9}$$

$$\Rightarrow Execution\ Time = 1.36363ms$$

Processor P2 :

$$Execution\ Time = \frac{\sum_{i=1}^n IC_i \times CPI_i}{Clock\ frequency}$$

$$\Rightarrow Execution\ Time = \frac{\left(\frac{30}{100} \times 2 + \frac{20}{100} \times 1 + \frac{35}{100} \times 2 + \frac{15}{100} \times 3\right) \times 10^6}{1.6 \times 10^9}$$

$$\Rightarrow Execution\ Time = 1.21875ms$$

\therefore Processor P2 is faster for the program.

Q5. Given,

No. of processors = 4

Directory Based coherence protocol is used.

Initially,

0	0	0	0	0
---	---	---	---	---

i. P1 has a read miss

0	1	0	0	0
---	---	---	---	---

ii. P2 has a write miss

0	0	1	0	1
---	---	---	---	---

iii. P0 has a write miss

1	0	0	0	1
---	---	---	---	---

iv. P3 has a read miss

1	0	0	1	0
---	---	---	---	---

v. P3 has a write miss

0	0	0	1	1
---	---	---	---	---

vi. P2 has a read miss

0	0	1	1	0
---	---	---	---	---

Q6. Let the no. of ways of application 1 be w_1

the no. of ways of application 2 be w_2

the no. of misses of application 1 be M_1

the no. of misses of application 2 be M_2

the Total no. of misses be M_{total}

So, $M_{total} = M_1 + M_2$

Given,

Total no. of ways = 8 [i.e., $w_1 + w_2 = 8$]

Application 1 :

Given,

No. of Misses scale linearly with no. of ways [i.e., $M_1 = m \times w_1 + c$]

Misses for 2 ways = 4000 [i.e., $2m + c = 4000$]

Misses for 6 ways = 3600 [i.e., $6m + c = 3600$]

$$2m + c = 4000$$

$$6m + c = 3600$$

$$\Rightarrow 4m = -400$$

$m = -100$

So,

$$\begin{aligned}2m + c &= 4000 \\ \Rightarrow 2 \times (-100) + c &= 4000 \\ \Rightarrow -200 + c &= 4000 \\ \boxed{c} &= 4200\end{aligned}$$

$$\therefore M_1 = 4200 - 100w_1$$

Application 2 :

Given,

No. of Misses scale linearly with no. of ways [i.e., $M_2 = m * w_2 + c$]

Misses for 2 ways = 2040 [i.e., $2m + c = 2040$]

Misses for 6 ways = 1600 [i.e., $6m + c = 1600$]

$$\begin{aligned}2m + c &= 2040 \\ 6m + c &= 1600 \\ \hline \Rightarrow 4m &= -440 \\ \boxed{m} &= -110\end{aligned}$$

So,

$$\begin{aligned}2m + c &= 2040 \\ \Rightarrow 2 \times (-110) + c &= 2040 \\ \Rightarrow -220 + c &= 2040 \\ \boxed{c} &= 2260\end{aligned}$$

$$\therefore M_2 = 2260 - 110w_2$$

$$\text{So, } M_{total} = M_1 + M_2$$

$$\Rightarrow M_{total} = 4200 - 100w_1 + 2260 - 110w_2$$

$$\Rightarrow M_{total} = 6460 - 100(w_1 + w_2) - 10w_2$$

$$\Rightarrow M_{total} = 6460 - 100(8) - 10w_2 \text{ } [\because w_1 + w_2 = 8]$$

$$\Rightarrow M_{total} = 5660 - 10w_2$$

for the M_{total} to be minimum, w_2 must be highest.

But as $w_1 + w_2 = 8$ & $w_1 \geq 2, w_1 \leq 6, w_2 \geq 2, w_2 \leq 6$

The highest value of $\boxed{w_2 = 6}$

$$\text{So, } w_1 + 6 = 8$$

$$\Rightarrow \boxed{w_1 = 2}$$

$$\text{So, } M_{total} = 5660 - 10w_2$$

$$\Rightarrow M_{total} = 5660 - 60$$

$$\boxed{M_{total} = 5600}$$

\therefore The total no. of misses is minimized when the application 1 has 2 ways and application 2 has 6 ways

Q7. (a) Time taken by application P

$$t_1 = \frac{600}{44}$$

Time taken by application Q

$$t_2 = \frac{600}{77}$$

Time taken by application R

$$t_3 = \frac{600}{91}$$

$$\text{Total time taken} = t_1 + t_2 + t_3 = \frac{600}{44} + \frac{600}{77} + \frac{600}{91}$$

$$\text{Total no of transactions} = 600 + 600 + 600 = 1800$$

$$\begin{aligned} \therefore \text{Average value of transactions per min} &= \frac{\text{Total no of transactions}}{\text{Total time taken}} \\ &= \frac{1800}{\frac{600}{44} + \frac{600}{77} + \frac{600}{91}} \\ &= \frac{3}{\frac{1}{44} + \frac{1}{77} + \frac{1}{91}} \end{aligned}$$

\therefore Harmonic mean [H.M] is used to get the average.

(b) Given,

$$\text{Total no. of Instructions} = 70 + 80 + 90 = 240$$

$$\text{Total no. of cycles} = 45 + 35 + 40 = 120$$

Instructions per Cycle [IPC] :

Average using Weighted A.M

$$\text{Weights used} = \frac{45}{120}, \frac{35}{120}, \frac{40}{120}$$

$$\begin{aligned} W.A.M &= \frac{45}{120} \times \frac{70}{45} + \frac{35}{120} \times \frac{80}{35} + \frac{40}{120} \times \frac{90}{40} \\ &= 2 \end{aligned}$$

Average using Weighted H.M

$$\text{Weights used} = \frac{70}{240}, \frac{80}{240}, \frac{90}{240}$$

$$\begin{aligned} W.H.M &= \frac{1}{\frac{70}{240} \times \frac{45}{70} + \frac{80}{240} \times \frac{35}{80} + \frac{90}{240} \times \frac{40}{90}} \\ &= 2 \end{aligned}$$

Cycles per Instruction [CPI] :

Average using Weighted A.M

$$\text{Weights used} = \frac{70}{240}, \frac{80}{240}, \frac{90}{240}$$

$$\begin{aligned} W.A.M &= \frac{70}{240} \times \frac{45}{70} + \frac{80}{240} \times \frac{35}{80} + \frac{90}{240} \times \frac{40}{90} \\ &= 0.5 \end{aligned}$$

Average using Weighted H.M

$$\text{Weights used} = \frac{45}{120}, \frac{35}{120}, \frac{40}{120}$$

$$\begin{aligned} W.H.M &= \frac{1}{\frac{45}{120} \times \frac{70}{45} + \frac{35}{120} \times \frac{80}{35} + \frac{40}{120} \times \frac{90}{40}} \\ &= 0.5 \end{aligned}$$

Q8. Let the total time of the application = t

System 0 :

Given,

$$\text{Time for Initialization} = 29\% = \frac{29t}{100}$$

$$\text{Time for vision-processing function} = 39\% = \frac{39t}{100}$$

$$\text{Time for signal-processing function} = 32\% = \frac{32t}{100}$$

$$\text{Total time}(T_1) = t$$

System 1 :

Given,

$$\text{Time for Initialization} = 29\% = \frac{29t}{100}$$

$$\text{Speedup in vision processing} = 7X$$

$$\text{Time for vision-processing function} = \frac{39t}{100 \times 7}$$

$$\text{Speedup in signal processing} = 12X$$

$$\text{Time for signal-processing function} = 32\% = \frac{32t}{100 \times 12}$$

$$\text{Total time}(T_2) = \frac{29t}{100} + \frac{39t}{100 \times 7} + \frac{32t}{100 \times 12}$$

$$\therefore \text{speedup of system 1 over system 0} = \frac{T_1}{T_2} = \frac{t}{\frac{29t}{100} + \frac{39t}{100 \times 7} + \frac{32t}{100 \times 12}} = 2.68542$$

Q9. (a) Execution time $\propto \frac{1}{\text{clock frequency}}$

So, for the smallest execution time, the frequency is to be maximum

$$\text{Given } f \propto V$$

$$\Rightarrow f = k \times V$$

$$\Rightarrow 3 \times 10^9 = k \times 1$$

$$\Rightarrow k = 3 \times 10^9$$

$$\therefore f = (3 \times 10^9) \times V$$

$$\text{So, the maximum frequency}(f_{\max}) = (3 \times 10^9) \times 1.2 = 3.6 \times 10^9 \text{ Hz}$$

$$\therefore \frac{\text{Execution time}_1}{\text{Execution time}_2} = \frac{\text{clock frequency}_2}{\text{clock frequency}_1}$$

$$\Rightarrow \frac{40}{\text{Execution time}_2} = \frac{3.6 \times 10^9}{3 \times 10^9}$$

$$\Rightarrow \text{Execution time}_2 = 33.33s$$

$$\therefore \text{Minimum Execution time} = 33.33s$$

(b) *Total power = Dynamic power + Leakage power*

$$Total\ power_{min} = Dynamic\ power_{min} + Leakage\ power_{min}$$

$$\begin{array}{l|l} Dynamic\ power \propto V^2 \times f & Leakage\ power \propto V \\ \Rightarrow Dynamic\ power \propto V^3 & \Rightarrow Leakage\ power \propto V \end{array}$$

So, Dynamic power & Leakage power are min at V_{min}

$$\begin{array}{l|l} \Rightarrow \frac{Dynamic\ power_1}{Dynamic\ power_{min}} = \frac{V_1^3}{V_{min}^3} & \Rightarrow \frac{Leakage\ power_1}{Leakage\ power_{min}} = \frac{V_1}{V_{min}} \\ \Rightarrow \frac{110}{Dynamic\ power_{min}} = \frac{1^3}{(0.8)^3} & \Rightarrow \frac{40}{Leakage\ power_{min}} = \frac{1}{0.8} \\ \therefore Dynamic\ power_{min} = 56.32W & \therefore Leakage\ power_{min} = 32W \end{array}$$

$$\therefore Total\ power_{min} = 56.32 + 32 = 88.32W$$

(c) *Total Energy_{at V_1} = (Dynamic power_{at V_1} + Leakage power_{at V_1}) × Execution time_{at V_1}*

$$\begin{array}{l|l|l} Dynamic\ power \propto V^3 & Leakage\ power \propto V & Execution\ time \propto \frac{1}{f} \propto \frac{1}{V} \\ \frac{Dynamic\ power}{Dynamic\ power_{at\ V_1}} = \frac{V^3}{V_1^3} & \frac{Leakage\ power}{Leakage\ power_{at\ V_1}} = \frac{V}{V_1} & \frac{Execution\ time}{Execution\ time_{at\ V_1}} = \frac{V_1}{V} \\ \frac{110}{Dynamic\ power_{at\ V_1}} = \frac{1^3}{V_1^3} & \frac{40}{Leakage\ power_{at\ V_1}} = \frac{1}{V_1} & \frac{40}{Execution\ time_{at\ V_1}} = \frac{V_1}{1} \\ Dynamic\ power_{at\ V_1} = 110 \times V_1^3 & Leakage\ power_{at\ V_1} = 40 \times V_1 & Execution\ time_{at\ V_1} = \frac{40}{V_1} \end{array}$$

$$\Rightarrow TotalEnergy_{at\ V_1} = (110 \times V_1^3 + 40 \times V_1) \times \frac{40}{V_1}$$

$$\Rightarrow Total\ Energy_{at\ V_1} = 4400 \times V_1^2 + 1600$$

So, The total Energy will be minimum when V is minimum

$$\begin{aligned} \therefore Total\ Energy_{min} &= 4400 \times (0.8)^2 + 1600 \\ &= 2816 + 1600 \\ &= 4416J \end{aligned}$$

Q10. (a) (a) ***Least Recently Used[LRU] Replacement policy***

<i>Address of Access Stream</i>	<i>Hit/Miss</i>
P	Miss
Q	Miss
R	Miss
S	Miss
P	Miss
Q	Miss
R	Miss
S	Miss
P	Miss
Q	Miss
R	Miss
S	Miss

Total no. of Misses = 12

(b) Most Recently Used[MRU] Replacement policy

<i>Address of Access Stream</i>	<i>Hit/Miss</i>
P	Miss
Q	Miss
R	Miss
S	Miss
P	Hit
Q	Hit
R	Miss
S	Hit
P	Hit
Q	Miss
R	Hit
S	Hit

Total no. of Misses = 6

(b) Use of Victim Cache :

<i>Access</i>	<i>L1 Cache State</i>			<i>Victim Cache State</i>	<i>L1 Cache Hit/Miss</i>	<i>Victim Cache Hit/Miss</i>
P	P				Miss	
Q	Q	P			Miss	
R	R	Q	P		Miss	
S	S	R	Q	P	Miss	
P	P	S	R	Q	Miss	Hit
Q	Q	P	S	R	Miss	Hit
R	R	Q	P	S	Miss	Hit
S	S	R	Q	P	Miss	Hit
P	P	S	R	Q	Miss	Hit
Q	Q	P	S	R	Miss	Hit
R	R	Q	P	S	Miss	Hit
S	S	R	Q	P	Miss	Hit

Q11. Given,

Base CPI = 3

Miss penalty = 60ns

Clock frequency = 2 GHz

So, Main Memory miss cycles = $60 \times 2 = 120$

Case 1 :

Miss cycles per instruction due to I - Cache Misses = $0.01 \times 120 = 1.2$

Miss cycles per instruction due to D - Cache Misses = $0.03 \times 0.3 \times 120 = 1.08$

Actual CPI = $3 + 1.2 + 1.08 = 5.28$

Case 2 :

L_2 Cache Miss Cycles = $6ns \times 2GHz = 6 \times 2 = 12$

For L_1 Cache :

Miss cycles per instruction due to I - Cache Misses = $0.01 \times 12 = 0.12$

Miss cycles per instruction due to D - Cache Misses = $0.03 \times 0.3 \times 12 = 0.108$

For L_2 Cache :

Miss Cycles per instruction due to D - Cache Misses = $0.04 \times 120 \times 0.3 \times 0.03 = 0.0432$

Actual CPI = $3 + 0.12 + 0.108 + 0.0432 = 3.2712$