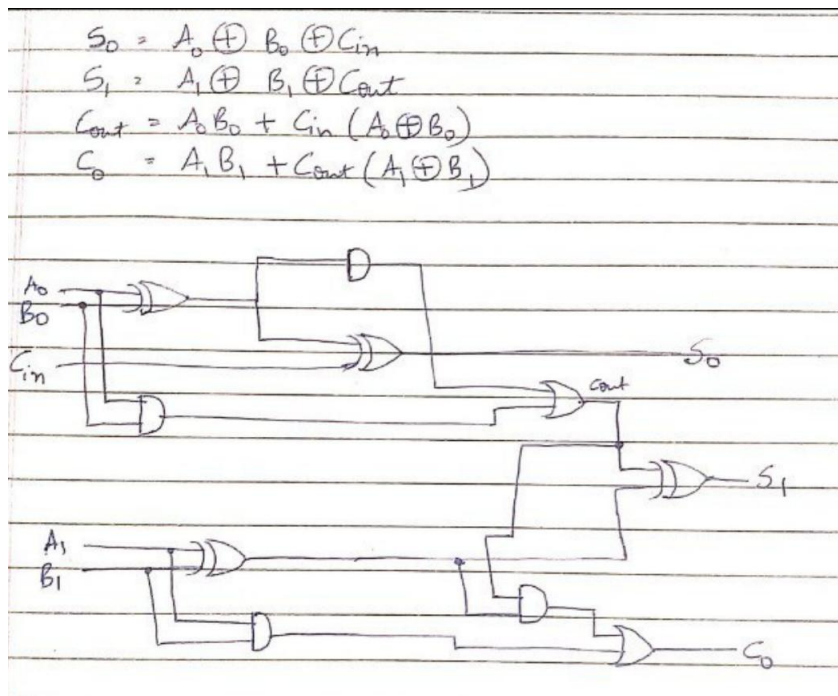


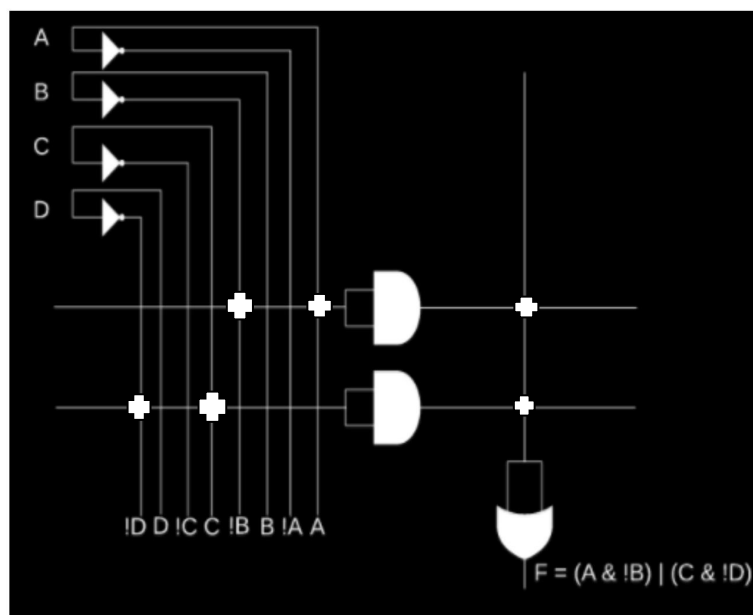
- 1) Using only logic gates, design a 2-bit full adder with carry.
A and B are inputs, C_i is carry in, S_i is output and C_o is carry out.

--



- 2) Show how the logic equation $(A \text{ AND NOT}(B)) \text{ OR } (C \text{ AND NOT}(D))$ can be implemented using the following:

--



RAM CONTENTS				
ADDRESS				OUTPUT Data
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

When A is ANDed with complement of B OR if C is ANDed with complement of D, the above is the only possible solution.