09 December 2024 08:19 PM

Consider a CPU that executes at a clock rate of 200MHz(5ns per cycle) with a single level cache. CPI execution i.e. CPI with ideal memory is 1.1. Instruction mix are 50% arithmetic/Logical, 30% load/store, 20% control instruction.

Assume the cache miss rate is 15% and a miss penalty of 50 cycles. The number of times cpu with ideal memory is faster when no miss occurs _____

Ideal memory Cpu has CPI=1.1

Memory accesses/instruction=cycles required for instruction fetch + cycles required for execution

=(0.5*1+0.3*1+0.2*1)+(0.5*0+0.3*1+0.2*0)=1.3

Total memory stalls=no of references * miss rate * miss penalty =1.3*0.15*50=9.75

CPI of cpu with miss operation=1.1+9.75=10.85

The number of times cpu with ideal memory is faster when no miss occurs =CPU with miss/CPU without miss=10.85/1.1=9.86

A given program has 25% load/store instructions. Suppose the ideal CPI (cycles per instruction) without any memory stalls is 2. The program exhibits 2% miss rate on instruction cache and 8% miss rate on data cache. The miss penalty is 100 cycles. The speedup (rounded off to two decimal places) achieved with a perfect cache (i.e., with NO data or instruction cache misses) is

Given Data:

1. Ideal CPI ($\text{CPI}_{\text{ideal}}$): 2
2. Fraction of Load/Store Instructions ($f_{\text{load/store}}$): $25\% = 0.25$
3. Instruction Cache Miss Rate ($\text{Miss Rate}_{\text{instr}}$): $2\% = 0.02$
4. Data Cache Miss Rate ($\text{Miss Rate}_{\text{data}}$): $8\% = 0.08$
5. Miss Penalty ($\text{Penalty}_{\text{miss}}$): 100 cycles

Step 1: Calculate Memory Stalls Per Instruction

$$\text{Memory Stalls Per Instruction} = (\text{Miss Rate}_{\text{instr}} \times \text{Penalty}_{\text{miss}}) + (f_{\text{load/store}} \times \text{Miss Rate}_{\text{data}} \times \text{Penalty}_{\text{miss}})$$

For Instruction Cache Misses:

$$\text{Stalls from Instr Cache} = 0.02 \times 100 = 2 \,\text{cycles per instruction}$$

For Data Cache Misses:

$$\text{Stalls from Data Cache} = 0.25 \times 0.08 \times 100 = 2 \,\text{cycles per instruction}$$

Total Memory Stalls Per Instruction:

$$\text{Memory Stalls Per Instruction} = 2 + 2 = 4 \,\text{cycles per instruction}$$

Step 2: Calculate CPI with Cache Misses

$$\text{CPI}_{\text{misses}} = \text{CPI}_{\text{ideal}} + \text{Memory Stalls Per Instruction}$$

Substitute the values:

$$\text{CPI}_{\text{misses}} = 2 + 4 = 6$$

Step 3: Calculate Speedup

$$\text{Speedup} = \frac{\text{CPI}_{\text{misses}}}{\text{CPI}_{\text{ideal}}}$$

Substitute the values:

$$\text{Speedup} = \frac{6}{2} = 3.00$$

Final Answer:

The speedup achieved with a perfect cache is **3.00** (rounded to two decimal places).