MCSE503L – Computer Architecture and Organisation

DA – 2

1. Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns (Latch delay or delay due to each register = 10 ns). Calculate-
    - Pipeline cycle time
    - Non-pipeline execution time
    - Speed up ratio
    - Pipeline time for 1000 tasks
    - Sequential time for 1000 tasks
    - Throughput
2. A four stage pipeline has the stage delays as 150, 120, 160 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate, Calculate the total time taken to process 1000 data items on the pipeline.
3. Consider the following program

    loop:

    1. $ADDI\ R2, R2, \#1$
    2. $LD\ R4, 0\ (R3)$
    3. $LD\ R5, 4\ (R3)$
    4. $ADD\ R6, R4, R5$
    5. $MUL\ R4, R6, R7$
    6. $SUBI\ R3, R3, \#8$
    7. $BNEZ\ R2, loop$
    8. $ADD\ R11, R12, R13$

Identify all data dependencies (potential data hazards) in the given code snippet. Specify if the data dependence is RAW, WAW or WAR.

4. Assume that the pipeline now supports full forwarding and bypassing. Furthermore, branches are handled as predicted-not-taken. Which dependencies cause stalls and why? How many cycles does the program take to execute now?

   Loop:

   1. $ADDI\ R2, R2, \#1$

   2. $LD\ R4, 0\ (R3)$

   3. $LD\ R5, 4\ (R3)$

   4. $ADD\ R6, R4, R5$

   5. $MUL\ R4, R6, R7$

   6. $SUBI\ R3, R3, \#8$

   7. $BNEZ\ R2, loop$

   8. $ADD\ R11, R12, R13$

5. A pipelined processor uses a 4-stage instruction pipeline with the following stages: Instruction fetch (IF), Instruction decode (ID), Execute (EX) and Writeback (WB). The arithmetic operations as well as the load and store operations are carried out in the EX stage. The sequence of instructions corresponding to the statement

   X = (S – R * (p + Q)) / T is given below.

   The values of variables P, Q , R ,S , T are available in the registers R0, R1 , R2, R3 and R4 respectively, before the execution of the instruction sequence.

ADD R5 , R0 ,R1

MUL R6,R2,R5

SUB R5,R3,R6

DIV R6 ,R5,R4 ; R5/R4

STORE R6, X

The IF, ID and WB stages take 1 clock cycle each. The EX stage takes 1 clock cycle each for the ADD, SUB and STORE operations, and 3 clock cycles each for MUL and DIV operations. Operand forwarding from the EX stage to the ID stage is used. Calculate the number of clock cycles required to complete the sequence of instructions .

6. The code is run on the Tomasulo architecture, with initial setup (Cycle 0) . Show what happens during the execution of the code for the first four (4) cycles, starting with Cycle 1. I recommend that you use the Tomasulo_table_template.

		Latency
L.D	F0, 10(R2)	2
ADD.D	F10, F8, F0	1
DIV.D	F2, F10, F6	5
L.D	F4, 0(R3)	2
ADD.D	F12, F4, F2	1