MCSE503L – Computer Architecture and Organisation

DA – 1

1. Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

a) Which processor has the highest performance expressed in instructions per second?

b) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

c) We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

2. A program runs in 10 seconds on computer A, which has a 2 GHz clock. A computer designer wants to build a computer B, which will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this may cause the computer B to require 1.2 times as many clock cycles as computer A for this program. What clock rate should we tell the designer to target?

3. Compilers can have a profound impact on the performance of an application. Assume that for a program, compiler A results in a dynamic instruction count of 1.0×10^9 and has an execution time of 1.1 s, while compiler B results in a dynamic instruction count of 1.2×10^9 and an execution time of 1.5 s.

a) Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.

b) Assume the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?

c) A new compiler is developed that uses only 6.0x108 instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using compiler A or B on the original processor?

Trying to reduce execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

4. Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2. Given a program with a dynamic instruction count of 1.0×10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C and 20% class D. Find the global CPI for each implementation? Compare the implementations and determine the faster one.

5. A byte-addressable computer has a small data cache capable of holding eight 32-bit words. Each cache block consists of one 32-bit word. When a given program is executed, the processor reads data sequentially from the following hex addresses: 200, 204, 208, 20C, 2F4, 2F0, 200, 204, 218, 21C, 24C, 2F4. This pattern is repeated two times.

a) Assume that the cache is initially empty. Show the contents of the cache at the end of each pass through the loop if a direct-mapped cache is used.

b) Compute the Hit rate and Miss rate.

6. Assume a memory access to main memory on a cache "miss" takes 30 ns and a memory access to the cache on a cache "hit" takes 3 ns. If 80% of the processor's memory requests result in a cache "hit", what is the average memory access time?

7. Which is the fastest cache mapping function? Justify.

8. Which cache mapping function does not require a replacement algorithm? Why.

9. M1 : 16K word 50 ns access time
M2: 1M words 400 ns Access time
If 8 word cache line and set size is 256 words with set associative mapping
-Give Mapping between M2 and M1.
-Calculate Effective memory access time (Cache hit ratio =0.95)

10. Consider a 2 way set associative cache with 256 blocks and uses LRU replacement. The following sequence of access to memory block
[0 , 128 , 256, 128, 0 , 128, 256 , 128 , 1 , 129 , 257 , 129 , 1 , 129 , 257, 129]
Find the number of conflict Misses.