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Router Verification Project Overview

Router Top Level Block Diagram

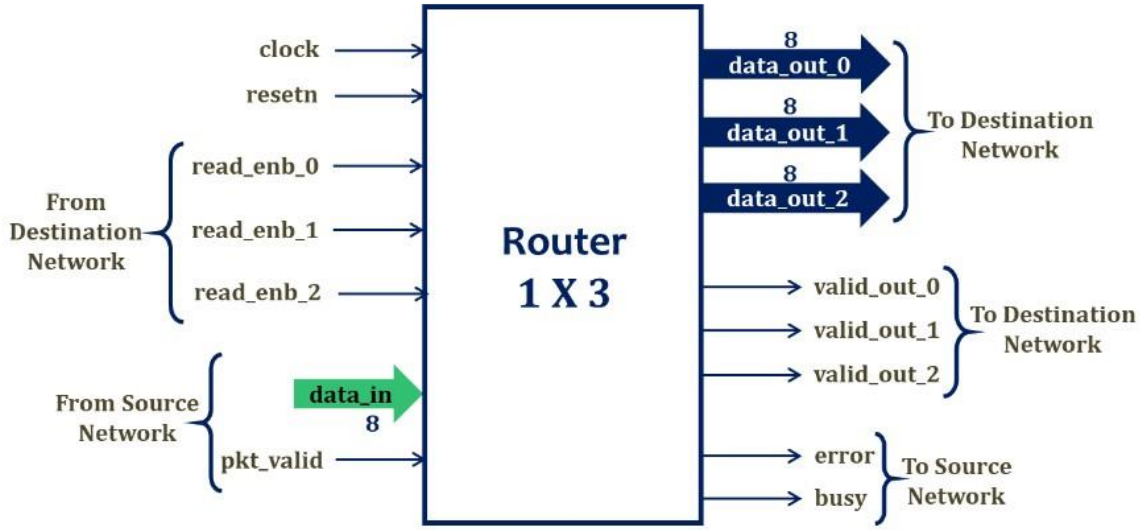

Fig. 1 Block Diagram of 1X3 Router

Overview

- The Router 1X3 design follows packet-based protocol and it receives the network packet from a source LAN using data_in on a byte-by-byte basis on active posedge of the clock. resetn is an active low synchronous reset.
- The start of a new packet is indicated by asserting pkt_valid and end of the current packet is indicated by de-asserting pkt_valid. The design stores the incoming packet inside a FIFO as per the address of the packet. The design has got 3 FIFOs for respective destination LANs.
- Sometimes router can enter busy state which is indicated by busy signal. It is sent back to source so that the source will wait to send the next byte of the packet.
- To evaluate the correctness of the packet received, there is error detection mechanism called parity check. If there is any mismatch, then it is indicated by error signal.

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- The design can receive only 1 packet and can read 3 packets at a time.

Packet Structure

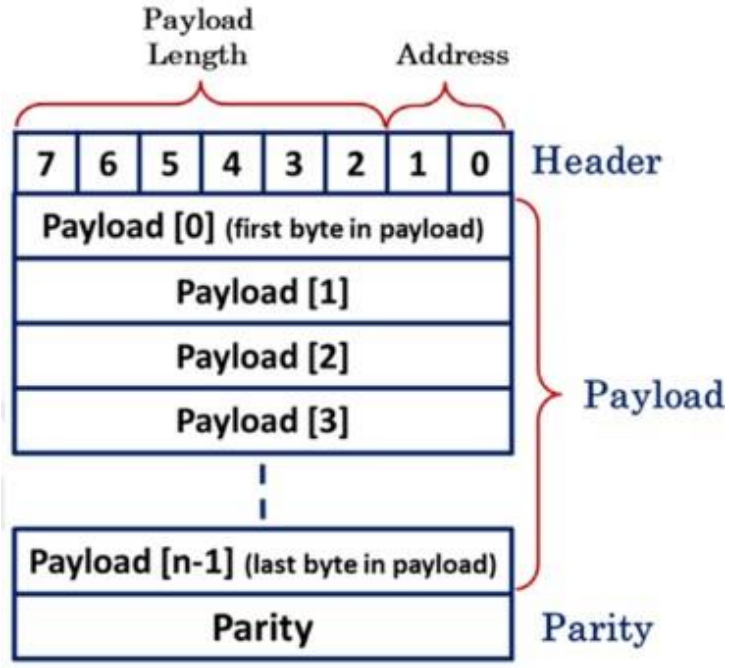

Fig. 2 Packet Structure

The packet consists of 3 parts: Header, payload and parity each of 8-bit width and the length of the payload can be extended between 3 between 1 byte to 63 byte.

Header: Packet header contain two fields DA and length.

- DA: destination address of the packet is of 2 bits. The router drives the packet to the respective ports based on this destination address of the packets. Each output port has 2-bit unique port address. If the destination address of the packet matches the port address, then router drives the packet to the output port. The address "3" is invalid.
- Length: length of the data is of 6-bits. It specifies the number of the number of the data bytes. A packet can have a minimum data size of 1 byte and a maximum size of 63 bytes.

i. If length =1, it means data length is 1 byte If length =2, it means data length is 2 bytes.

ii. If length =63, it means data length is 63 bytes

Payload: payload is the data information. Data should be in terms of the bytes.

Parity: This field contains the security check of the packet. It is calculated as bitwise exor over the header and payload bytes of the packet as mentioned below.

Features to be verified

- The packet should reach all the three destinations properly as per the channel address.
- All the three destinations should receive packet of all the possible payload lengths.
- When the data is corrupted, error signal should go high.
- When data out is not read within 30 cycles of valid out going high, soft reset should occur.
- When busy signal is high, data should be stable until busy signal becomes low.
- Address of destination network will never be 2'b11. So, header [1:0] should never be 2'b11.
- Payload length contains information of no. of payload bytes in the packet structure. Payload length should lie between 1 to 63 and never be 0.

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Router Input Waveform

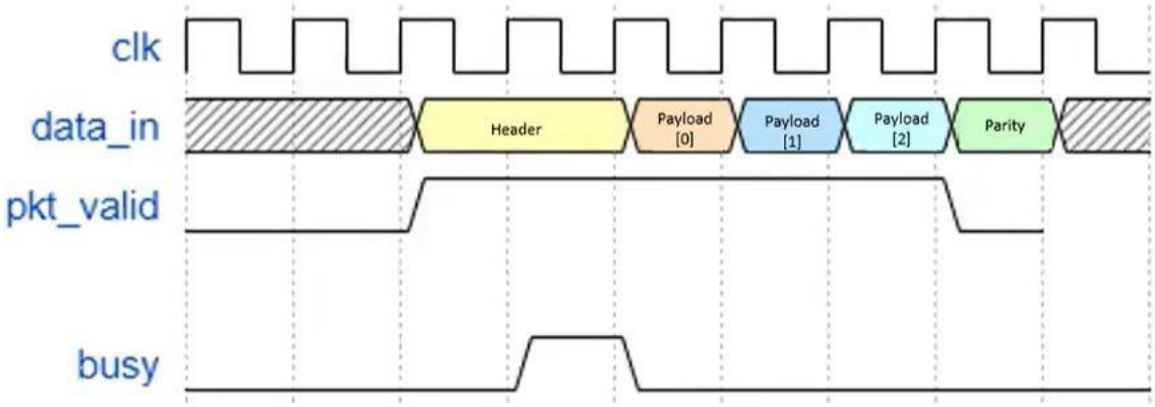

Fig. 3 Input Waveform

- Clocking block can be used to drive the signals on the positive edge of the clock itself and thus avoids metastability.
- The pkt_valid signal is asserted on the same clock edge when the header byte driven onto the input data bus.
- Each subsequent byte of payload after header byte should be driven on the input data bus for every new raising edge of the clock.
- After the last payload byte has been driven, on the next falling edge of the clock, the pkt_valid signal must be de-asserted, and the packet parity should be driven.
- The testbench shouldn't drive any byte when busy signal is detected instead it should hold the last driven values.
- The "busy" signal when asserted drops any incoming byte of the data.
- The "err" signal is asserted when a packet parity mismatch is detected. After 2 clock cycles of routing parity information, error signal is sent by DUT.

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Router Output Waveform

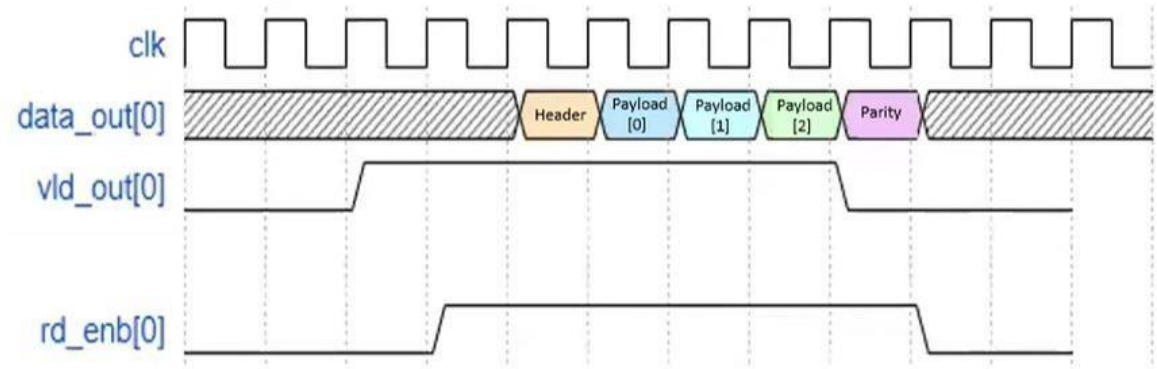

Fig. 4 Output Waveform

- All output signals are active high and are synchronized to the rising edge of the clock.
- Each output port data_out[X] (data_out[0], data_out[1], data_out[2]) is internally buffered by a FIFO of size 16X9.
- The router asserts the vld_out[X] (vld_out[0], vld_out[1], vld_out[2]) signal when valid data appears on the data_out[X] (data_out[0], data_out[1], data_out[2]) output bus. This is a signal to the receiver's client which indicates the data is available on a particular output data bus.
- The packet receiver will then wait until it has enough space to hold the bytes of the packet and then respond with the assertion of the rd_enb[X](rd_enb[0], rd_enb[1], rd_enb[2]) signal.
- The rd_enb[X](rd_enb[0], rd_enb[1], rd_enb[2]) must be asserted within 30 clock cycles of the vld_out[X] (vld_out[0], vld_out[1], vld_out[2]) being asserted else time-out occurs, which resets the FIFO.