Assignment 7

mahesh

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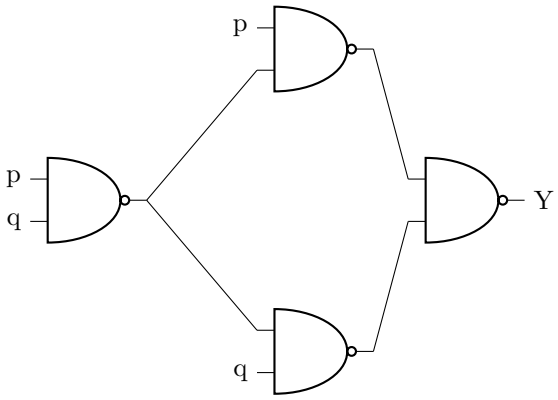

Figure 1: Logic Gate for NAND logic

$$Y = p.\overline{q} + q.\overline{p} \tag{1}$$