Assignment 11

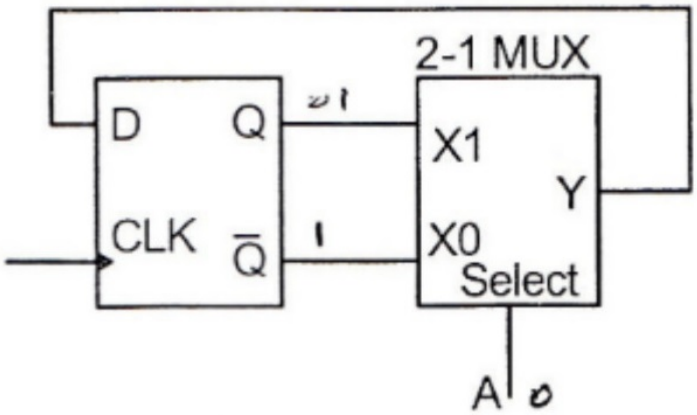
Solution to gate EC 2014-2,question 9

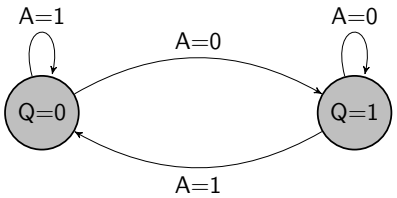
January 9, 2021

Table of Contents

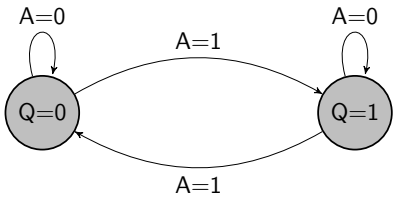
Question

The state transition diagram for the logic circuit shown as

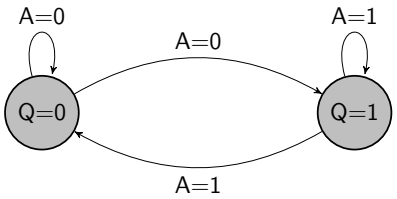




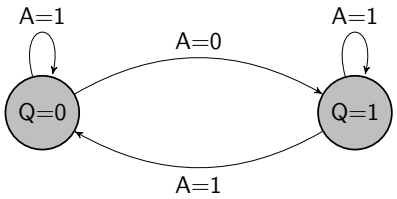
(a) (A)



(b) (B)



(c) (C)



(d) (D)

Table of Contents

Explanation

We know,
2-1 MUX $\Longrightarrow$ 2-1 Multiplexer
When A=0,
X_0 line is selected and connected to $\overline{Q}$ and now $\overline{Q}$
is now connected to X_0 that is, X_0 is going to be shortened to Y. The output Y is now communicated with X_0 which is connected to $\overline{Q}$.
so,Y will become whenever A=0
$Y = X_0 = \overline{Q} = D$
$then, Q+ = \overline{Q}$
and similarly when A=1
Y=X_1=Q=D Assume that Q=0 as one state and Q=1 as another state
At state Q=0
if A=0
then transition of state changes from Q=0 to Q=1
if A=1
then transition of state remains constant

Explanation

At state Q=1
if A=0
then transition of state remains constant
if A=1
then transition of state changes from Q=1 to Q=0

Table of Contents

Transition Table

Q (P.S)	input D	**(N.S)** Q_n
0	0	0
0	1	1
1	0	0
1	1	1

Table: Sate Transition Table

Table of Contents

Conclusion

Hence OPTION 'D' IS THE RIGHT OPTION