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| Tool Version     : Vivado v.2025.1 (win64) Build 6140274 Thu May 22 00:12:29 MDT 2025
| Date             : Tue Nov 11 12:20:05 2025
| Host             : LAPTOP-ETMBL9OL running 64-bit major release  (build 9200)
| Command          : report_power -file fifo_buffer_power_routed.rpt -pb fifo_buffer_power_summary_routed.pb -rpx fifo_buffer_power_routed.rpx
| Design           : fifo_buffer
| Device           : xc7z020clg484-1
| Design State     : routed
| Grade            : commercial
| Process          : typical
| Characterization : Production
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```

Power Report

Table of Contents

1. Summary

Total On-Chip Power (W)	3.544
Design Power Budget (W)	Unspecified*
Power Budget Margin (W)	NA
Dynamic (W)	3.336
Device Static (W)	0.208
Effective TJA (C/W)	11.5
Max Ambient (C)	44.1
Junction Temperature (C)	65.9
Confidence Level	Low
Setting File	---
Simulation Activity File	---
Design Nets Matched	NA

* Specify Design Power Budget using, set_operating_conditions -design_power_budget <value in Watts>

1.1 On-Chip Components

On-Chip	Power (W)	Used	Available	Utilization (%)
Slice Logic	0.103	41	---	---
LUT as Logic	0.082	13	53200	0.02
LUT as Distributed RAM	0.010	4	17400	0.02
BUFG	0.006	1	32	3.13
Register	0.005	12	106400	0.01
Others	0.000	1	---	---
Signals	0.152	32	---	---
I/O	3.081	14	200	7.00
Static Power	0.208			
Total	3.544			

1.2 Power Supply Summary

Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)	Powerup (A)	Budget (A)	Margin (A)
Vccint	1.000	0.319	0.283	0.036	NA	Unspecified	NA
Vccaux	1.800	0.136	0.112	0.025	NA	Unspecified	NA
Vcco33	3.300	0.865	0.864	0.001	NA	Unspecified	NA
Vcco25	2.500	0.000	0.000	0.000	NA	Unspecified	NA
Vcco18	1.800	0.000	0.000	0.000	NA	Unspecified	NA
Vcco15	1.500	0.000	0.000	0.000	NA	Unspecified	NA
Vcco135	1.350	0.000	0.000	0.000	NA	Unspecified	NA
Vcco12	1.200	0.000	0.000	0.000	NA	Unspecified	NA

| Vccaux_io | 1.800 | 0.000 | 0.000 | 0.000 |
NA | Unspecified | NA |
| Vccbram | 1.000 | 0.002 | 0.000 | 0.002 |
NA | Unspecified | NA |
| MGTAVcc | 1.000 | 0.000 | 0.000 | 0.000 |
NA | Unspecified | NA |
| MGTAVtt | 1.200 | 0.000 | 0.000 | 0.000 |
NA | Unspecified | NA |
| MGTVccaux | 1.800 | 0.000 | 0.000 | 0.000 |
NA | Unspecified | NA |
| Vccpint | 1.000 | 0.062 | 0.000 | 0.062 |
NA | Unspecified | NA |
| Vccpaux | 1.800 | 0.010 | 0.000 | 0.010 |
NA | Unspecified | NA |
| Vccpll | 1.800 | 0.003 | 0.000 | 0.003 |
NA | Unspecified | NA |
| Vcco_ddr | 1.500 | 0.000 | 0.000 | 0.000 |
NA | Unspecified | NA |
| Vcco_mio0 | 1.800 | 0.000 | 0.000 | 0.000 |
NA | Unspecified | NA |
| Vcco_mio1 | 1.800 | 0.000 | 0.000 | 0.000 |
NA | Unspecified | NA |
| Vccadc | 1.800 | 0.020 | 0.000 | 0.020 |
NA | Unspecified | NA |
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1.3 Confidence Level

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| User Input Data | Confidence | Details
| Action
|
+-----------------------------+------------+-----------------------------
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| Design implementation state | High | Design is routed
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| Clock nodes activity | Low | User specified less than 75%
of clocks | Provide missing clock activity with a
constraint file, simulation results or by editing the "By Clock Domain"
view |
| I/O nodes activity | Low | More than 75% of inputs are
missing user specification | Provide missing input activity with
simulation results or by editing the "By Resource Type -> I/Os" view
|
| Internal nodes activity | Medium | User specified less than 25%
of internal nodes | Provide missing internal nodes activity with
simulation results or by editing the "By Resource Type" views |
| Device models | High | Device models are Production
|
|

Overall confidence level	Low	

2. Settings

2.1 Environment

Ambient Temp (C)	25.0
ThetaJA (C/W)	11.5
Airflow (LFM)	250
Heat Sink	none
ThetaSA (C/W)	0.0
Board Selection	medium (10"x10")
# of Board Layers	8to11 (8 to 11 Layers)
Board Temperature (C)	25.0

2.2 Clock Constraints

Clock	Domain	Constraint (ns)

3. Detailed Reports

3.1 By Hierarchy

Name	Power (W)
fifo_buffer	3.336
FIFO_reg_0_7_0_3	0.014