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| Tool Version : Vivado v.2025.1 (win64) Build 6140274 Thu May 22
00:12:29 MDT 2025
| Date         : Tue Nov 11 12:20:05 2025
| Host         : LAPTOP-ETMBL9OL running 64-bit major release  (build
9200)
| Command      : report_timing_summary -max_paths 10 -routable_nets -
report_unconstrained -file fifo_buffer_timing_summary_routed.rpt -pb
fifo_buffer_timing_summary_routed.pb -rpx
fifo_buffer_timing_summary_routed.rpx -warn_on_violation
| Design       : fifo_buffer
| Device       : 7z020-clg484
| Speed File   : -1  PRODUCTION 1.12 2019-11-22
| Design State : Routed
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Timing Summary Report

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| Timer Settings
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  Enable Multi Corner Analysis               :  Yes
  Enable Pessimism Removal                   :  Yes
  Pessimism Removal Resolution               :  Nearest Common Node
  Enable Input Delay Default Clock           :  No
  Enable Preset / Clear Arcs                 :  No
  Disable Flight Delays                      :  No
  Ignore I/O Paths                           :  No
  Timing Early Launch at Borrowing Latches   :  No
  Borrow Time for Max Delay Exceptions       :  Yes
  Merge Timing Exceptions                    :  Yes
  Inter-SLR Compensation                     :  Conservative

  Corner  Analyze    Analyze
  Name    Max Paths  Min Paths
  ------  ---------  ---------
  Slow    Yes        Yes
  Fast    Yes        Yes


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| Report Methodology
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```

Rule	Severity	Description	Violations
TIMING-17	Critical Warning	Non-clocked sequential cell	20

Note: This report is based on the most recent report_methodology run and may not be up-to-date. Run report_methodology on the current design for the latest report.

check_timing report

Table of Contents
----

1. checking no_clock (20)

There are 20 register/latch pins with no clock driven by root clock pin: CLOCK (HIGH)

2. checking constant_clock (0)

There are 0 register/latch pins with constant_clock.

3. checking pulse_width_clock (0)

There are 0 register/latch pins which need pulse_width check

4. checking unconstrained_internal_endpoints (72)

There are 72 pins that are not constrained for maximum delay. (HIGH)

There are 0 pins that are not constrained for maximum delay due to constant clock.

5. checking no_input_delay (7)

There are 7 input ports with no input delay specified. (HIGH)

There are 0 input ports with no input delay but user has a false path constraint.

```
6. checking no_output_delay (6)
-------------------------------
 There are 6 ports with no output delay specified. (HIGH)

 There are 0 ports with no output delay but user has a false path
constraint

 There are 0 ports with no output delay but with a timing clock defined
on it or propagating through it


7. checking multiple_clock (0)
------------------------------
 There are 0 register/latch pins with multiple clocks.


8. checking generated_clocks (0)
--------------------------------
 There are 0 generated clocks that are not connected to a clock source.


9. checking loops (0)
---------------------
 There are 0 combinational loops in the design.


10. checking partial_input_delay (0)
------------------------------------
 There are 0 input ports with partial input delay specified.


11. checking partial_output_delay (0)
-------------------------------------
 There are 0 ports with partial output delay specified.


12. checking latch_loops (0)
----------------------------
 There are 0 combinational latch loops in the design through latch input



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| Design Timing Summary
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    WNS(ns)      TNS(ns)  TNS Failing Endpoints  TNS Total Endpoints
WHS(ns)      THS(ns)  THS Failing Endpoints  THS Total Endpoints
WPWS(ns)     TPWS(ns)  TPWS Failing Endpoints  TPWS Total Endpoints
    -------      -------  --------------------  -------------------
-------      -------  --------------------  -------------------     ----
----     --------  ----------------------  --------------------
```

```
        inf        0.000                     0                   78
inf        0.000                     0                   78           NA
NA                    NA                    NA


There are no user specified timing constraints.


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| Clock Summary
| -------------
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| Intra Clock Table
| -----------------
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----------------------

Clock             WNS(ns)      TNS(ns)  TNS Failing Endpoints  TNS Total
Endpoints      WHS(ns)      THS(ns)  THS Failing Endpoints  THS Total
Endpoints     WPWS(ns)     TPWS(ns)  TPWS Failing Endpoints  TPWS Total
Endpoints
-----             -------      -------  ---------------------  ----------
---------      -------      -------  ---------------------  -------------
------     --------     --------  ----------------------  ---------------
-----


------------------------------------------------------------------------
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| Inter Clock Table
| -----------------
------------------------------------------------------------------------
----------------------

From Clock    To Clock          WNS(ns)      TNS(ns)  TNS Failing
Endpoints  TNS Total Endpoints      WHS(ns)      THS(ns)  THS Failing
Endpoints  THS Total Endpoints
----------    --------          -------      -------  -------------------
--  -------------------      -------      -------  ---------------------
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------------------------------------------------------------------------
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| Other Path Groups Table
| -----------------------
------------------------------------------------------------------------
----------------------

Path Group    From Clock    To Clock          WNS(ns)      TNS(ns)  TNS
Failing Endpoints  TNS Total Endpoints      WHS(ns)      THS(ns)  THS
Failing Endpoints  THS Total Endpoints
```

```
----------    ----------    --------          -------      -------  -----
---------------  --------------------      -------      -------  --------
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```

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| User Ignored Path Table
| -----------------------
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```
Path Group    From Clock    To Clock
----------    ----------    --------
```

```
------------------------------------------------------------------------
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| Unconstrained Path Table
| ------------------------
------------------------------------------------------------------------
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```

```
Path Group    From Clock    To Clock
----------    ----------    --------
(none)
```

```
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| Timing Details
| --------------
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------------------------------------------------------------------------
-------------
Path Group:  (none)
From Clock:
  To Clock:

Max Delay            78 Endpoints
Min Delay            78 Endpoints
------------------------------------------------------------------------
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```

```
Max Delay Paths
------------------------------------------------------------------------
-------------
Slack:                   inf
  Source:                RD_PTR_EXT_reg[0]/C
                           (rising edge-triggered cell FDRE)
  Destination:           EMPTY
                           (output port)
  Path Group:            (none)
  Path Type:             Max at Slow Process Corner
```

```
  Data Path Delay:        9.864ns  (logic 4.533ns (45.954%)  route
5.331ns (54.046%))
  Logic Levels:           4  (FDRE=1 LUT3=1 LUT6=1 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X112Y88        FDRE                         0.000     0.000 r
RD_PTR_EXT_reg[0]/C
    SLICE_X112Y88        FDRE (Prop_fdre_C_Q)         0.518     0.518 r
RD_PTR_EXT_reg[0]/Q
                         net (fo=11, routed)          1.161     1.679
RD_PTR_EXT_reg_n_0_[0]
    SLICE_X111Y87        LUT6 (Prop_lut6_I1_O)        0.124     1.803 r
FULL_OBUF_inst_i_2/O
                         net (fo=9, routed)           0.848     2.650
RD_DATA2
    SLICE_X113Y87        LUT3 (Prop_lut3_I0_O)        0.152     2.802 r
EMPTY_OBUF_inst_i_1/O
                         net (fo=1, routed)           3.323     6.125
EMPTY_OBUF
    W22                  OBUF (Prop_obuf_I_O)         3.739     9.864 r
EMPTY_OBUF_inst/O
                         net (fo=0)                   0.000     9.864
EMPTY
    W22                                                          r
EMPTY (OUT)
  -------------------------------------------------------------------
-------------------

Slack:                   inf
  Source:                RD_PTR_EXT_reg[0]/C
                           (rising edge-triggered cell FDRE)
  Destination:           FULL
                           (output port)
  Path Group:            (none)
  Path Type:             Max at Slow Process Corner
  Data Path Delay:       9.353ns  (logic 4.278ns (45.744%)  route
5.074ns (54.256%))
  Logic Levels:          4  (FDRE=1 LUT3=1 LUT6=1 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X112Y88        FDRE                         0.000     0.000 r
RD_PTR_EXT_reg[0]/C
    SLICE_X112Y88        FDRE (Prop_fdre_C_Q)         0.518     0.518 r
RD_PTR_EXT_reg[0]/Q
                         net (fo=11, routed)          1.161     1.679
RD_PTR_EXT_reg_n_0_[0]
    SLICE_X111Y87        LUT6 (Prop_lut6_I1_O)        0.124     1.803 r
FULL_OBUF_inst_i_2/O
                         net (fo=9, routed)           0.846     2.648
RD_DATA2
    SLICE_X113Y87        LUT3 (Prop_lut3_I0_O)        0.124     2.772 r
FULL_OBUF_inst_i_1/O
```

```
                         net (fo=1, routed)           3.068     5.840
FULL_OBUF
    U19                  OBUF (Prop_obuf_I_O)         3.512     9.353 r
FULL_OBUF_inst/O
                         net (fo=0)                   0.000     9.353
FULL
    U19                                                                 r
FULL (OUT)
  -------------------------------------------------------------------
-------------------

Slack:                    inf
  Source:                 RD_DATA_reg[3]/C
                            (rising edge-triggered cell FDRE)
  Destination:            RD_DATA[3]
                            (output port)
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        7.160ns  (logic 3.986ns (55.664%)  route
3.175ns (44.336%))
  Logic Levels:           2  (FDRE=1 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X113Y87        FDRE                         0.000     0.000 r
RD_DATA_reg[3]/C
    SLICE_X113Y87        FDRE (Prop_fdre_C_Q)         0.456     0.456 r
RD_DATA_reg[3]/Q
                         net (fo=1, routed)           3.175     3.631
RD_DATA_OBUF[3]
    U21                  OBUF (Prop_obuf_I_O)         3.530     7.160 r
RD_DATA_OBUF[3]_inst/O
                         net (fo=0)                   0.000     7.160
RD_DATA[3]
    U21                                                                 r
RD_DATA[3] (OUT)
  -------------------------------------------------------------------
-------------------

Slack:                    inf
  Source:                 RD_DATA_reg[2]/C
                            (rising edge-triggered cell FDRE)
  Destination:            RD_DATA[2]
                            (output port)
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        7.105ns  (logic 3.987ns (56.114%)  route
3.118ns (43.886%))
  Logic Levels:           2  (FDRE=1 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X113Y87        FDRE                         0.000     0.000 r
RD_DATA_reg[2]/C
```

```
    SLICE_X113Y87        FDRE (Prop_fdre_C_Q)         0.456     0.456 r
RD_DATA_reg[2]/Q
                         net (fo=1, routed)           3.118     3.574
RD_DATA_OBUF[2]
    U22                  OBUF (Prop_obuf_I_O)         3.531     7.105 r
RD_DATA_OBUF[2]_inst/O
                         net (fo=0)                   0.000     7.105
RD_DATA[2]
    U22                                                          r
RD_DATA[2] (OUT)
  -------------------------------------------------------------------
-------------------

Slack:                    inf
  Source:                 RD_DATA_reg[0]/C
                            (rising edge-triggered cell FDRE)
  Destination:            RD_DATA[0]
                            (output port)
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        7.092ns  (logic 3.978ns (56.095%)  route
3.114ns (43.905%))
  Logic Levels:           2  (FDRE=1 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X113Y87        FDRE                         0.000     0.000 r
RD_DATA_reg[0]/C
    SLICE_X113Y87        FDRE (Prop_fdre_C_Q)         0.456     0.456 r
RD_DATA_reg[0]/Q
                         net (fo=1, routed)           3.114     3.570
RD_DATA_OBUF[0]
    T22                  OBUF (Prop_obuf_I_O)         3.522     7.092 r
RD_DATA_OBUF[0]_inst/O
                         net (fo=0)                   0.000     7.092
RD_DATA[0]
    T22                                                          r
RD_DATA[0] (OUT)
  -------------------------------------------------------------------
-------------------

Slack:                    inf
  Source:                 RD_DATA_reg[1]/C
                            (rising edge-triggered cell FDRE)
  Destination:            RD_DATA[1]
                            (output port)
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        6.947ns  (logic 3.970ns (57.144%)  route
2.977ns (42.856%))
  Logic Levels:           2  (FDRE=1 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
-------------------
```

```
    SLICE_X113Y87        FDRE                          0.000     0.000 r
RD_DATA_reg[1]/C
    SLICE_X113Y87        FDRE (Prop_fdre_C_Q)          0.456     0.456 r
RD_DATA_reg[1]/Q
                         net (fo=1, routed)            2.977     3.433
RD_DATA_OBUF[1]
    T21                  OBUF (Prop_obuf_I_O)          3.514     6.947 r
RD_DATA_OBUF[1]_inst/O
                         net (fo=0)                    0.000     6.947
RD_DATA[1]
    T21                                                          r
RD_DATA[1] (OUT)
  -------------------------------------------------------------------
------------------

Slack:                    inf
  Source:                 RD_EN
                            (input port)
  Destination:            RD_PTR_EXT_reg[0]/CE
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        4.993ns  (logic 1.063ns (21.294%)  route
3.930ns (78.706%))
  Logic Levels:           2  (IBUF=1 LUT5=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
------------------
    H17                                            0.000     0.000 r
RD_EN (IN)
                         net (fo=0)                    0.000     0.000
RD_EN
    H17                  IBUF (Prop_ibuf_I_O)          0.939     0.939 r
RD_EN_IBUF_inst/O
                         net (fo=1, routed)            3.120     4.059
RD_EN_IBUF
    SLICE_X111Y87        LUT5 (Prop_lut5_I4_O)         0.124     4.183 r
RD_DATA[3]_i_2/O
                         net (fo=8, routed)            0.810     4.993
RD_DATA[3]_i_2_n_0
    SLICE_X112Y88        FDRE                                    r
RD_PTR_EXT_reg[0]/CE
  -------------------------------------------------------------------
------------------

Slack:                    inf
  Source:                 RD_EN
                            (input port)
  Destination:            RD_PTR_EXT_reg[1]/CE
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        4.993ns  (logic 1.063ns (21.294%)  route
3.930ns (78.706%))
  Logic Levels:           2  (IBUF=1 LUT5=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
```

```
  ------------------------------------------------------------------
------------------
    H17                                               0.000     0.000 r
RD_EN (IN)
                         net (fo=0)                   0.000     0.000
RD_EN
    H17                  IBUF (Prop_ibuf_I_O)         0.939     0.939 r
RD_EN_IBUF_inst/O
                         net (fo=1, routed)           3.120     4.059
RD_EN_IBUF
    SLICE_X111Y87        LUT5 (Prop_lut5_I4_O)        0.124     4.183 r
RD_DATA[3]_i_2/O
                         net (fo=8, routed)           0.810     4.993
RD_DATA[3]_i_2_n_0
    SLICE_X112Y88        FDRE                                       r
RD_PTR_EXT_reg[1]/CE
  ------------------------------------------------------------------
------------------

Slack:                    inf
  Source:                 RD_EN
                            (input port)
  Destination:            RD_DATA_reg[0]/CE
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        4.670ns  (logic 1.063ns (22.769%)  route
3.606ns (77.231%))
  Logic Levels:           2  (IBUF=1 LUT5=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  ------------------------------------------------------------------
------------------
    H17                                               0.000     0.000 r
RD_EN (IN)
                         net (fo=0)                   0.000     0.000
RD_EN
    H17                  IBUF (Prop_ibuf_I_O)         0.939     0.939 r
RD_EN_IBUF_inst/O
                         net (fo=1, routed)           3.120     4.059
RD_EN_IBUF
    SLICE_X111Y87        LUT5 (Prop_lut5_I4_O)        0.124     4.183 r
RD_DATA[3]_i_2/O
                         net (fo=8, routed)           0.486     4.670
RD_DATA[3]_i_2_n_0
    SLICE_X113Y87        FDRE                                       r
RD_DATA_reg[0]/CE
  ------------------------------------------------------------------
------------------

Slack:                    inf
  Source:                 RD_EN
                            (input port)
  Destination:            RD_DATA_reg[1]/CE
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        4.670ns  (logic 1.063ns (22.769%)  route
3.606ns (77.231%))
```

```
  Logic Levels:           2  (IBUF=1 LUT5=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
------------------
    H17                                               0.000     0.000 r
RD_EN (IN)
                         net (fo=0)                   0.000     0.000
RD_EN
    H17                  IBUF (Prop_ibuf_I_O)         0.939     0.939 r
RD_EN_IBUF_inst/O
                         net (fo=1, routed)           3.120     4.059
RD_EN_IBUF
    SLICE_X111Y87        LUT5 (Prop_lut5_I4_O)        0.124     4.183 r
RD_DATA[3]_i_2/O
                         net (fo=8, routed)           0.486     4.670
RD_DATA[3]_i_2_n_0
    SLICE_X113Y87        FDRE                                       r
RD_DATA_reg[1]/CE
  -------------------------------------------------------------------
------------------
```

```
Min Delay Paths
--------------------------------------------------------------------------------
-------------
Slack:                   inf
  Source:                RD_PTR_EXT_reg[2]/C
                           (rising edge-triggered cell FDRE)
  Destination:           RD_PTR_EXT_reg[3]/D
  Path Group:            (none)
  Path Type:             Min at Fast Process Corner
  Data Path Delay:       0.375ns  (logic 0.183ns (48.860%)  route
0.192ns (51.140%))
  Logic Levels:          2  (FDRE=1 LUT4=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
------------------
    SLICE_X111Y87        FDRE                         0.000     0.000 r
RD_PTR_EXT_reg[2]/C
    SLICE_X111Y87        FDRE (Prop_fdre_C_Q)         0.141     0.141 r
RD_PTR_EXT_reg[2]/Q
                         net (fo=9, routed)           0.192     0.333
RD_PTR_EXT_reg_n_0_[2]
    SLICE_X111Y87        LUT4 (Prop_lut4_I2_O)        0.042     0.375 r
RD_PTR_EXT[3]_i_1/O
                         net (fo=1, routed)           0.000     0.375
p_0_in__1[3]
    SLICE_X111Y87        FDRE                                       r
RD_PTR_EXT_reg[3]/D
  -------------------------------------------------------------------
------------------
```

```
Slack:                    inf
  Source:                 RD_PTR_EXT_reg[2]/C
                            (rising edge-triggered cell FDRE)
  Destination:            RD_PTR_EXT_reg[2]/D
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.378ns  (logic 0.186ns (49.266%)  route
0.192ns (50.734%))
  Logic Levels:           2  (FDRE=1 LUT3=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X111Y87        FDRE                         0.000     0.000 r
RD_PTR_EXT_reg[2]/C
    SLICE_X111Y87        FDRE (Prop_fdre_C_Q)         0.141     0.141 r
RD_PTR_EXT_reg[2]/Q
                         net (fo=9, routed)           0.192     0.333
RD_PTR_EXT_reg_n_0_[2]
    SLICE_X111Y87        LUT3 (Prop_lut3_I2_O)        0.045     0.378 r
RD_PTR_EXT[2]_i_1/O
                         net (fo=1, routed)           0.000     0.378
p_0_in__1[2]
    SLICE_X111Y87        FDRE                                       r
RD_PTR_EXT_reg[2]/D
  -------------------------------------------------------------------
-------------------

Slack:                    inf
  Source:                 WR_PTR_EXT_reg[0]/C
                            (rising edge-triggered cell FDRE)
  Destination:            WR_PTR_EXT_reg[3]/D
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.380ns  (logic 0.184ns (48.410%)  route
0.196ns (51.590%))
  Logic Levels:           2  (FDRE=1 LUT4=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X110Y87        FDRE                         0.000     0.000 r
WR_PTR_EXT_reg[0]/C
    SLICE_X110Y87        FDRE (Prop_fdre_C_Q)         0.141     0.141 r
WR_PTR_EXT_reg[0]/Q
                         net (fo=13, routed)          0.196     0.337
WR_PTR_EXT_reg_n_0_[0]
    SLICE_X110Y87        LUT4 (Prop_lut4_I1_O)        0.043     0.380 r
WR_PTR_EXT[3]_i_2/O
                         net (fo=1, routed)           0.000     0.380
p_0_in__2[3]
    SLICE_X110Y87        FDRE                                       r
WR_PTR_EXT_reg[3]/D
  -------------------------------------------------------------------
-------------------
```

```
Slack:                    inf
  Source:                 WR_PTR_EXT_reg[0]/C
                            (rising edge-triggered cell FDRE)
  Destination:            WR_PTR_EXT_reg[2]/D
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.382ns  (logic 0.186ns (48.680%)  route
0.196ns (51.320%))
  Logic Levels:           2  (FDRE=1 LUT3=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X110Y87        FDRE                         0.000     0.000 r
WR_PTR_EXT_reg[0]/C
    SLICE_X110Y87        FDRE (Prop_fdre_C_Q)         0.141     0.141 r
WR_PTR_EXT_reg[0]/Q
                         net (fo=13, routed)          0.196     0.337
WR_PTR_EXT_reg_n_0_[0]
    SLICE_X110Y87        LUT3 (Prop_lut3_I0_O)        0.045     0.382 r
WR_PTR_EXT[2]_i_1/O
                         net (fo=1, routed)           0.000     0.382
p_0_in__2[2]
    SLICE_X110Y87        FDRE                                       r
WR_PTR_EXT_reg[2]/D
  -------------------------------------------------------------------
-------------------

Slack:                    inf
  Source:                 WR_PTR_EXT_reg[0]/C
                            (rising edge-triggered cell FDRE)
  Destination:            WR_PTR_EXT_reg[1]/D
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.390ns  (logic 0.183ns (46.923%)  route
0.207ns (53.077%))
  Logic Levels:           2  (FDRE=1 LUT2=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X110Y87        FDRE                         0.000     0.000 r
WR_PTR_EXT_reg[0]/C
    SLICE_X110Y87        FDRE (Prop_fdre_C_Q)         0.141     0.141 r
WR_PTR_EXT_reg[0]/Q
                         net (fo=13, routed)          0.207     0.348
WR_PTR_EXT_reg_n_0_[0]
    SLICE_X110Y87        LUT2 (Prop_lut2_I0_O)        0.042     0.390 r
WR_PTR_EXT[1]_i_1/O
                         net (fo=1, routed)           0.000     0.390
p_0_in__2[1]
    SLICE_X110Y87        FDRE                                       r
WR_PTR_EXT_reg[1]/D
  -------------------------------------------------------------------
-------------------
```

```
Slack:                    inf
  Source:                 WR_PTR_EXT_reg[0]/C
                            (rising edge-triggered cell FDRE)
  Destination:            WR_PTR_EXT_reg[0]/D
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.393ns  (logic 0.186ns (47.328%)  route
0.207ns (52.672%))
  Logic Levels:           2  (FDRE=1 LUT1=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X110Y87        FDRE                         0.000     0.000 r
WR_PTR_EXT_reg[0]/C
    SLICE_X110Y87        FDRE (Prop_fdre_C_Q)         0.141     0.141 f
WR_PTR_EXT_reg[0]/Q
                         net (fo=13, routed)          0.207     0.348
WR_PTR_EXT_reg_n_0_[0]
    SLICE_X110Y87        LUT1 (Prop_lut1_I0_O)        0.045     0.393 r
WR_PTR_EXT[0]_i_1/O
                         net (fo=1, routed)           0.000     0.393
p_0_in__2[0]
    SLICE_X110Y87        FDRE                                       r
WR_PTR_EXT_reg[0]/D
  -------------------------------------------------------------------
-------------------

Slack:                    inf
  Source:                 RD_PTR_EXT_reg[0]/C
                            (rising edge-triggered cell FDRE)
  Destination:            RD_PTR_EXT_reg[1]/D
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.394ns  (logic 0.207ns (52.488%)  route
0.187ns (47.512%))
  Logic Levels:           2  (FDRE=1 LUT2=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X112Y88        FDRE                         0.000     0.000 r
RD_PTR_EXT_reg[0]/C
    SLICE_X112Y88        FDRE (Prop_fdre_C_Q)         0.164     0.164 r
RD_PTR_EXT_reg[0]/Q
                         net (fo=11, routed)          0.187     0.351
RD_PTR_EXT_reg_n_0_[0]
    SLICE_X112Y88        LUT2 (Prop_lut2_I0_O)        0.043     0.394 r
RD_PTR_EXT[1]_i_1/O
                         net (fo=1, routed)           0.000     0.394
p_0_in__1[1]
    SLICE_X112Y88        FDRE                                       r
RD_PTR_EXT_reg[1]/D
  -------------------------------------------------------------------
-------------------
```

```
Slack:                    inf
  Source:                 RD_PTR_EXT_reg[0]/C
                            (rising edge-triggered cell FDRE)
  Destination:            RD_PTR_EXT_reg[0]/D
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.396ns  (logic 0.209ns (52.728%)  route
0.187ns (47.272%))
  Logic Levels:           2  (FDRE=1 LUT1=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X112Y88        FDRE                         0.000     0.000 r
RD_PTR_EXT_reg[0]/C
    SLICE_X112Y88        FDRE (Prop_fdre_C_Q)         0.164     0.164 f
RD_PTR_EXT_reg[0]/Q
                         net (fo=11, routed)          0.187     0.351
RD_PTR_EXT_reg_n_0_[0]
    SLICE_X112Y88        LUT1 (Prop_lut1_I0_O)        0.045     0.396 r
RD_PTR_EXT[0]_i_1/O
                         net (fo=1, routed)           0.000     0.396
p_0_in__1[0]
    SLICE_X112Y88        FDRE                                       r
RD_PTR_EXT_reg[0]/D
  -------------------------------------------------------------------
-------------------

Slack:                    inf
  Source:                 WR_PTR_EXT_reg[2]/C
                            (rising edge-triggered cell FDRE)
  Destination:            FIFO_reg_0_7_0_3/RAMA/WADR2
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.401ns  (logic 0.141ns (35.155%)  route
0.260ns (64.845%))
  Logic Levels:           1  (FDRE=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X110Y87        FDRE                         0.000     0.000 r
WR_PTR_EXT_reg[2]/C
    SLICE_X110Y87        FDRE (Prop_fdre_C_Q)         0.141     0.141 r
WR_PTR_EXT_reg[2]/Q
                         net (fo=11, routed)          0.260     0.401
FIFO_reg_0_7_0_3/ADDRD2
    SLICE_X112Y87        RAMD32                                     r
FIFO_reg_0_7_0_3/RAMA/WADR2
  -------------------------------------------------------------------
-------------------

Slack:                    inf
  Source:                 WR_PTR_EXT_reg[2]/C
                            (rising edge-triggered cell FDRE)
```

```
  Destination:            FIFO_reg_0_7_0_3/RAMA_D1/WADR2
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.401ns  (logic 0.141ns (35.155%)  route
0.260ns (64.845%))
  Logic Levels:           1  (FDRE=1)

    Location             Delay type                Incr(ns)  Path(ns)
Netlist Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X110Y87        FDRE                         0.000     0.000 r
WR_PTR_EXT_reg[2]/C
    SLICE_X110Y87        FDRE (Prop_fdre_C_Q)         0.141     0.141 r
WR_PTR_EXT_reg[2]/Q
                         net (fo=11, routed)          0.260     0.401
FIFO_reg_0_7_0_3/ADDRD2
    SLICE_X112Y87        RAMD32                                     r
FIFO_reg_0_7_0_3/RAMA_D1/WADR2
  -------------------------------------------------------------------
-------------------
```