✅ **Topic 1: Implementation of Basic Gates (AND, OR, NOT) using ICs**

1. **MCQ**: Which IC is used for implementing AND gates?
   A) 7404 B) 7408 C) 7432 D) 7486

2. **MCQ**: The IC 7404 contains how many NOT gates?
   A) 2 B) 4 C) 6 D) 8

3. **Short Answer**: Name the IC used for the 2-input OR gate.

4. **True/False**: IC 7432 is used for NAND gate implementation.

5. **Short Answer**: Draw the pin diagram for IC 7408.

6. **MCQ**: Which IC is used to implement NOT gates?
   A) 7408 B) 7410 C) 7404 D) 7432

7. **Short Answer**: What logic function is performed by IC 7432?

8. **True/False**: TTL logic family is faster than CMOS.

9. **Short Answer**: Write a brief procedure to verify an AND gate using IC 7408.

10. **MCQ**: Which IC package contains all three basic logic gates (AND, OR, NOT)?
    A) 7400 B) 7410 C) Not available D) 7486

✅ **Topic 2: Boolean Expressions & K-map Simplification**

1. **MCQ**: A + AB = ?
   A) B B) AB C) A D) A + B

2. **True/False**: $A + A' = 1$ is a valid Boolean identity.

3. **Short Answer**: Simplify $AB + A'B + AB'$

4. **Short Answer**: Express the function $F = A + B(C + D)$ in canonical SOP form.

5. **K-map**: Use a 3-variable K-map to simplify $F = Σm(1, 2, 3, 5)$

6. **MCQ**: How many cells are there in a 4-variable K-map?
   A) 8 B) 12 C) 16 D) 32

7. **Short Answer**: What is the dual of the expression $AB + C$?

8. **True/False**: In Boolean algebra, $A + A = 2A$

9. **MCQ**: What is the simplified form of $A'B + AB$?
   A) A + B
   B) B
   C) A ⊕ B
   D) A ≡ B

10. **Short Answer**: Simplify using Boolean theorems:
    $(A + B)(A + B')$

✅ **Topic 3: Universality of NAND & NOR Gates**

1. **MCQ**: NAND gate can be used to implement:
   A) AND B) OR C) NOT D) All of the above

2. **True/False**: NOR gate is not a universal gate.

3. **Short Answer**: How can you make an OR gate using only NOR gates?

4. **Short Answer**: Show how to implement NOT using only NAND gates.

5. **MCQ**: How many NAND gates are needed to build a NOT gate?
   A) 2 B) 1 C) 3 D) 0

6. **MCQ**: Which is more power-efficient in CMOS: NAND or NOR?
   A) NAND B) NOR C) Both same D) None

7. **Short Answer**: Why are NAND gates preferred in IC design?

8. **True/False**: NAND and NOR gates can be used to build any digital circuit.

9. **Short Answer**: Implement the expression $A + B$ using only NAND gates.

10. **Short Answer**: Design a XOR gate using only NOR gates.

✅ **Topic 4: Combinational Circuits (Adder, Subtractor, Encoder, Decoder)**

1. **MCQ**: What are the outputs of a half adder?
   A) Sum and Carry
   B) Sum and Borrow
   C) Carry and Borrow
   D) None

2. **Short Answer**: Write the truth table for a half subtractor.

3. **MCQ**: A 3-to-8 decoder has how many output lines?
   A) 4 B) 6 C) 8 D) 3

4. **True/False**: An encoder has fewer input lines than output lines.

5. **Short Answer**: Design a 2-to-4 decoder circuit.

6. **Short Answer**: What is the difference between a multiplexer and a decoder?

7. **MCQ**: A full adder requires how many XOR gates?
   A) 2 B) 3 C) 4 D) 1

8. **True/False**: A half adder can be used to design a full adder.

9. **Short Answer**: Write the block diagram of a 4-bit binary adder.

10. **MCQ**: Which logic gate combination is used in a full subtractor?
    A) XOR, AND, OR

B) AND, OR
C) NAND, NOR
D) XOR, NOR

✅ **Topic 5: Circuits Using NAND, NOR Only**

1. **Short Answer**: Implement NOT using NAND.

2. **MCQ**: To implement AND using NOR gates, what is the minimum number of gates required?
A) 2 B) 3 C) 4 D) 1

3. **Short Answer**: Implement OR gate using NAND only.

4. **True/False**: Every Boolean expression can be implemented using only NAND gates.

5. **MCQ**: Which gate has the highest propagation delay?
A) XOR B) NOR C) NAND D) AND

6. **Short Answer**: Design a 2-input XOR gate using only NAND gates.

7. **True/False**: NAND gates are easier to fabricate in CMOS technology.

8. **Short Answer**: Implement a 2-input NOR gate using NAND gates.

9. **MCQ**: How many NAND gates are required to build a 2-input XOR gate?
A) 4 B) 5 C) 6 D) 3

10. **Short Answer**: Show the circuit diagram of a 3-input AND gate using only NANDs.

✅ **Topic 6: Sequential Circuits, Flip-Flops, Shift Registers**

1. **MCQ**: Which flip-flop toggles its state when both inputs are 1?
A) SR B) JK C) D D) T

2. **True/False**: SR flip-flop has a forbidden state.

3. **Short Answer**: Draw the truth table of a D flip-flop.

4. **Short Answer**: What is a race-around condition in JK flip-flop?

5. **MCQ**: How many flip-flops are required for a 4-bit shift register?
   A) 2 B) 3 C) 4 D) 5

6. **Short Answer**: Design a T flip-flop using a JK flip-flop.

7. **True/False**: A shift register can be used for data storage.

8. **Short Answer**: What is the difference between serial-in parallel-out and parallel-in serial-out shift registers?

9. **MCQ**: Which of the following is edge-triggered?
   A) Latch B) SR C) JK D) D Flip-Flop

10. **Short Answer**: Verify the output of a 4-bit SISO register with input = 1010.

✅ **Topic 1: Implementation of Basic Gates using ICs**

1. **C) 7408**
2. **C) 6**
3. **7432**
4. **False**
5. **[Draw 7408 pin diagram: 14-pin IC, each gate on 3 pins: A, B, and Output]**
6. **C) 7404**
7. **Performs logical OR**
8. **True**
9. **Connect inputs and verify output logic with truth table**
10. **C) Not available**

✅ **Topic 2: Boolean Expressions & K-map Simplification**

1. **C) A**

2. **True**
3. **F = A + B**
4. **F = AB + AC + AD + BC + BD + CD** (Canonical form)
5. **F = B'C + BC' (simplified via K-map)**
6. **C) 16**
7. **A + B (dual of AB + C)**
8. **False**
9. **D) A ≡ B**
10. **F = A + B**

✅ **Topic 3: Universality of NAND & NOR Gates**

1. **D) All of the above**
2. **False**
3. **Use NOR → NOT (A NOR A), then use De Morgan's to construct OR**
4. **Connect both inputs of NAND to A (A NAND A = A')**
5. **B) 1**
6. **A) NAND**
7. **They are functionally complete and easy to fabricate in CMOS**
8. **True**
9. **(A NAND A) NAND (B NAND B)**
10. **Build A NOR B = (A + B)' and then derive XOR from NOR combinations**

✅ **Topic 4: Combinational Circuits (Adder, Subtractor, Encoder, Decoder)**

1. **A) Sum and Carry**
2. **Truth Table:**

A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

3. **C) 8**
4. **False**
5. **[Draw 2 inputs, 4 outputs: Y0 to Y3; logic: Y0 = A'B', Y1 = A'B, Y2 = AB', Y3 = AB]**
6. **MUX selects input; decoder activates outputs based on input**
7. **A) 2**
8. **True**
9. **[Four full adders connected in cascade]**

10. **A) XOR, AND, OR**

✅ **Topic 5: Circuits Using NAND, NOR Only**

1. **Connect both NAND inputs to A → output is A'**
2. **B) 3**
3. **A NAND A = A'; B NAND B = B'; then (A' NAND B')' = A + B**
4. **True**
5. **B) NOR**
6. **XOR = ((A NAND B) NAND (A NAND A)) NAND ((A NAND B) NAND (B NAND B))**
7. **True**
8. **Use De Morgan's laws and extra inverters to convert NAND to NOR**
9. **C) 6**
10. **Use 2-input NAND gate structure to connect 3 inputs**

✅ **Topic 6: Sequential Circuits, Flip-Flops, Shift Registers**

1. **B) JK**
2. **True**
3. **Truth Table (D Flip-Flop):**

D	CLK	Q (Next State)
0	↑	0
1	↑	1
4. **Condition when both J = K = 1 and clock is high → toggles rapidly (unstable)**
5. **C) 4**
6. **Connect J = T, K = T to JK Flip-Flop → becomes T Flip-Flop**
7. **True**
8. **SIPO: Data in serial, out in parallel. PISO: Data in parallel, out serially**
9. **D) D Flip-Flop**
10. **Input: 1 → 0 → 1 → 0 → output will shift accordingly: Q3 Q2 Q1 Q0 = 1010**

Great! Here's a **new set of 10 quiz questions and answers per topic** for **Digital System Design**, covering different sub-areas than before. Each question is followed by its correct answer.

✅ **Topic 1: Implementation of Basic Gates using ICs (Set 2)**

1. **Which IC is used for implementing the NOT gate?**
   A) 7408 B) 7400 C) 7404 D) 7432
   ➤ **Answer:** C) 7404
2. **What is the function of pin 14 on a 7408 IC?**
   ➤ **Answer:** It is the Vcc pin (+5V supply).
3. **How many NOT gates are in 7404?**
   ➤ **Answer:** 6
4. **Which gate is not available in 7400 series?**
   A) XOR B) OR C) NOT D) NAND
   ➤ **Answer:** A) XOR
5. **Which is the ground pin in 7432 IC?**
   ➤ **Answer:** Pin 7
6. **What is the typical operating voltage for TTL ICs like 7408?**
   ➤ **Answer:** 5V
7. **A gate whose output is LOW only when all inputs are HIGH is:**
   ➤ **Answer:** NAND gate
8. **Which instrument is used to verify the output logic of IC gates?**
   ➤ **Answer:** Logic probe or LED
9. **What does IC 7400 contain?**
   ➤ **Answer:** Four 2-input NAND gates
10. **How can you test an IC logic gate circuit?**
    ➤ **Answer:** Apply inputs and compare outputs with the truth table.

✅ **Topic 2: Boolean Expressions & K-map (Set 2)**

1. **Which Boolean identity simplifies A + AB?**
   ➤ **Answer:** A
2. **What is the result of A + A'?**
   ➤ **Answer:** 1
3. **A 3-variable K-map contains how many cells?**
   ➤ **Answer:** 8
4. **What does the expression A(B + C) simplify to?**
   ➤ **Answer:** AB + AC
5. **Which method is best for simplifying a logic expression?**
   ➤ **Answer:** Karnaugh Map (K-map)
6. **F = A + AB' simplifies to:**
   ➤ **Answer:** A + B'

7. **Which term is not valid in a canonical SOP form?**
   A) AB B) ABC' C) A'C D) A + B
   ➤ **Answer:** D) A + B
8. **How many 1's must be grouped together in a K-map?**
   ➤ **Answer:** Power of 2 (1, 2, 4, 8, etc.)
9. **Which law is used in A + AB = A?**
   ➤ **Answer:** Absorption Law
10. **The dual of the equation A + 0 = A is:**
    ➤ **Answer:** A • 1 = A

✅ **Topic 3: Universality of NAND & NOR (Set 2)**

1. **How can an OR gate be implemented using NAND?**
   ➤ **Answer:** A' NAND B' (using inverters and NAND)
2. **Which universal gate is faster in CMOS?**
   ➤ **Answer:** NAND
3. **What is the output of a NAND gate with both inputs HIGH?**
   ➤ **Answer:** LOW
4. **What is the result of A NOR A?**
   ➤ **Answer:** A'
5. **What type of gate is needed to implement XOR using NAND?**
   ➤ **Answer:** 4 NAND gates minimum
6. **Why are NAND gates widely used in IC design?**
   ➤ **Answer:** Economical, fast, easy to fabricate
7. **Which gate gives output HIGH only if all inputs are LOW?**
   ➤ **Answer:** NOR gate
8. **Can a NOT gate be built using only NAND gates?**
   ➤ **Answer:** Yes
9. **To build AND using NOR gates, what logic is applied?**
   ➤ **Answer:** Invert inputs, then NOR
10. **Which logic family prefers NOR in memory cell design?**
    ➤ **Answer:** RTL (Resistor-Transistor Logic)

✅ **Topic 4: Combinational Circuits (Set 2)**

1. **What does an encoder do?**
   ➤ **Answer:** Converts inputs to binary code.

2. **Which adder handles carry from previous stage?**
   ➤ **Answer:** Full Adder
3. **How many outputs does a 3-to-8 decoder have?**
   ➤ **Answer:** 8
4. **A 2-to-4 decoder requires how many input lines?**
   ➤ **Answer:** 2
5. **Which circuit selects one of many data inputs?**
   ➤ **Answer:** Multiplexer
6. **Which is not a combinational circuit?**
   A) Adder B) Decoder C) Flip-Flop D) Subtractor
   ➤ **Answer:** C) Flip-Flop
7. **What is the output of XOR gate if both inputs are 1?**
   ➤ **Answer:** 0
8. **Which logic circuit adds two 4-bit numbers?**
   ➤ **Answer:** 4-bit Parallel Adder
9. **What is the purpose of a decoder?**
   ➤ **Answer:** Activate only one output for each input pattern
10. **Which combinational circuit has more outputs than inputs?**
    ➤ **Answer:** Decoder

✅ **Topic 5: Circuits using NAND/NOR only (Set 2)**

1. **NAND is equivalent to which gate followed by NOT?**
   ➤ **Answer:** AND
2. **To build OR using NAND, which law is applied?**
   ➤ **Answer:** De Morgan's Law
3. **Which gate combination gives XOR using only NOR?**
   ➤ **Answer:** 5 NOR gates
4. **Why are NAND gates preferred in logic design?**
   ➤ **Answer:** Universality and ease of integration
5. **NOR + NOR = which gate behavior?**
   ➤ **Answer:** AND
6. **NAND as inverter works when:**
   ➤ **Answer:** Both inputs are tied together
7. **Using NAND, NOT gate is formed by:**
   ➤ **Answer:** A NAND A

8. **Which circuit needs fewer gates: NAND-only or NOR-only?**
   ➤ **Answer:** NAND-only (usually)
9. **How many 2-input NAND gates are needed to implement a 3-input AND?**
   ➤ **Answer:** 5
10. **Can XOR be implemented using only NANDs?**
    ➤ **Answer:** Yes

✅ **Topic 6: Sequential Circuits & Flip-Flops (Set 2)**

1. **What is the purpose of the clock signal in flip-flops?**
   ➤ **Answer:** Synchronize state changes
2. **What happens in SR flip-flop when S = 1 and R = 0?**
   ➤ **Answer:** Output is set (Q = 1)
3. **Which flip-flop toggles its state on clock pulse?**
   ➤ **Answer:** T Flip-Flop
4. **What is the output of a D Flip-Flop after one clock if D = 0?**
   ➤ **Answer:** Q = 0
5. **Which register allows data to be loaded in serially and read out in parallel?**
   ➤ **Answer:** SIPO (Serial In Parallel Out)
6. **How many flip-flops are required to build a 4-bit shift register?**
   ➤ **Answer:** 4
7. **Which flip-flop type can be used as a frequency divider?**
   ➤ **Answer:** T Flip-Flop
8. **Flip-flop transition occurs at:**
   ➤ **Answer:** Clock edge
9. **Which flip-flop has an undefined state when both inputs are 1?**
   ➤ **Answer:** SR Flip-Flop (basic)
10. **In JK Flip-Flop, when J = K = 1, what is the output?**
    ➤ **Answer:** Output toggles

Let me know if you'd like these as a printable handout or want another batch of questions!