The Innovate UK office will be closed from 5:00pm on Friday 23 May until 9:00am on Wednesday 28 May 2025. Please email support@iuk.ukri.org and we will reply when our phone lines reopen.

Project details

Subsidy basis

Partner	Funding rules	
MEDIPROSPECTSAI LIMITED	Subsidy control	View answers
TRACKGENESIS LIMITED	Subsidy control	View answers
QUANTONOVA LIMITED (Lead)	Subsidy control	View answers

Application team

QUANTONOVA LIMITED (Lead)

Organisation details

Type	Business

Team members

Full name	Email	EDI survey
Sureshkumar Sooraj	quantonova@gmail.com	Complete
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Nazia Hameed (pending for 1 days)	nazia.hameed@nottingham.ac.uk	Incomplete

MEDIPROSPECTSAI LIMITED

Organisation details

Type	Business

Team members

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TRACKGENESIS LIMITED

Organisation details

Type	Business

Team members

Full name	Email	EDI survey
Rajesh Kumar	trackgenesis22@gmail.com	Complete

Application details

Competition name
Developing Semiconductor Hardware For Critical Technologies

Application name
OpenPDK: AI-Enhanced Process Design Kit Accessibility and Optimisation for Low-Power RISC-V Edge AI Hardware

When do you wish to start your project?
1 September 2025

Project duration in months
6 months

Has this application been previously submitted to Innovate UK?
No

Research category

Selected research category
Feasibility studies

Project summary

Project summary

OpenPDK is an innovative **AI-powered** design assistant and optimisation platform aimed at significantly enhancing the accessibility and efficiency of semiconductor design for UK SMEs. The project addresses critical barriers faced by small-scale chip developers, particularly the complexity and inaccessibility of advanced **Process Design Kits (PDKs)**. It integrates two groundbreaking technologies: a natural language interface powered by **Large Language Models (LLMs)** and an **AI-based** optimisation engine targeting ultra-low-power semiconductor designs, specifically for **RISC-V** edge AI hardware.

The natural language interface component of **OpenPDK** allows designers without deep foundry-level expertise to seamlessly interact with complex PDK documentation. Leveraging advanced LLMs fine-tuned on semiconductor-specific datasets, designers will be able to pose queries such as, "What are the spacing rules for power rails at this node?" or "Generate simulation scripts for low-leakage memory cells." This drastically reduces the learning curve and accelerates the design process, making advanced semiconductor nodes accessible to a broader range of UK innovators.

Parallel to the LLM interface, the AI optimisation engine applies state-of-the-art machine learning techniques, such as reinforcement learning and genetic algorithms, to refine transistor-level parameters and standard cell libraries. The optimised components are rigorously benchmarked for Power, Performance, and Area (PPA), focusing explicitly on real-world workloads typical of RISC-V edge AI applications. These optimised cells are tailored to emerging low-power nodes such as FD-SOI, ensuring that UK semiconductor designers achieve the highest possible efficiency and performance in their chip designs.

The combined impact of OpenPDK's dual approach addresses both usability and performance optimisation, presenting a unique solution unmatched by current proprietary tools like Synopsys DSO.ai or Google's AI floorplanner. By making advanced semiconductor technologies accessible and optimised for SMEs, the project aligns closely with Innovate UK's strategic goals- reducing reliance on

foreign design ecosystems, enhancing chip design productivity, and fostering national semiconductor innovation.

Key anticipated outcomes of this feasibility study include:

- A fully functional prototype of the LLM-based PDK assistant
- Optimised standard cell libraries validated through benchmarking
- Detailed simulation reports demonstrating measurable PPA improvements
- Comprehensive feedback from SME stakeholders and a clear roadmap for broader adoption

Ultimately, OpenPDK will empower UK SMEs, catalyse innovation in critical technologies such as edge AI and IoT, and significantly enhance national competitiveness in the global semiconductor industry.

Public description

Public description

OpenPDK is a feasibility study exploring how artificial intelligence can make advanced semiconductor design tools more accessible to small and medium-sized enterprises (SMEs) across the United Kingdom. The project aims to reduce the complexity and exclusivity of Process Design Kits (PDKs), which are essential for creating custom chips using modern semiconductor technologies. These PDKs are typically provided by foundries and contain detailed models, layout rules, and simulation data, but they are often inaccessible to organisations without deep technical expertise in electronic design automation.

Many UK-based startups and research teams are actively developing technologies for artificial intelligence, edge computing, and the Internet of Things. However, their ability to create custom silicon is often limited by the steep learning curve and closed nature of traditional chip design processes. OpenPDK directly addresses this challenge by investigating how natural language interfaces and machine learning techniques can make PDKs more user-friendly and performance-optimised.

The first part of the project involves creating an intelligent design assistant based on a Large Language Model (LLM). This assistant will allow chip designers to engage with PDK documentation using everyday language. For example, they could ask questions such as "Which standard cells are best for low-power applications?" or "How can I simulate a memory block using this technology node?" This natural-language capability will simplify access to PDK knowledge and help smaller design teams operate more independently.

In parallel, the project will develop an AI-based optimisation engine that refines standard cell libraries and device models for energy-efficient performance. Using techniques like reinforcement learning and evolutionary algorithms, the system will

explore new configurations that reduce power consumption, increase processing speed, and optimise silicon area. These improvements will be tailored to open architectures such as RISC-V, which are gaining traction in edge AI and embedded systems.

The outcomes of OpenPDK will include a working prototype of the language-based assistant, a set of optimised cell libraries, simulation results demonstrating performance gains, and feedback from UK chip developers. By focusing on usability and practical design efficiency, the project aims to lower the barriers to semiconductor innovation and enable a wider range of organisations to participate in the UK's growing chip design ecosystem.

Ultimately, OpenPDK supports national ambitions to increase technological resilience, foster innovation, and enhance sovereign capabilities in critical semiconductor technologies.

Scope

How does your project align with the scope of this competition?

The OpenPDK project is firmly aligned with the scope and objectives of the "Developing Semiconductor Hardware for Critical Technologies" competition. This feasibility study addresses key challenges in semiconductor hardware development by improving accessibility, productivity, and design efficiency for UK-based organisations engaged in the creation of energy-efficient, high-performance chips. It directly supports critical technology areas such as edge AI, IoT, and next-generation compute by enabling more effective use of advanced Process Design Kits (PDKs).

The project focuses on two tightly integrated innovation strands:

- **Natural language interface for PDKs**: A Large Language Model (LLM)-powered assistant will make complex design rules and simulation models easier to understand and interact with, especially for SMEs and academic researchers who may not have in-house EDA specialists.
- **AI-driven PDK optimisation**: A machine learning framework will refine standard cells and device-level parameters to improve performance metrics such as power, area, and speed, specifically targeting ultra-low-power RISC-V core designs for edge AI workloads.

These focus areas are fully aligned with the competition's targeted outcomes, particularly:

- **Development of Process Design Kits (PDKs)**: OpenPDK aims to enhance both usability and performance of PDKs for advanced nodes, creating a more inclusive design environment for UK chip developers.

- **Semiconductor fabrication and back end of line processes**: The optimisation work will explore how transistor-level design and cell layout parameters can be fine-tuned to match the characteristics of modern semiconductor platforms like FD-SOI, supporting manufacturing efficiency and improved thermal management.
- **Multi-technology integration**: By bridging natural language models with electronic design automation (EDA) flows, the project facilitates new interaction modes between AI systems and traditional design toolchains, enabling hybrid approaches that can be extended to additional design domains.

In addition to the technical fit, OpenPDK also reflects the competition's emphasis on supporting UK SMEs. By focusing on accessibility, the project will lower the entry barriers that currently prevent smaller organisations from contributing to chip design innovation. The project is UK-led, with all activities conducted domestically, and intends to create reusable outputs that benefit the broader national ecosystem.

Finally, this feasibility study will provide concrete data on design performance, user engagement, and toolchain compatibility, building the foundation for scalable adoption of AI-enhanced design workflows across the UK semiconductor sector. In doing so, OpenPDK supports the strategic vision of strengthening UK capabilities in semiconductor hardware for critical technologies.

Application questions

1. Applicant location (not scored)

Applicant location (not scored)

Answer yet to be provided

2. Animal testing (not scored)

Will your project involve any trials with animals or animal testing?

No

3. Permits and licences (not scored)

Permits and licences (not scored)

Yes

4. Need or challenge

What problems or opportunities will your project address relating to UK semiconductor hardware development supporting the critical technologies?

The main motivation behind the OpenPDK project is to address a **critical accessibility** and **productivity gap** in the UK's semiconductor design ecosystem. While the demand for specialised chips in edge AI, IoT, and next-generation compute continues to grow, many UK-based startups, SMEs, and research institutions face significant challenges in **designing silicon** at advanced technology nodes. One of the primary barriers is the complexity and limited usability of Process Design Kits (PDKs), which are essential for chip development but often remain difficult to interpret, navigate, or optimise without specialist expertise. Moreover, as AI chips grow in complexity, with pin counts expected to rise from 22,000 to over 80,000, testing becomes a major bottleneck, further highlighting the need for intelligent, PDK-level design optimisation to reduce downstream fabrication and validation challenges.

This problem is especially acute for fabless semiconductor startups, university spinouts, and design consultancies that lack full-time electronic design automation (EDA) teams. Despite having strong application-level innovations, these groups are often excluded from meaningful participation in chip development at energy-efficient nodes like FD-SOI or at the architectural level using RISC-V. OpenPDK seeks to remove these constraints by creating AI-enhanced design tools that lower

technical entry barriers and enable broader adoption of advanced-node design capabilities.

From a market opportunity perspective, there is growing global interest in the intersection of AI and semiconductor design. Existing tools such as **Synopsys DSO.ai** and Google's floorplanning AI have demonstrated early success but remain expensive, proprietary, and focused on large enterprises. They do not address the specific needs of UK SMEs nor the critical issue of making **PDK documentation** and standard **cell librarie**s more user-friendly. Moreover, most of these innovations focus on floorplanning or layout stages and not on enabling better access to or optimisation of PDK components.

To explore and validate this opportunity, we have already undertaken several preparatory activities:

- Conducted technical feasibility analysis using **open-source PDKs** such as **SKY130** and **NIST 180nm**
- Interviewed UK-based chip developers and academic researchers who highlighted PDK usability as a major blocker and produced a white paper.
- Carried out small-scale experiments on LLM fine-tuning with semiconductor-specific documentation

These early findings confirm the need for a more accessible, intelligent interface to engage with PDKs and a parallel AI-based approach to co-optimise cell libraries for low-power applications.

Post-pandemic supply chain vulnerabilities and the UK Government's National Semiconductor Strategy have highlighted the urgency of developing sovereign design capabilities. Environmental goals and incoming efficiency regulations further increase the relevance of low-power chip design tools. OpenPDK directly responds to these pressures by proposing a feasible, scalable, and innovation-led solution.

5. Approach and innovation

What approach will you take, where will the focus of the innovation be and how will this support semiconductor hardware development for the critical technologies?

OpenPDK will address the critical challenges in semiconductor design accessibility and optimisation through a two-track innovation strategy that merges natural language processing with AI-driven design optimisation. This structured approach responds directly to the needs of UK SMEs and academic teams working on advanced, energy-efficient chips by providing tools that simplify design processes and enhance silicon efficiency.

The first component of our approach is the development of a Large Language Model (LLM)-powered PDK assistant. We will fine-tune open-source LLMs using domain-specific corpora, including simulation languages (such as SPICE, Verilog, and Tcl), layout rules, and foundry documentation. This assistant will allow users to input natural language queries like "What is the minimum spacing for metal layers in this node?" or "Generate a simulation script for SRAM leakage testing." The assistant will interpret and respond with actionable design insights or code snippets, effectively bridging the gap between human intent and complex electronic design automation (EDA) documentation.

The second component is an AI-based optimisation engine. This will utilise reinforcement learning and genetic algorithms to tune transistor-level parameters and standard cell designs for ultra-low-power applications. Cells will be iteratively simulated and benchmarked for Power, Performance, and Area (PPA) using open and commercial toolchains. These enhancements are specifically targeted at RISC-V cores and edge AI workloads, offering a level of optimisation rarely seen in open-access toolsets.

Our team brings over a decade of combined expertise in AI-driven design automation, digital VLSI design, and semiconductor R&D. We have previously delivered machine learning-based optimisation engines and participated in international chip design collaborations. This background equips us with the technical capability and systems knowledge required to successfully execute the OpenPDK vision.

OpenPDK advances the semiconductor sector by introducing a disruptive, inclusive approach to PDK utilisation. Current tools from large vendors focus on physical layout and are cost-prohibitive for smaller teams. Our innovation provides accessible entry into early-stage design and parameter tuning, enabling high-performance custom silicon development with minimal overhead.

We have full freedom to operate based on our use of:

- Public domain LLMs such as Mistral and Llama
- Open-access PDKs including SKY130 and NIST 180nm
- Open-source EDA frameworks like OpenROAD and Qflow

Expected outcomes of the project include:

- A working prototype of the LLM-based PDK assistant
- A validated set of optimised standard cells
- Reports on commercial feasibility and performance benchmarking

These outputs will support wider adoption of AI-enhanced design workflows and strengthen the UK's capacity in critical semiconductor technologies.

6. Team and resources

Who is in the project team and what are their roles?

The **OpenPDK** project will be delivered by a cross-disciplinary team of experts in AI, semiconductor design, and EDA tooling, supported by strategic collaborations with external organisations for simulation and foundry process alignment.

Core Project Team

Key Team Members:

- **Sureshkumar Sooraj: Principal Investigator:** Electronics and Semiconductor Expert: He has 8 Years+ experience in semiconductor PDK areas. He successfully led an Innovate UK project called QuantoTrace- an error correction platform using quantum computing. He will be the project lead. Oversees delivery, project coordination, and partner alignment. Brings 10+ years' experience in AI-enabled system design and research project leadership.
- **Mahmuda Akhter:** She will be the project manager and will communicate with the monitoring officer. She led the "Canvas of Hope" project earlier, funded by Innovate UK, and is also actively part of the PQSHIFT project reviewers.
- **Abrar Fahim:LLM/NLP Engineer:** He will specialise in fine-tuning large language models and domain-specific AI integration. Will lead the development of the natural language PDK assistant, trained on EDA and fabrication rule corpora.
- **Ahmed Khaled: EDA Toolchain Engineer:** With prior experience in Cadence, Synopsys, and OpenROAD environments, this role ensures compatibility of PDK outputs with commercial and open-source workflows.
- **Muhammad Mahfuzur Rahman: PDK Optimisation Lead:** He has experience working in successful Innovate UK projects and will apply reinforcement learning and genetic algorithms to explore power-performance trade-offs. Will own the AI co-design engine for standard cell libraries.
- **One RA** will be recruited.
- **Two Existing research interns** will work full-time on this project to support the senior engineers and collaborate with the other team members.
- **Ben Heinemann: Commercialisation Expert:** Ben has supported over **45 brand launches** in more than **45 countries**, including high-impact roles with Procter & Gamble and Grey, where he oversaw global brand growth and secured over **$150 million** in new business. For the past decade, Ben has acted as an expert in **Horizon Europe** programmes, advising on **IoT, health, and environmental technologies**, and helping raise over **€15 million** in funding for innovation consortia.

In OpenPDK, Ben leads the commercialisation strategy, focusing on market validation, SME engagement, and exploitation planning to ensure that AI-driven semiconductor tooling reaches viable UK and international audiences. His cross-

sector expertise and advisory roles across Asia, Europe, and Africa position him as a key enabler in translating technical innovation into real-world uptake.

- **MCS DataLab: Semiconductor Design Consultant (Subcontractor):** from Germany will be led by a specialist with hands-on expertise in FD-SOI and RISC-V SoC layout. The specialist will validate cell library functionality and contribute to benchmarking activities.

Advisory Group:

- **Dr Marzia Tania:** Advisor: She is a postdoc in the Machine learning research group at the University of Oxford. She will guide us in the ML integration for the Cloud platform and the integration of error handling techniques.
- **Sakibul Islam:** Advisor: He is pursuing a Ph.D. at the University of New Mexico, NM, USA in the Electrical and Computer Science Engineering program. He is working at Nanometa Lab.
- **Dr M Mahmudul:** Consultant: He is an expert in building data-driven AI products.

Collaborating Organisations and Resources

- **Knowledge Partners**: **Dr Nazia Hameed** from Nottingham University and **Dr Monjur Showkat** from Imperial College London will be advising time to time to
- **EDA Vendor Partner (TBC)**: May provide evaluation access to simulation environments (e.g., Genus, Virtuoso) for PDK validation and commercial viability testing.
- **Cloud Resource Provider**: Compute infrastructure for LLM fine-tuning and simulation runs will be provisioned via AWS or Google Cloud, with GPU/TPU access for training and model inference.
- **Facilities and Tools**
- Source control and devops will be managed via **GitLab** with CI/CD integration for reproducible flows.
- LLM training will use pre-trained models hosted in secure environments with containerised environments for reproducibility.
- Layout and simulation will occur in both **open-source (OpenROAD, Qflow)** and **commercial EDA toolchains**, where licensing permits.**New Roles to Recruit**
- **AI Research Assistant (Junior)**: To assist in dataset creation, annotation, and LLM fine-tuning.
- **EDA Toolchain Intern (optional)**: To support testing workflows and open-source compatibility efforts.

The project builds on existing collaborations and will strengthen partnerships across academia and industry. It also lays the groundwork for future joint R&D and IP licensing efforts.

7. UK semiconductor market awareness

What does the market or markets you are targeting look like?

OpenPDK targets a strategically important and fast-evolving segment of the semiconductor ecosystem: AI-enabled design automation for advanced-node chip development, specifically tailored for low-power RISC-V-based architectures and edge AI workloads. **Our primary market includes UK-based fabless semiconductor SMEs, academic research groups, and design consultancies who face significant challenges accessing and utilising Process Design Kits (PDKs) for custom silicon design.**

There are over 100 active fabless (e.g., **EnSilica, Picocom, Ransemi ARM**) design entities across the UK, many of which are constrained by limited access to advanced EDA tools, high software licensing costs, and a shortage of skilled engineers trained to work with complex PDKs. These organisations often rely on legacy nodes or design IP sourced from external providers, limiting innovation and value capture. OpenPDK responds to this bottleneck by offering an open, AI-augmented solution that enables natural language access to PDK data and automatic tuning of standard cell libraries for ultra-low-power applications.

The global Electronic Design Automation (EDA) market was valued at approximately £8.2 billion in 2023 and is expected to reach more than £15 billion by 2030, with growth driven by AI, automotive, and custom edge computing hardware (Allied Market Research, 2023). Within this space, the RISC-V architecture is experiencing rapid adoption due to its open standard, with the market forecast to grow at over 20% CAGR and exceed £1.4 billion by 2030 (Semico Research, 2023).

The current market is heavily centralised around p**roprietary, high-cost offerings from vendors like Synopsys, Cadence, and Siemens**. These toolchains cater to large design houses and are rarely optimised for SMEs. Moreover, current AI integrations focus on physical layout (e.g., floorplanning), not on early-stage PDK usability or standard cell co-optimisation. OpenPDK shifts this paradigm by introducing AI into the entry point of the design process, where it can have the highest impact for lean teams.

Key technical enablers include:

- Open-access PDKs such as SKY130 and NIST 180nm
- OpenROAD and Qflow as backend simulation and synthesis environments
- Integration of LLMs for SPICE, Verilog, and design rule interpretation

Internationally, we anticipate parallel demand in EU-aligned markets, our German (MCS) and French (irt-systemx), partners' North American academic labs, and emerging sovereign chip initiatives. The project will validate these market

opportunities through pilots, benchmark demonstrations, and engagement with open silicon consortia.

By making advanced chip design more accessible, OpenPDK will help position the UK as a leader in AI-enhanced semiconductor tooling and design capability.

8. Outcomes

How are you going to grow your business and increase long term productivity as a result of the project?

OpenPDK positions us to establish a foothold in the emerging and under-served niche of AI-enabled semiconductor design tools, with a specific focus on PDK usability and optimisation for fabless startups and SMEs. Currently, the market is dominated by large EDA vendors offering proprietary, high-cost solutions that are inaccessible to most UK-based small-scale chip developers. This project enables us to introduce a new product category that combines AI assistance, natural language accessibility, and low-power design optimisation with real-world applicability.

We are currently active in AI-driven design automation and early-stage semiconductor tool research. OpenPDK will expand our capabilities into the PDK enablement layer, providing a differentiated offering that builds upon our existing work. Our target users include:

- Fabless chip startups aiming to reduce development time, cost, and risk
- Research teams developing custom SoCs or novel chip architectures
- Design service providers supporting early-stage or low-volume silicon prototyping

Value to users is delivered through easier access to advanced PDKs, improved productivity in chip design workflows, and the ability to generate highly efficient RISC-V-based low-power cores optimised for edge AI applications. These users would benefit from significantly reduced time-to-tapeout and lower engineering overhead.

We expect to generate commercial revenue through:

- Licensing of optimised standard cell libraries to design houses and universities
- Offering the LLM-based PDK assistant as a SaaS tool or desktop utility
- Providing integration and consulting services for onboarding and workflow adaptation

This innovation will also help reduce our internal development costs, accelerate IP creation, and increase investor confidence in future spinouts. The project allows

us to extend our business from niche AI tools to full-stack design enablement, with a clear technical roadmap and scalable model that meets emerging demand.

Looking beyond RISC-V and FD-SOI, we plan to expand our scope into:

- Photonics-PDK co-design for quantum and sensing chips
- Cloud-based integration with third-party EDA platforms
- Engagement with UK and EU foundries to support open PDK standardisation and interoperability

Our strategy to target these markets includes early pilot deployments with UK SMEs, co-development with academic partners, presentations at industry conferences, and active engagement with open silicon communities. We will build traction through demonstrator trials, licensing partnerships, and performance case studies.

Overall, OpenPDK will generate research and commercial outcomes that support UK priorities in semiconductor innovation, energy-efficient computing, and sovereign design capability. It will lay a sustainable foundation for future growth, skill development, and global competitiveness.

9. Wider impacts

What impact might this project have outside the project team?

The OpenPDK project will deliver a range of wider impacts that extend well beyond the immediate project team. These include measurable benefits to external customers, supply chain stakeholders, the UK semiconductor industry, and the broader innovation ecosystem.

From an economic standpoint, the project will increase productivity for UK SMEs and research institutions by reducing the time and expertise required to design chips using advanced nodes. By simplifying the interaction with Process Design Kits and automating standard cell optimisation, chip developers can reduce design cycles by several weeks, lowering development costs and time-to-market. This productivity gain enables more frequent prototyping and fosters a more agile innovation culture within UK semiconductor firms.

Additionally, OpenPDK will contribute to import substitution by enabling UK organisations to rely less on expensive, overseas-provided EDA tools and consultancy services. This helps retain value within the UK economy, especially among emerging fabless companies that currently depend on foreign vendors for IP libraries and tooling support.

The project also strengthens the UK's semiconductor supply chain by stimulating demand for domestic EDA services, local foundry collaboration, and chip packaging providers. It promotes interoperability with open-source PDK flows and

reinforces sovereign capabilities aligned with the UK Government's National Semiconductor Strategy.

Key environmental impacts are also expected. By developing AI models that optimise power and area efficiency in chip designs, OpenPDK supports the design of lower-energy, higher-efficiency hardware. This contributes to long-term reductions in carbon emissions across deployed edge devices in sectors such as healthcare, agriculture, transport, and consumer IoT. The project will also encourage a more sustainable approach to compute infrastructure through energy-aware design practices.

Regionally, OpenPDK will support high-value job creation and innovation activity across key semiconductor clusters in the UK, particularly in Cambridge, Bristol, and South Wales. These regions host a growing base of fabless design firms and universities, which stand to benefit from project outputs and future collaboration opportunities.

From a social perspective, the project will contribute to:

- Creation of technical and research roles in AI, chip design, and software engineering
- Academic access to tools for training the next generation of chip designers
- Increased participation of under-represented groups by lowering entry barriers to complex design tools
- Public empowerment through future open-access tooling and documentation

OpenPDK will enhance inclusion, improve design accessibility, and promote a more diverse and competitive semiconductor ecosystem across the UK. These broader impacts align with national priorities in innovation, skills development, and economic resilience.

10. Project management

How will you manage your project effectively?

To ensure effective delivery of OpenPDK, we will adopt a structured project management approach combining agile development cycles with milestone-based tracking. This enables flexibility during technical implementation while ensuring accountability and timely progress across the six-month project period. A core coordination team will manage planning, delivery, monitoring, and risk mitigation, with clear ownership assigned to each work package and milestone.

Work Packages and Timeline

WP1: Project Initiation and Architecture Planning (Month 1)

- Finalise system architecture and delivery plan

- Set up cloud infrastructure and dev tools (e.g. GitLab, AWS)
- Secure open-source PDKs (SKY130, NIST 180nm)
- Onboard the team and define project workflows
- Establish documentation and reporting templates

WP2: LLM-Based PDK Assistant Development (Months 1--3)

- Build a domain-specific corpus from PDK documents
- Implement retrieval-augmented generation (RAG) search
- Adapt/fine-tune LLMs for PDK query handling
- Develop a prompt interface for rule lookup and script generation
- Test with real-world chip design queries

WP3: AI-Based Standard Cell Optimisation (Months 2--4)

- Develop RL/genetic algorithms for standard cell tuning
- Optimise for low-power edge AI (RISC-V)
- Run simulations to evaluate PPA (power, performance, area)
- Generate and compare cell variants
- Maintain compatibility with FD-SOI and 180nm nodes

WP4: Benchmarking, Validation, and Integration (Months 4--5)

- Validate optimised cells using OpenROAD/Qflow flows
- Benchmark results against baseline PDK cells
- Ensure compatibility with EDA toolchains
- Refine models and document reproducibility
- Finalise design flow integration

WP5: Dissemination, Exploitation, and Final Reporting (Month 6)

- Gather feedback from SMEs and academic advisors
- Compile final technical and feasibility reports
- Develop IP and commercialisation strategy
- Share results through demos and pilot engagement
- Deliver final outputs to Innovate UK

Project Management Tools and Mechanisms

- **ClickUp** for milestone planning, dependency tracking, and Gantt charts
- **GitLab** for CI/CD pipelines, version control, and reproducible builds
- **Obsidian** for technical documentation, decision logs, and collaborative knowledge management

- **Slack and Google Meet** for real-time coordination, stand-ups, and stakeholder meetings
- **Jira** for agile issue tracking and team workload management (internally)
- Monthly internal reviews and bi-monthly steering updates will ensure timely alignment and risk control

Management Structure and Dependencies

The Project Lead and Manager will oversee daily operations, with technical leads reporting to WP. Dependencies are mapped across WPs --- WP1 enables WP2--3; WP3 feeds WP4; and validated results in WP4 inform WP5 outputs. This structured yet flexible plan ensures smooth delivery of technical and strategic outcomes.

11. Risks

What are the main risks for this project?

1. LLM domain underperformance (Technical)
There is a genuine risk that general-purpose LLMs will struggle to interpret or generate accurate responses for semiconductor-specific queries, particularly in SPICE/Verilog syntax or design rule terminology.

Mitigation: During the feasibility phase, we will rely on a retrieval-augmented generation (RAG) framework instead of freeform generation. The LLM will be constrained to answer from validated context extracted from SKY130 and NIST PDK documents. Fine-tuning will be limited to domain-cleaned datasets only. Evaluation metrics will focus on factual precision, not fluency.

2. Inconsistent benchmarking of optimised cells (Technical)
Optimised standard cells may behave inconsistently across different EDA flows, especially when ported between OpenROAD, Qflow, or commercial environments.

Mitigation: All benchmarking will use a fixed reference circuit suite. Results will be validated in parallel across open-source and commercial tools, with mismatches flagged early. The subcontractor (MCS DataLab) will perform functional checks using FD-SOI flows where relevant.

3. GPU/TPU resource limitations (Resource)
LLM fine-tuning and simulation workloads are GPU-intensive. Public cloud resources (e.g. AWS spot instances) are not guaranteed and may delay training or simulation.

Mitigation: We have secured scheduled access to a dedicated A100-class GPU workstation via our university research partner, ensuring reliable compute for LLM fine-tuning and simulations. Tasks will be pre-scheduled in batches, and smaller

models (e.g. Mistral-7B) will be used early to reduce training time and avoid bottlenecks.

Critical project inputs:

- **Open-source PDKs**: SKY130 and NIST 180nm are essential to model rules, generate libraries, and validate simulations.
- **EDA tools**: OpenROAD, Qflow, and selected commercial tools (under evaluation license) are required to run and validate designs.
- **Expertise**: Access to domain specialists in layout optimisation, LLM integration, and simulation flows is fundamental---secured through the project and subcontractor teams.

Regulatory and ethical considerations:

No personal data is used, and the project does not involve human-facing AI outputs or safety-critical systems. However, there is a minor risk that downstream applications (e.g. optimised standard cell libraries) could be reviewed under export control or critical technology frameworks, particularly if integrated into high-performance or defence-related systems.

To manage this, all outputs will be documented with full traceability, including version control, authorship, and origin of source data. The LLM assistant will include clear disclaimers and will be explicitly positioned as a decision-support tool, not an autonomous design engine. Only qualified semiconductor professionals will be the intended users.

OpenPDK_Risk_Register_Appendix.pdf (opens in a new window) (/application/10163239/form/question/46940/forminput/132465/file/824602/download).

12. Added value

How will this public funding help you to accelerate or enhance your approach to developing your project towards commercialisation? What impact would this award have on the organisations involved?

Public funding is critical to accelerate the development and de-risk the early stages of the OpenPDK platform, which integrates artificial intelligence with advanced semiconductor design processes. The project includes foundational activities such as fine-tuning large language models, optimising standard cell libraries through machine learning, and integrating these innovations with real-world electronic design automation (EDA) workflows.

This grant will allow us to:

- Rapidly build and test a minimum viable product for AI-assisted PDK interaction

- Conduct rigorous benchmarking of AI-optimised standard cells using real-world edge AI workloads
- Engage UK-based SMEs and research teams in pilot trials
- Strengthen partnerships with universities and cloud EDA service providers

These activities are essential to validating our technical approach and generating early traction in the UK semiconductor sector. With Innovate UK support, we can accelerate delivery timelines, reduce risk, and strengthen our appeal to future investors and commercial partners.

We have explored private equity and accelerator funding, but these routes are not well-suited to pre-revenue, deep-tech feasibility studies. Most commercial investors require demonstrable traction or IP, which this project will help deliver. We have also engaged with university innovation offices, but their support is limited to academic IP protection and incubation.

Without public funding, this project would be delayed significantly and reduced in scope. Development would be limited to exploratory internal research, lacking the scale or validation required to meet SME and academic needs. The absence of structured pilot testing would also limit our ability to produce reusable tools and benchmarks, delaying commercialisation by at least 12 to 18 months.

The Innovate UK grant will be used in combination with in-kind contributions from academic partners, including access to open PDKs, research compute infrastructure, and design expertise. The lead applicant will provide the remaining 20 percent of the project costs through internal resources and reinvested revenues from previously commercialised AI toolsets.

The impact of the project on all involved organisations will be significant. The lead partner will establish a strategic position in semiconductor design enablement. Academic collaborators will gain a platform for applied research translation and education. Subcontractors will participate in benchmarking and validation activities that position them for further industry engagement. This public investment is essential to delivering high-value outcomes, building sovereign design capabilities, and positioning the UK at the forefront of AI-assisted chip design.

13. Costs and value for money

How much will the project cost and how does it represent value for money for the team and the taxpayer?

The total eligible project cost is **£250,000**, for which we are requesting an **Innovate UK grant of £200,000**. The remaining **£50,000 (20%)** will be contributed by the lead applicant and delivery partners, through a combination of internal resource commitment, matched funding, and access to existing capital infrastructure.

Cost Breakdown and Partner Contributions

- **Lead applicant** will cover project management, LLM fine-tuning, and integration activities. This includes cash and in-kind support from existing engineering staff and cloud infrastructure credits.
- **University/research partner** will contribute compute access, simulation tooling, and PDK research assets in-kind, helping to reduce capital costs.
- A key **subcontractor** will provide expert input on cell-level benchmarking and EDA tool compatibility---critical to ensuring the optimised libraries are viable for UK fabless designers. The subcontractor budget is **£35,000**, and this work cannot be replicated in-house due to its specialist nature.

Value for Money for the Taxpayer

This project offers exceptional value to the taxpayer by:

- **Unlocking sovereign design capability** among UK SMEs and academic chip teams---reducing dependence on overseas tooling and services.
- Creating a **reusable AI toolset and optimised library IP** that can benefit a wide range of UK technology developers long after the feasibility study ends.
- Leveraging public investment to **attract future private capital**---including SaaS revenue models, licensing opportunities, and co-development partnerships.

The cost per output (e.g., trained LLM assistant, optimised PDK library, benchmarking data, and market readiness analysis) is modest when compared to the typical investment needed to develop even a basic ASIC flow.

Opportunity Cost and Justification

Without this project, the same funds would likely go toward exploratory R&D with limited IP outcomes and minimal market validation. OpenPDK offers a focused, de-risked path to innovation that:

- Directly responds to a market gap,
- Demonstrates commercial relevance in AI chip design,
- Delivers clear outputs aligned with Innovate UK's strategic aims.

The cost split across partners is balanced and transparent, ensuring no single party is over-leveraged. Each cost line item is directly tied to project delivery, technical feasibility, or commercial impact, reflecting a lean and accountable use of public funds.

The finances of all project partners are included in this summary.

Return to your project finances (/application/10163239/form/section/19120/) to complete or make changes to your organisation's financial information.

	Total costs (£)	Funding level (%)	Funding sought (£)	Contribution to project (£)	Other public sector funding (£)
QUANTONOVA LIMITED Lead organisation	**150,105**	70.00	105,074	45,032	0
MEDIPROSPECTSAI LIMITED Partner	**49,999**	70.00	34,999	15,000	0
TRACKGENESIS LIMITED Partner	**29,276**	70.00	20,493	8,783	0
Total	**£229,380**		160,566	68,814	0

Funding breakdown

	Total	Labour (£)	Overheads (£)	Materials (£)	Capital usage (£)	Subcontracting (£)	Travel and subsistence (£)	Other costs (£)
QUANTONOVA LIMITED Lead organisation View finances (/application/10163239/form/FINANCE)	**£150,105**	94,828	18,966	3,450	861	32,000	0	0
MEDIPROSPECTSAI LIMITED Partner	**£49,999**	41,666	8,333	0	0	0	0	0
TRACKGENESIS LIMITED Partner	**£29,276**	24,397	4,879	0	0	0	0	0
Total	**£229,380**	160,891	32,178	3,450	861	32,000	0	0

Supporting information

Project impact

Understanding the benefits of the projects Innovate UK supports

These organisations have not completed the project impact survey:
- MEDIPROSPECTSAI LIMITED
- TRACKGENESIS LIMITED

This application cannot be submitted until all partners complete the survey.

Partner	Status
QUANTONOVA LIMITED (Lead)	Complete
MEDIPROSPECTSAI LIMITED	Incomplete
TRACKGENESIS LIMITED	Incomplete

Terms and conditions

Award terms and conditions

The following organisations have not yet accepted:

- MEDIPROSPECTSAI LIMITED
- TRACKGENESIS LIMITED

This application cannot be submitted until all partners accept our terms and conditions.

Partner	Funding rules	Terms and conditions	Stat
QUANTONOVA LIMITED (Lead)	Subsidy control	Innovate UK - Subsidy control (/application/10163239/form/terms-and-conditions/organisation/93776/question/46890)	Acc
MEDIPROSPECTSAI LIMITED	Subsidy control	Innovate UK - Subsidy control (/application/10163239/form/terms-and-conditions/organisation/27504/question/46890)	Not acc
TRACKGENESIS LIMITED	Subsidy control	Innovate UK - Subsidy control (/application/10163239/form/terms-and-conditions/organisation/81098/question/46890)	Not acc