CHITKARA UNIVERSITY

**Sessional III– NOVEMBER, 2017**

**Semester V**

ID No: …… [Total No. Of Pages: 02]

**Time: 90 minutes** **Department:** Computer Science &Engg.

**Title of the Course:**Computer System Architecture **Max. Marks: 40**

**Course Code: CSL 4208**

**Instructions:**

For Section A

- There is one question having five parts. Each part is having four distinct options out of which only one choice will be correct. There is no negative marking for incorrect answers.

For Section B

- There are 6 Questions of 2 marks each. There is a choice to attempt 5 questions out of 6.

For Section C

- There are 4 Questions of 5 marks each. There is a choice to attempt 3 questions out of 4.

For Section D

- There are 2 Questions of 10 marks each. There is a choice to attempt 1 question out of 2.

---

## Section-A

*(All Questions are Compulsory, Each question carries 01 mark)*

1. i) The circuit used to store one bit of data is known as
   a) Register b) Encoder
   c) Decoder d) Flip Flop
   ii) In case of, Zero-address instruction method the operands are stored in _____ .
   a) Registers b) Accumulators
   c) Push down stack d) Cache
   iii) The reason for the implementation of the cache memory is
   a) To increase the internal memory of the system b) The different in speeds of the processor and memory
   c) To reduce the memory access and cycle time d) All of the above
   iv) The DMA differs from the interrupt mode by
   a) The involvement of the processor for the operation b) The method accessing the I/O devices
   c) The amount of data transfer possible d) Both a and c
   v) A word whose individual bits represent a control signal is _____.
   a) Command word b) Control word
   c) Co-ordination word d) Generation word

## Section-B

*(Attempt any 5 questions, each question carries 02 marks)*

2. Derive the flowchart of hardware multiply algorithm.
3. Convert the given expression into reverse polish notation 3+4*[10*(2+6)+8] and evaluate.
4. Draw the space time diagram for six segments showing the time it takes to process eight tasks.
5. How BSA is different from BUN, what are the micro-operations performed during BSA.
6. Which is more preferable RISC or CISC and why?

7. List down at least five data transfer instructions.

## Section-C

*(Attempt any 3 questions, each question carries 5 marks, subparts (if any) carry equal weightage)*

8. Why does DMA have priority over CPU when both requests a memory transfer? Explain with a neat diagram of signal flow while a DMA transfer occurs. 5

9. What is the difference between an instruction and a microinstruction? Explain it in relevance of their respective formats. Is it possible to design a microprocessor without a microinstruction? 5

10. The bus organized CPU has 16 register with 32 bits in each, an ALU, and a destination.
i) How many multiplexers are there in the A bus, and what is the size of each multiplexer?
ii) How many selection inputs are needed for MUX A and MUX B?
iii) How many inputs and outputs are there in the ALU for data, including inputs and output carries? 5

11. What are the hardware components involved in computing signed magnitude addition and subtraction explain with the help of neat diagram. 5

## Section-D

*(Attempt any one question, each question carries 10 marks, subparts (if any) carry equal weightage)*

12. i) Suppose you have a 4-way set associative cache which has in total 4096 bytes of cache memory and each cache line is 128 bytes. How many sets are there is this cache? If memory is byte addressable and addresses are 16 bits then How many bytes are used for the tag? 5
ii) a) How many 128*8 RAM chips are needed to provide a memory capacity of 2048 bytes? 3
b) How many lines must be decoded for chip select? Specify the size of the decoders. 2

13. i) Describe the interrupt cycle in detail with diagram. Also specify the instructions executing during interrupt cycle. 5
ii) The pipeline has following propagation times: 40 ns for the operands to be read from memory into register R1 and R2, 45 ns for the signal to propagate through the multiplier, 5 ns for the transfer into R3, and 15 ns to add the two numbers into R5.
a) What is the minimum clock cycle time that can be used?
b) Calculate the speedup of the pipeline for 10 tasks and again for 100 tasks. 5