AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

[Group Information]

4th Year 1st Semester
Section: D2

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PROJECT PROPOSALS

Project Name: Design of Flip-Flops for High Performance VLSI Applications using Deep Submicron CMOS Technology.

Objective:
This paper delves into the evaluation of low-power, high-speed designs of SET, DET, TSPC, and C2CMOS Flip-Flops at 90nm technology. These compact topologies offer reduced area and power consumption, applicable across digital VLSI clocking systems, buffers, and microprocessors. Using DSCH and Microwind tools, the study compares these Flip-Flops in terms of area, transistor count, power dissipation, and propagation delay. It emphasizes the use of recent CMOS micron layout tools to develop low-power chips, aligning with advancements in chip manufacturing technology. Specifically, the project focuses on True Single Phase Clocking (TSPC) and C2CMOS flip flops, comparing them against existing topologies, analyzing parameters such as area, transistor count, power dissipation, propagation delay, and parasitic values through Microwind simulations.

Circuit Diagrams:

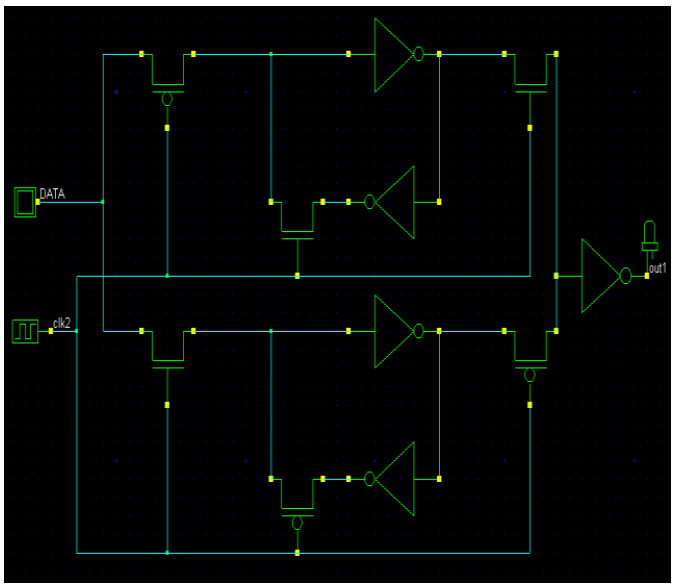

Figure 1: Schematic of DET D flip flop in Dsch.

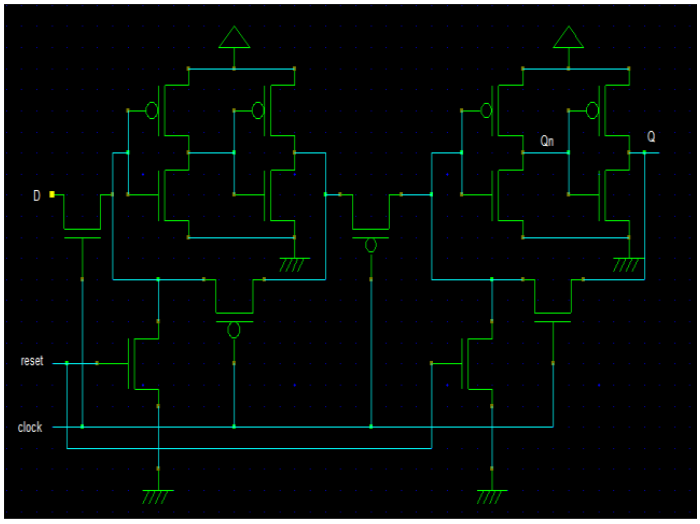

Figure 2: Schematic of SET D flip flop in Dsch.

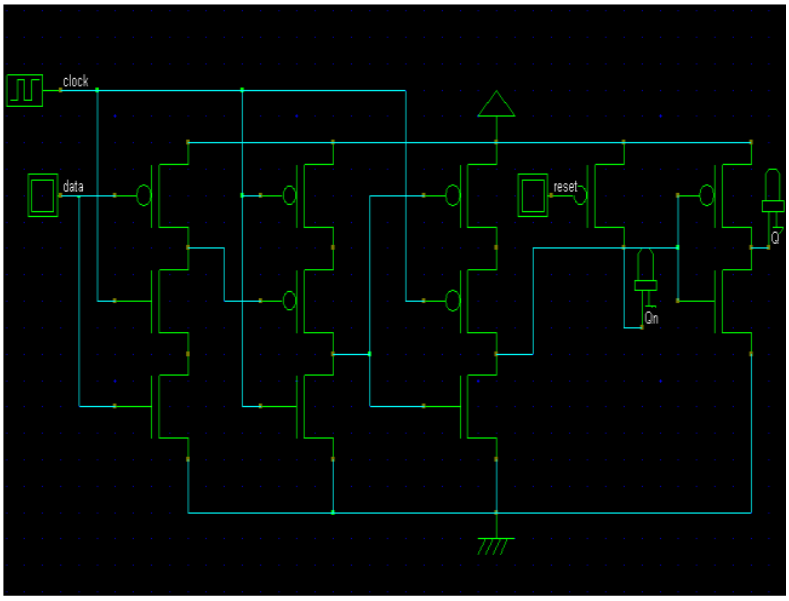

Figure 3: Schematic of SET D flip flop in Dsch.

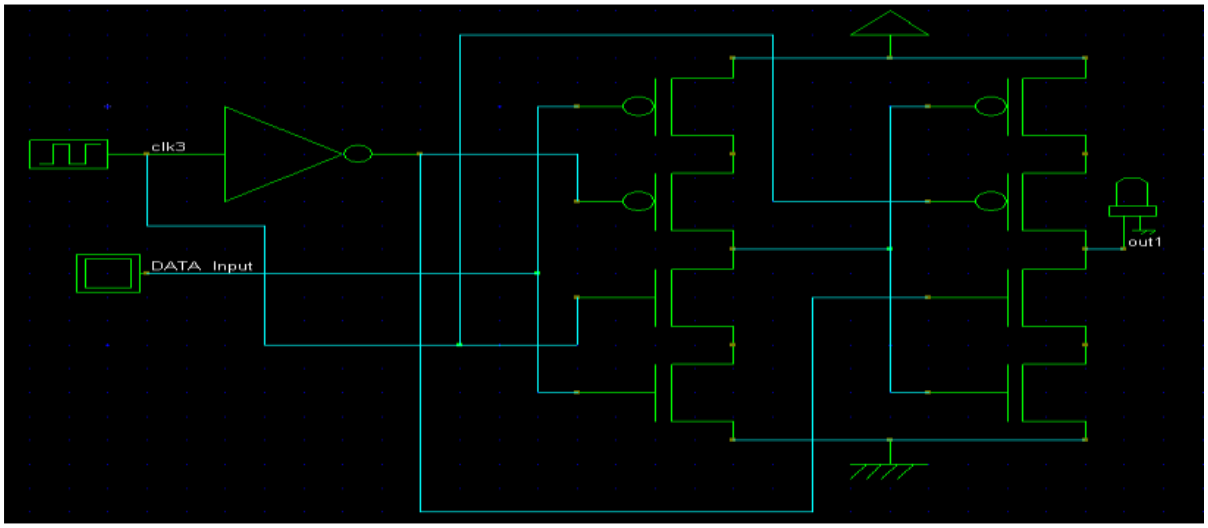

Figure: Schematic of C2CMOS D flip flop in Dsch.

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