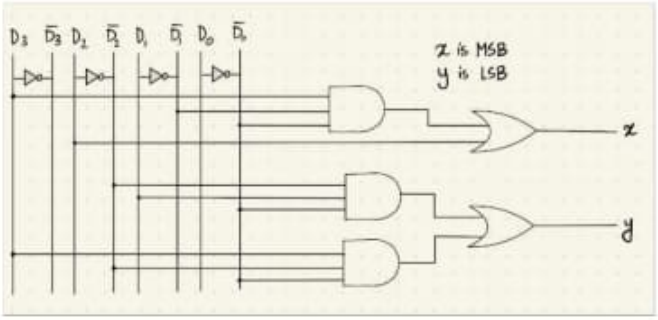
1 Consider the following circuit of priority encoder. What is the correct priority order of the input lines? 1 point



- ○ D1>D2>D0>D3
- ○ D2>D1>D3>D0
- ◉ D2>D0>D1>D3
- ○ D3>D1>D0>D2

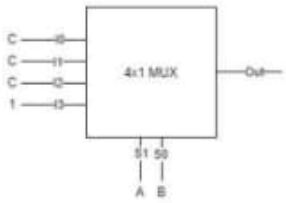
Clear selection

2 The POS form for the function f(A,B,C,D)= ∑m(0,2,4,8,10,14) is 1 point

- ◉ D'(A+B'+C') (A'+B'+C)
- ○ D'(A+B'+C) (A'+B'+C)
- ○ D'(A+B'+C') (A'+B+C)
- ○ D'(A+B'+C') (A+B'+C)

Clear selection

3 Consider the following 4x1 MUX. Here I0-I3 are the input bits and S0-S1 are the two select bits.Which Boolean function does it implement? 1 point



- ○ A'B' + C
- ○ ABC
- ◉ AB + C
- ○ 1

Clear selection

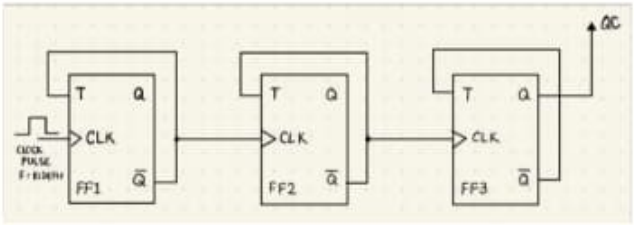
4 Which one of the following is an advantage of an asynchronous counter when compared to a synchronous counter? 1 point

- ○ Less timing delay
- ◉ Easier to implement
- ○ Requires fewer logic elements
- ○ More reliable

Clear selection

- A - 00, B - 11, C – 10, D - 01
- A - 01, B - 10, C – 11, D - 00

5 Consider the following circuit. If the frequency of the input clock pulse is 1024Hz, then what will be the frequency of the signal represented by QC? 1 point



- 128Hz
- 512Hz
- 2048Hz
- 64Hz

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6 Which one below is not a valid state of a 5-bit twisted-ring counter?

- 11100
- 01110
- 00111
- 11110

Clear selection

7 You are given two 2-bit synchronous up counters. You have to design a 4-bit up counter using them. Which one of the following is true? 1 point

- It cannot be done
- It can be done using extra logic gates
- It can be done using another 2-bit up counter
- Both (b) and (c)

8 Which of the following is not a correct property of a moore machine? 1 point

- Asynchronous output and state generation
- Output depends only upon present state
- They react slower to inputs (One clock cycle later)
- If input changes, output does change

Clear selection

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Consider the following circuit of priority encoder. What is the correct priority order of the input lines? 1 point

All of the above Boolean functions can be implemented using a single 4x1 MUX

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9 Which of the following Boolean functions is not equal to F(x,y,z) = Σ(1,2,5,7)? 1 point

- y'z + x'yz' + xz
- x'yz' + x'y'z + xy'z + xyz
- y'z + x'y + xyz
- y'z + x'yz' + xyz

Clear selection

10 The SOP form for the function f(A,B,C,D)= ∑m(0,2,4,8,10,14) is 1 point

- BD' +ACD' +A'C'D'
- B'D +ACD' +A'C'D'
- B'D' +ACD' +A'C'D'
- B'D' +AC'D +A'C'D'

Clear selection

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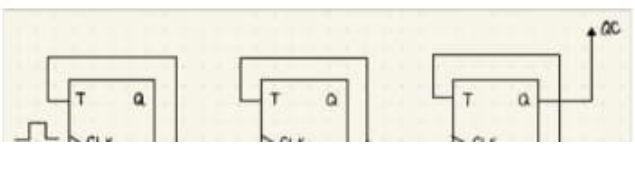
11 Which one of the following is a race free state assignment for the following flow table? 1 point

	00	01	11	10
A	(A),0	D,0	B,-	(A),0
B	A,-	-	C,-	-
C	A,-	(C),1	(C),1	(C),1
D	A,0	(D),0	(D),0	C,-

- A - 00, B - 01, C – 10, D - 11
- A - 01, B - 00, C – 10, D - 11
- A - 00, B - 11, C – 10, D - 01
- A - 01, B - 10, C – 11, D - 00

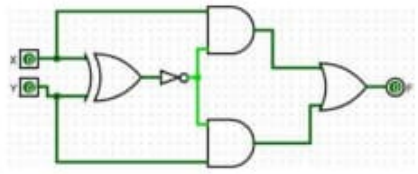
Consider the following circuit. If the frequency of the input clock pulse is 1024Hz, then what will be the frequency of the signal represented by QC? 1 point



- Any boolean function can be implemented using 4x1 multiplexers only.
- Any boolean function can be implemented using 2x1 multiplexers only.
- Any boolean function can be implemented using NOR gates only.
- (●) All of the above statements are true.

Clear selection

12 Which boolean function does the following circuit implement? 1 point



- x'y
- (●) xy
- 0
- x + y'

Clear selection

13 If you want to mimic the behavior of a 35-state ring counter using a module-35 counter, which of the below additional components would suffice? 1 point

- 4-to-16 decoder
- 5-to-32 decoder
- 3-to-8 decoder
- (●) 6-to-64 decoder

Clear selection

14 Which propagation delay mainly limits the speed of a ripple counter? 1 point

- All flip-flops and gates
- Only circuit gates
- (●) Each flip-flop
- None of the above

Clear selection

15 Which of the following boolean function cannot be implemented using a single 4x1 MUX only(not even using any extra NOT gate)? 1 point

- F(a,b,c) = a XOR b
- F(a,b,c) = ab'c
- F(a,b,c) = ab + c'
- (●) All of the above Boolean functions can be implemented using a single 4x1 MUX

Jan 2021 CSE 206 Quiz Section A

Questions

16 You are to convert a decade counter to a Grey counter. What is the minimum number of logic gates required to make the conversion? 1 point

- ○ 2
- ◉ 3
- ○ 4
- ○ 5

Clear selection

17 How many OR gates are required to implement a Decimal to BCD encoder? 1 point

- ○ 5
- ○ 2
- ◉ 4
- ○ 3

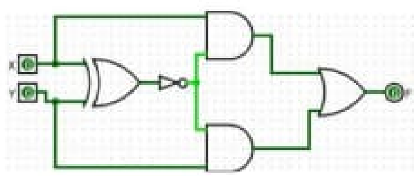
Clear selection

18 Which of the following statement is false (if any)? 1 point

- ○ Any boolean function can be implemented using 4x1 multiplexers only.
- ○ Any boolean function can be implemented using 2x1 multiplexers only.
- ○ Any boolean function can be implemented using NOR gates only.
- ◉ All of the above statements are true.

Clear selection

Which boolean function does the following circuit implement? 1 point



19 A positive edge-triggered D flip-flop will store a 1 when 1 point

- (●) The D input is HIGH and the clock transitions from LOW to HIGH
- ( ) The D input is HIGH and the clock transitions from HIGH to LOW
- ( ) The D input is HIGH and the clock is LOW
- ( ) The D input is HIGH and the clock is HIGH

Clear selection

20 The inputs of a one bit comparator are A and B and the output is Y. Which of the following equations will give the right output for A = B? 1 point

- ( ) Y = AB' + AB
- ( ) Y = A'B' + A'B
- ( ) Y = AB' + A'B
- (●) Y = A'B' + AB

Clear selection

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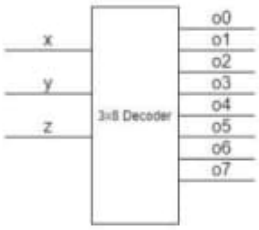
21 Consider the following 3x8 Decoder. Here x,y,z are the decoder inputs and o0 to o7 are the eight decoder output lines. Supposeyou want to implement the boolean function F(x,y,z) = xy + yz. Which output lines need to be ORed toimplement the desired function? 1 point



- ( ) o0, o1, o2, o4, o5
- (●) o3, o6, o7
- ( ) o2, o5, o6
- ( ) o2, o5, o3, o6

Clear selection

22 The logic circuits whose outputs at any instant of time depends not only on the present input but also on the past outputs are called 1 point

- ( ) Flip-flops
- ( ) Combinational circuits
- ( ) Latches
- (●) Sequential circuits

Clear selection

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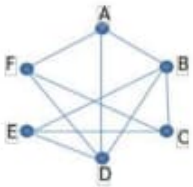
23 In the following Merger Diagram which of the following sets of states is a minimal closed covering. 1 point



- ○ ABDF, CE
- ◉ ADF, BCE
- ○ ADF, BDE
- ○ ABD, CEF

Clear selection

24 Which of the following is not correct for an Encoder? 1 point

- ○ The number of inputs accepted by an encoder is 2^n
- ○ The output lines for an encoder is n
- ◉ AND gate is the basic logic element used in it
- ○ It performs the reverse operation of a Decoder

Clear selection

25 It should be kept in mind that don't care terms should be used along with the terms that are present in 1 point

- ○ Latches
- ○ Minterms
- ◉ K-Map
- ○ Expressions

Clear selection

26 A positive edge-triggered D flip-flop will store a 1 when 1 point

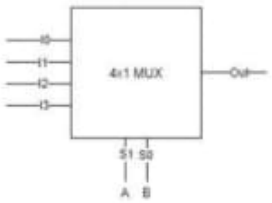
- ◉ The D input is HIGH and the clock transitions from LOW to HIGH
- ○ The D input is HIGH and the clock transitions from HIGH to LOW
- ○ The D input is HIGH and the clock is LOW
- ○ The D input is HIGH and the clock is HIGH

Clear selection

The inputs of a one bit comparator are A and B and the output is Y. Which of the following equations will give the right output for A = B? 1 point

- ○ Y = AB' + AB

27 Consider the following 4x1 MUX. Here I0-I3 are the inputs and S0,S1 are the selection bits. 'Out'is the output line. Suppose you want to implement the Boolean function AB+BC. What inputsshould you give to the input lines? 1 point



- (●) I0 = 0, I1 = C, I2 = 0, I3 = 1
- ( ) I0 = 1, I1 = C, I2 = C, I3 = 1
- ( ) I0 = 0, I2= C, I2 = 0, I3 = C
- ( ) It is not possible to implement AB+BC using a single 4x1 MUX.

Clear selection

28 A basic S-R flip-flop can be constructed by cross-coupling of which logic gates? 1 point

- ( ) XOR or XNOR gates
- (●) NOR or NAND gates
- ( ) AND or NOR gates
- ( ) AND or OR gates

Clear selection

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29 A full adder circuit is given with three inputs x, y and z. You have to design a full subtractor using this full adder circuits with x denoting minuend, y denoting subtrahend and z is the previous borrow. It can be done by: 1 point

- ( ) None of the above
- (●) Complementing the input x to the circuit of carry out of the full adder
- ( ) Complementing the input y to the circuit of carry out of the full adder
- ( ) Complementing the input z to the circuit of carry out of the full adder

Clear selection

30 Which of the following input transition is valid for inputs X1X2X3 of a fundamental mode circuit? 1 point

- (●) 010 -> 110
- ( ) 011 -> 100
- ( ) 000 -> 011
- ( ) 100 -> 010

Clear selection

When overflow occurs in a 20-bit ripple counter, how many transient states does it transition through? 1 point

- ( ) 2^19
- ( ) 20