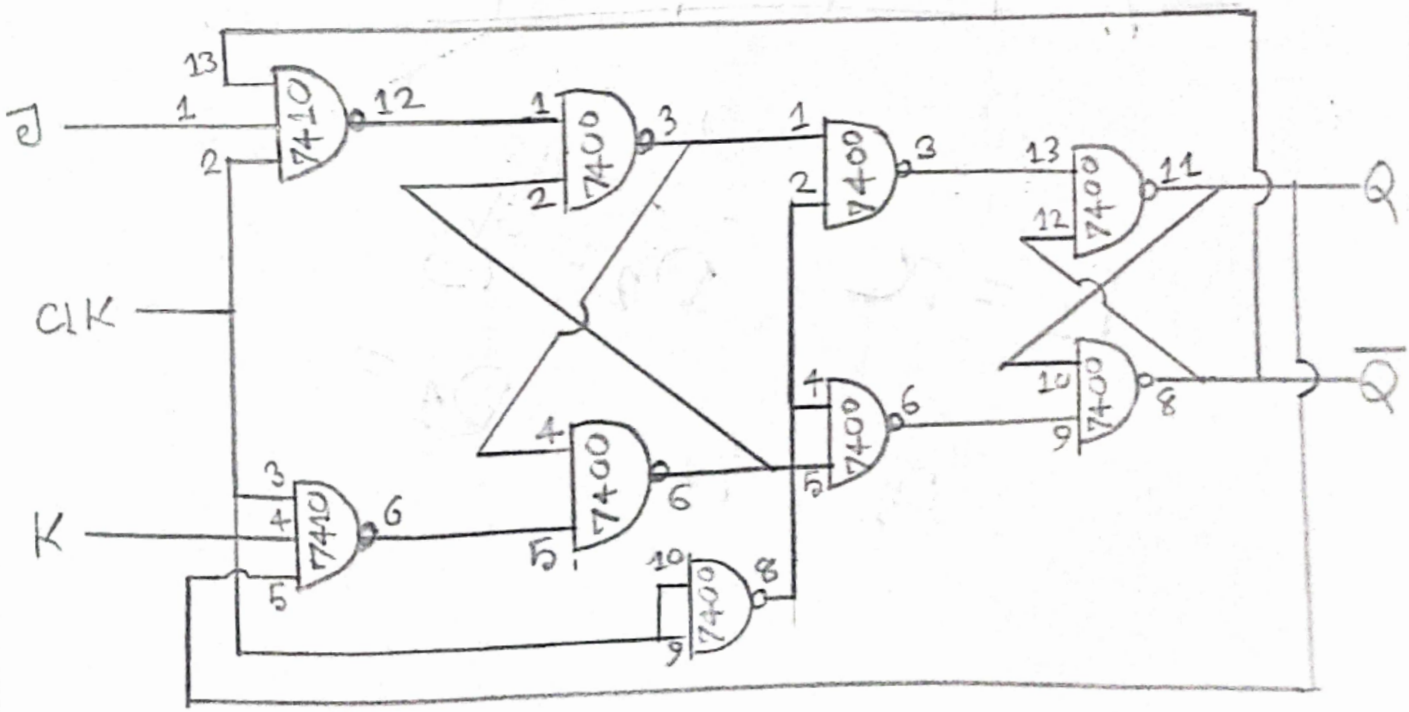
Problem-1:

Design and implement a master-slave JK flip-flop using only nand gates.

Excitation Table:

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Circuit Diagram:



Problem 2:

Design and implement a 4-bit universal shift register.

Clr	CLK	S_1	S_0	A_3	A_2	A_1	A_0	Mode
1	x	x	x	0	0	0	0	Async Reset
0	x	0	0	Q_3	Q_2	Q_1	Q_0	Hold
0	1	0	1	I_R	Q_3	Q_2	Q_1	Shift Right
0	1	1	0	Q_2	Q_1	Q_0	I_L	Shift Left
0	1	1	1	I_3	I_2	I_1	I_0	Parallel load

Circuit Diagram: