3-bit Binary to Gray Converter

Group Number:- 26

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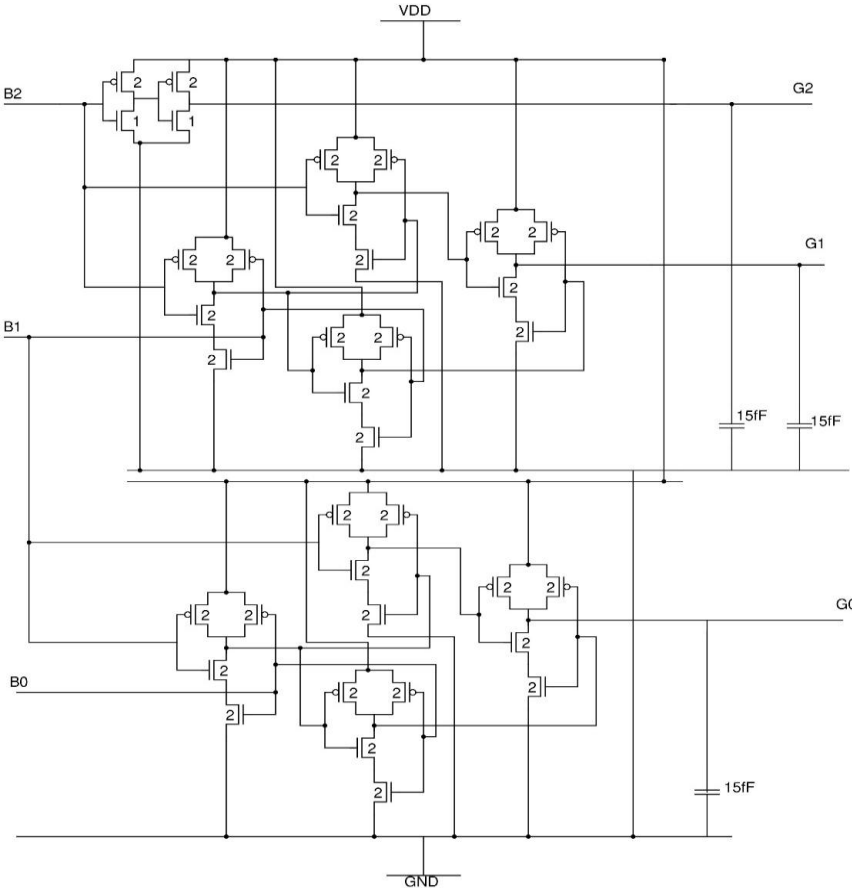Abhinav Chaudhary

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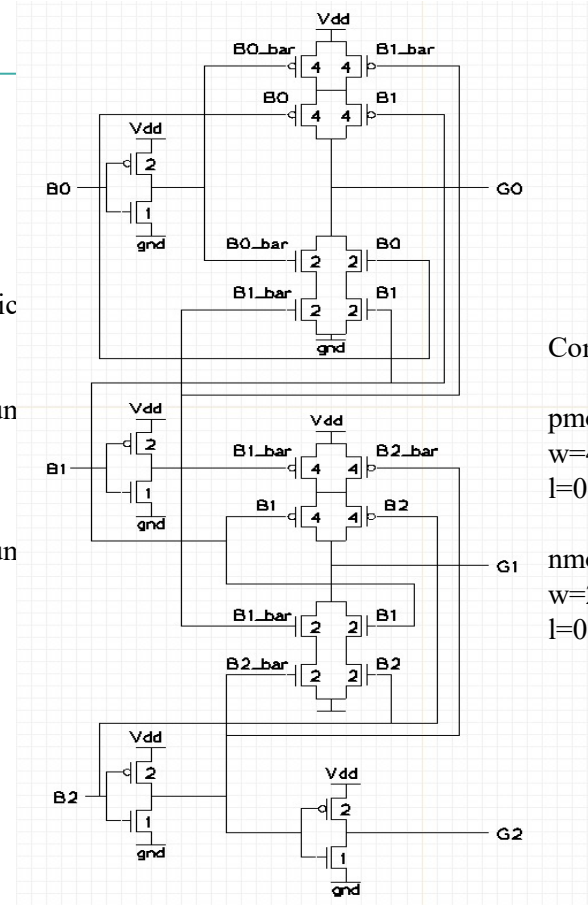INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY **DELHI**

Schematic + Sizing

Non Complex logic

pmos:
w=2*0.135=0.27um
l=0.6um

nmos:
w=2*0.135=0.27um
l=0.6um

Complex logic
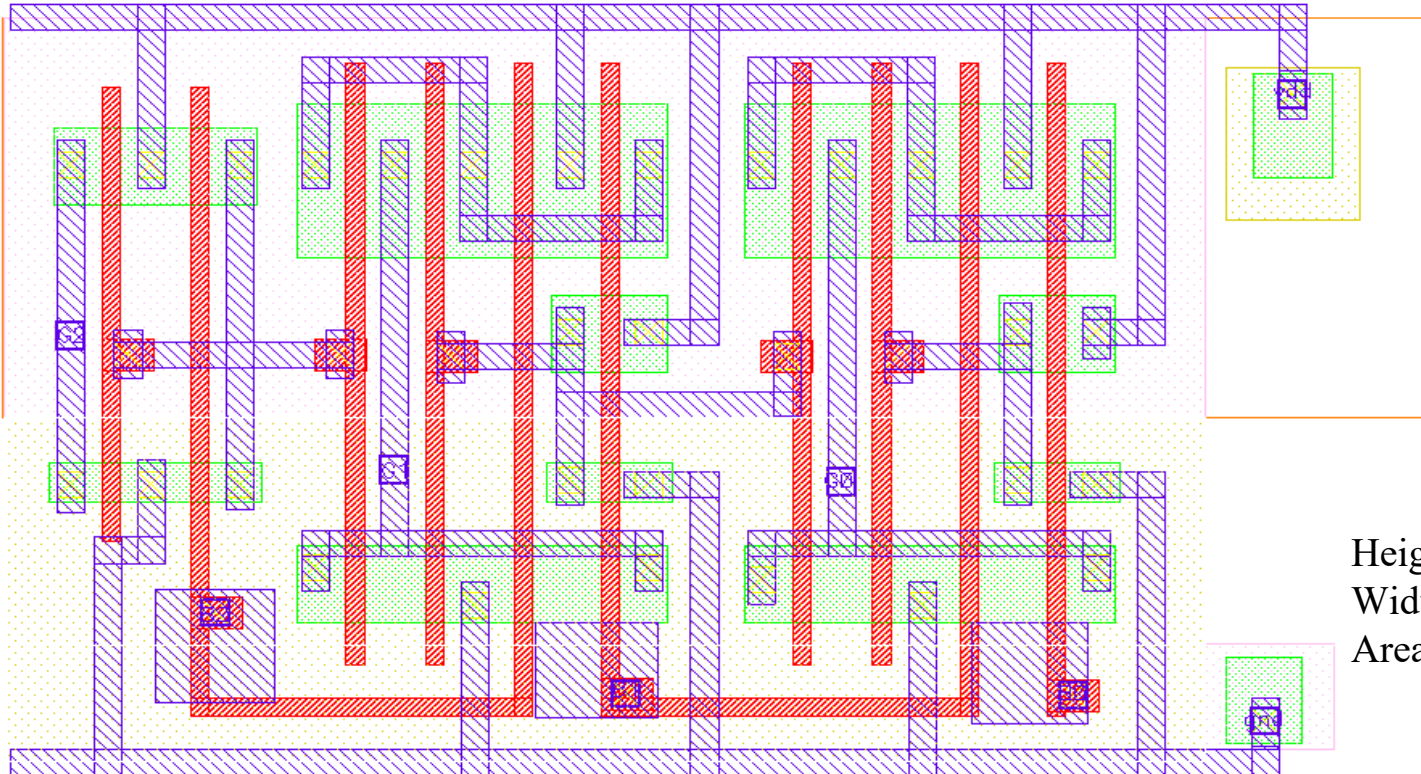
pmos:
w=4*0.135= 0.54um
l=0.6um
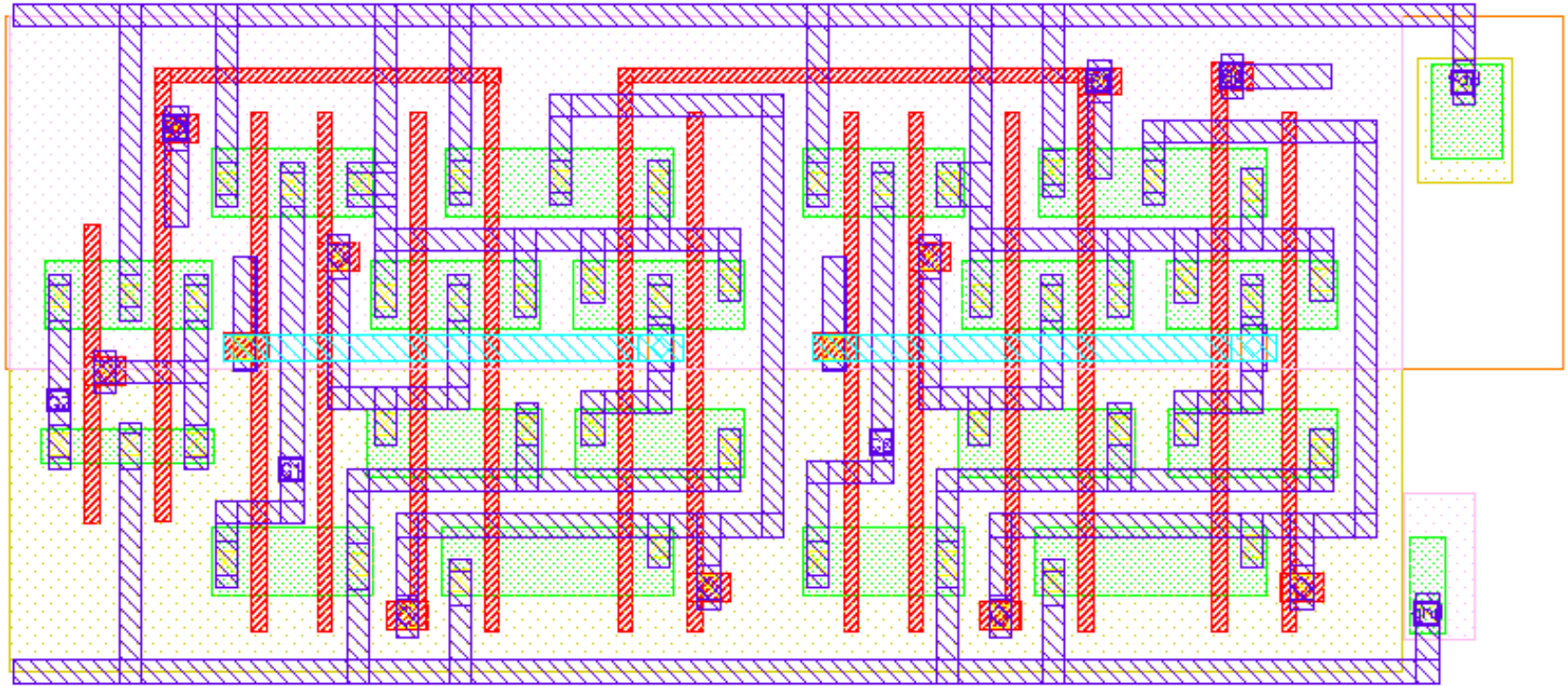
nmos:
w=2*0.135=0.27um
l=0.6um

Complex Layout

Height : 13 Tracks
Width : 19 Tracks
Area : 9.88 um^2

Non Complex Layout

Height : 13 Tracks
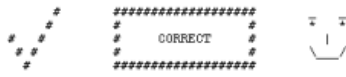Width : 28 Tracks
Area : 14.7 um^2

DRC & LVS

Left window (Calibre - RVE):

Show Unresolved ⊞ b2gC, 0 Results (in 0 of 1583 Checks)

Check / Cell / Results

Cell b2gC Summary (Clean)

```
                CELL COMPARISON RESULTS ( TOP LEVEL )

              #      ####################
          #   #      #                  #
            #   #    #      CORRECT      #
          # #   #    #                  #
            # #      #                  #
              #      ####################
```

```
LAYOUT CELL NAME:       b2gC
SOURCE CELL NAME:       bin2gray
------------------------------------------------------------
NUMBERS OF OBJECTS
------------------

                Layout    Source    Component Type
                ------    ------    --------------
Ports:            8         8
Nets:            17        17
Instances:       12        12       MN (4 pins)
                 12        12       MP (4 pins)
                ------    ------
Total Inst:      24        24
```

```
*********************************************************************
              INFORMATION AND WARNINGS
```

Right window (Calibre - RVE v2):

Applications Places System

Show Unresolved ⊞ B2G_PB, 0 Results (in 0 of 1583 Checks)
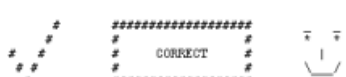
Check / Cell / Results

Rules
- Rules File

View
- Info
- Finder
- Schematics

Setup
- Options

Cell B2G_PB Summary (Clean)

```
                CELL COMPARISON RESULTS ( TOP LEVEL )

              #      ####################
          #   #      #                  #
            #   #    #      CORRECT      #
          # #   #    #                  #
            # #      #                  #
              #      ####################
```

```
LAYOUT CELL NAME:       B2G_PB
SOURCE CELL NAME:       B2G
------------------------------------------------------------
NUMBERS OF OBJECTS
------------------

                Layout    Source    Component Type
                ------    ------    --------------
Ports:            8         8
Nets:            23        23
Instances:       18        18       MN (4 pins)
                 18        18       MP (4 pins)
                ------    ------
Total Inst:      36        36
```

Delays and Power

Tpd (SS, 1.08V, 125C)						
	Pre - Layout (ps)			Post Layout (ps)		
Output bits	G2	G1	G0	G2	G1	G0
Complex	213	246	240	216	252	247
Non - Complex	196.8	254	254.3	198.4	258	258.9
Tcd (FF, 1.32V, -40C)						
	Pre - Layout (ps)			Post - Layout (ps)		
Output bits	G2	G1	G0	G2	G1	G0
Complex	97.9	93.3	91.03	98.9	95.7	93.5
Non - Complex	91	101	102	91.6	103	104

Power (SS, 1.08V, 125C)				
	Pre - Layout		Post Layout	
	Dynamic Power(uW)	Leakage Power(nW)	Dynamic Power(uW)	Leakage Power(nW)
Complex	87.4	55.7	87.5	63.7
Non - Complex	87.2	30.36	88	28.82
Power (FF, 1.32V, -40C)				
	Pre - Layout		Post - Layout	
	Dynamic Power(uW)	Leakage Power(nW)	Dynamic Power(uW)	Leakage Power(nW)
Complex	130.1	77.13	130.17	74.44
Non - Complex	130.6	37.5	132	39.9

Delay Calculation

B2

B1

B0

G2

G1

G0

```
.measure tran tplh_G0
+ TRIG v(B0) VAL='SUPPLY/2' FALL=1
+ TARG v(G0) VAL='SUPPLY/2' RISE=1

.measure tran tphl_G0
+ TRIG v(B0) VAL='SUPPLY/2' FALL=2
+ TARG v(G0) VAL='SUPPLY/2' FALL=1

.measure tran tplh_G1
+ TRIG v(B1) VAL='SUPPLY/2' FALL=1
+ TARG v(G1) VAL='SUPPLY/2' RISE=1

.measure tran tphl_G1
+ TRIG v(B1) VAL='SUPPLY/2' FALL=2
+ TARG v(G1) VAL='SUPPLY/2' FALL=1

.measure tran tplh_G2
+ TRIG v(B2) VAL='SUPPLY/2' RISE=1
+ TARG v(G2) VAL='SUPPLY/2' RISE=1

.measure tran tphl_G2
+ TRIG v(B2) VAL='SUPPLY/2' FALL=1
+ TARG v(G2) VAL='SUPPLY/2' FALL=1

.measure Tpd_G2 param = ('tplh_G2+tphl_G2'/2)
.measure Tpd_G1 param = ('tplh_G1+tphl_G1'/2)
.measure Tpd_G0 param = ('tplh_G0+tphl_G0'/2)
```
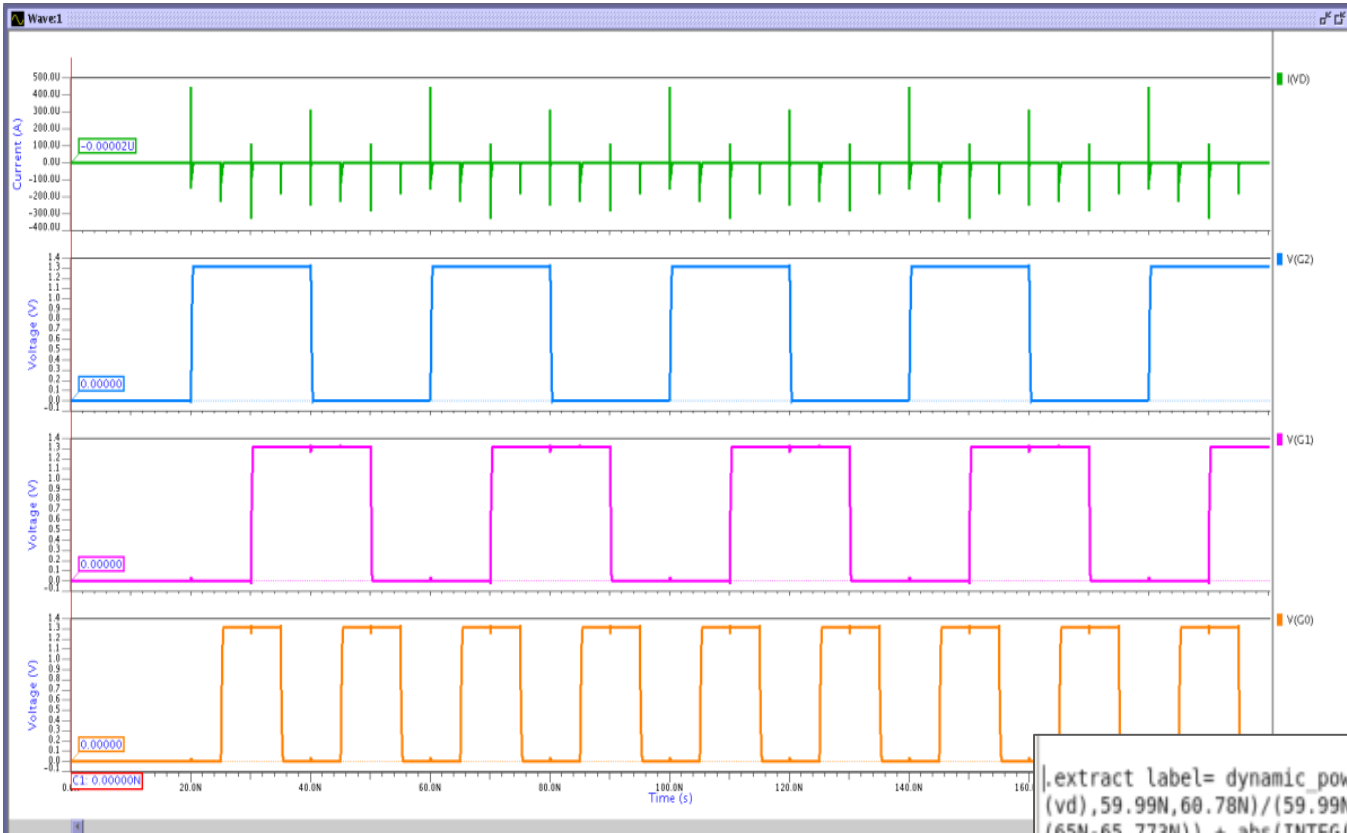
B2 pulse period = 40ns
B1 pulse period = 20ns
B0 pulse period = 10ns

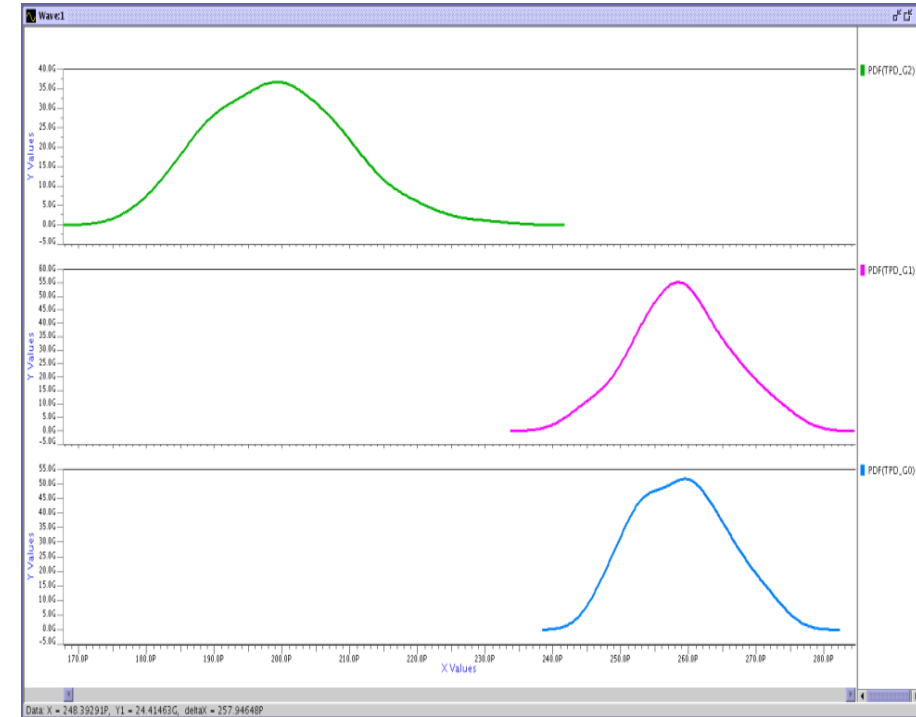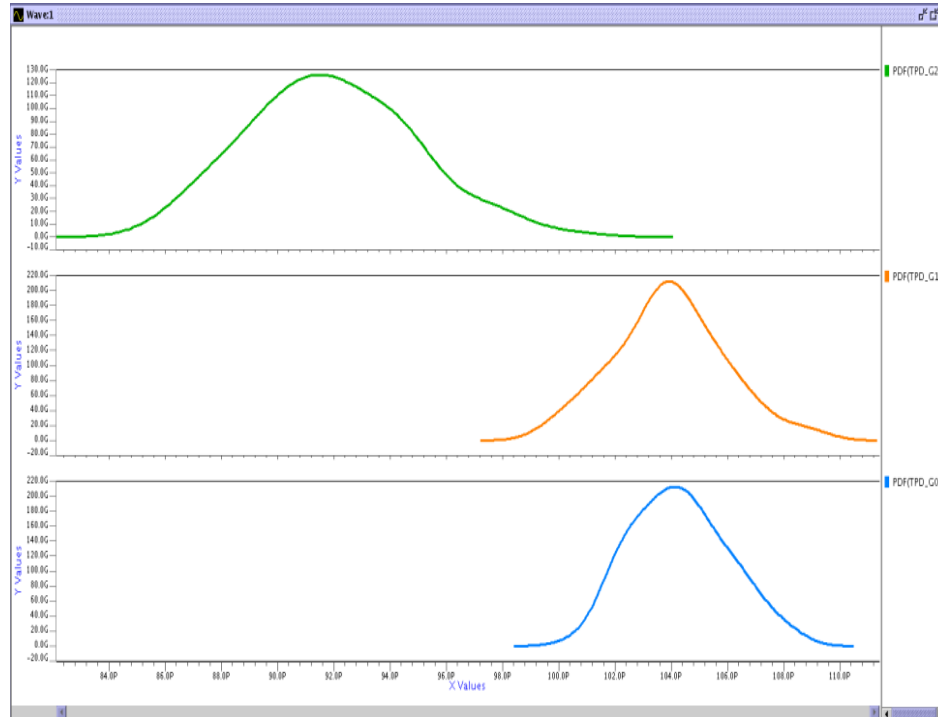# Power calculation

I(vdd)

G2

G1

G0

```
.extract label= dynamic_power ( SUPPLY * (      abs(INTEG(I
(vd),59.99N,60.78N)/(59.99N-60.78N)) + 2 * (abs(INTEG(I(vd),65N,65.773N)/
(65N-65.773N)) + abs(INTEG(I(vd),69.997N,71.27N)/(69.997N-71.27N)) + abs
(INTEG(I(vd),75.009N,75.85N)/(75.009N-75.85N))) +  abs(INTEG(I
(vd),79.99N,80.85N)/(79.99N-80.85N)) )  )
```

Monte Carlo Analysis

At FF, 1.32, -40   At SS, 1.08, 125

Work Distribution

- Complex layout and simulations done by Karan and Anany

- Non Complex layout and simulations done by Gagandeep and Saurav