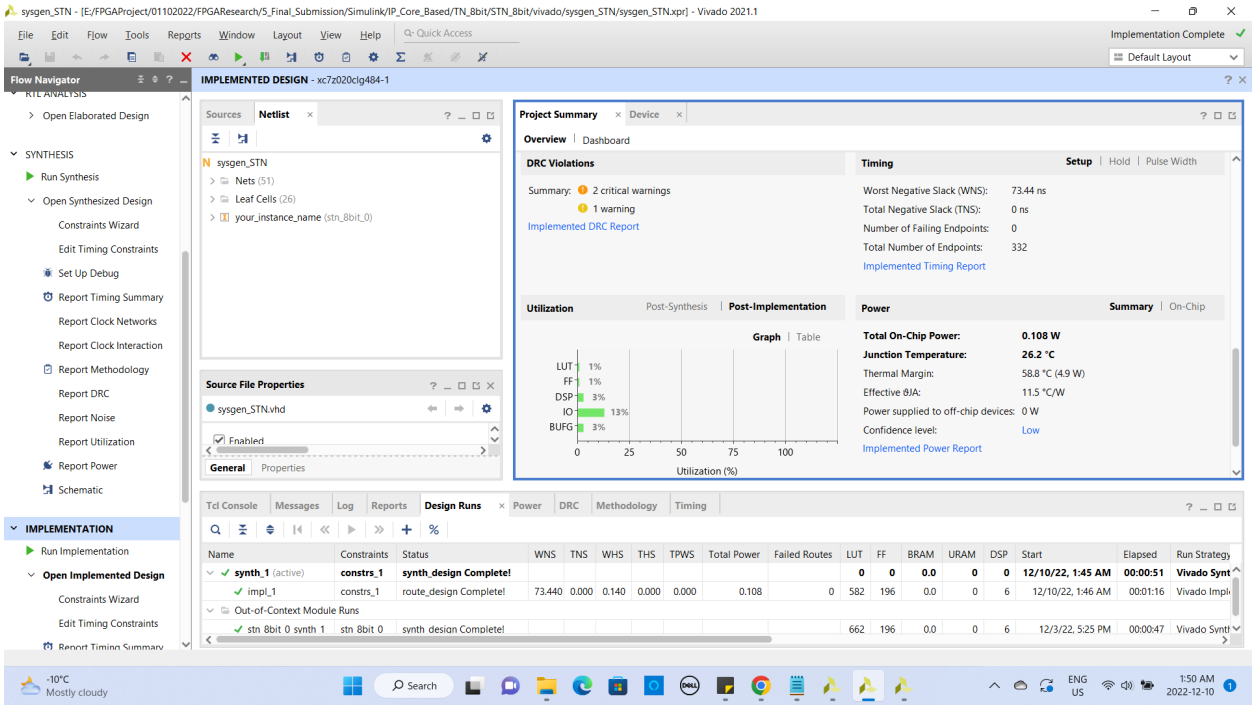
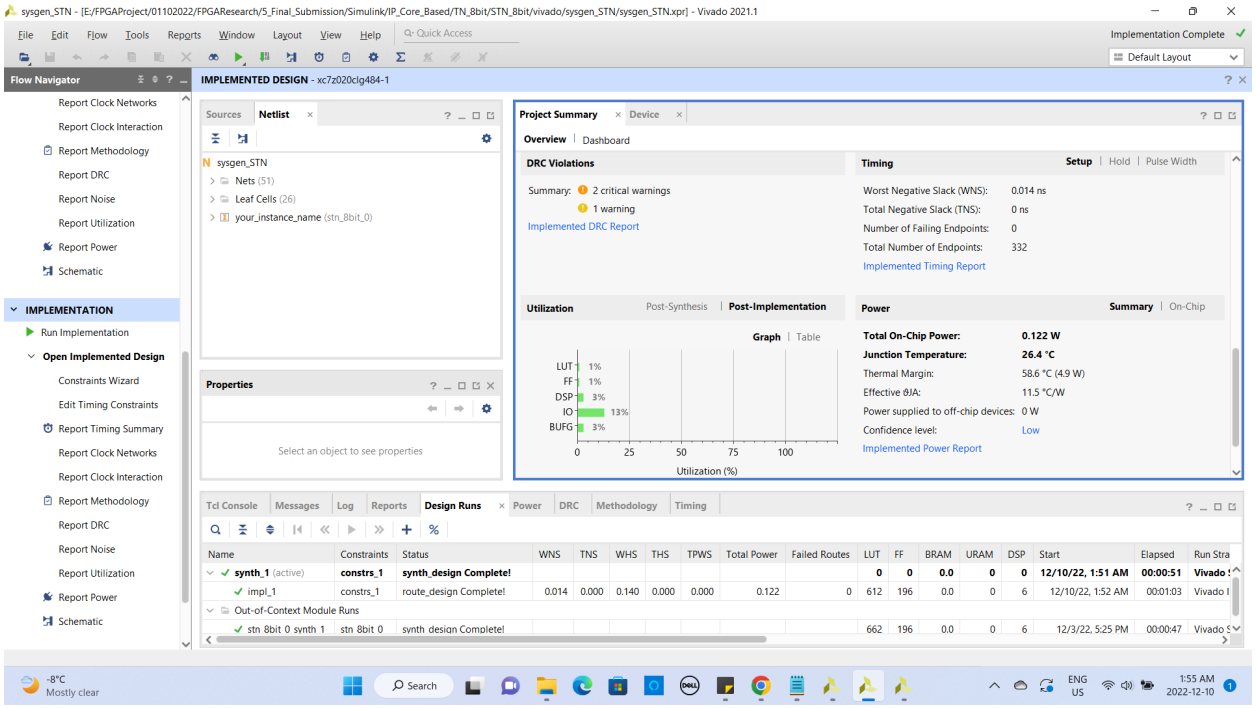
8-bit IP_Core

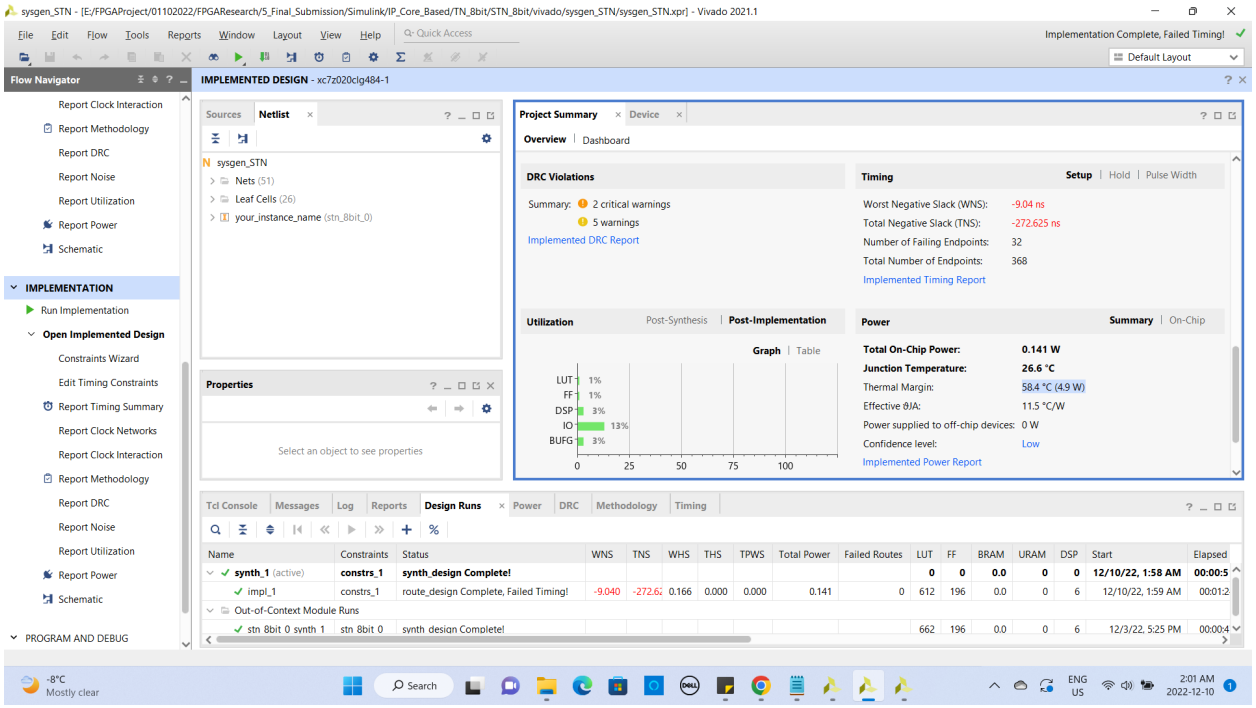
10MHz



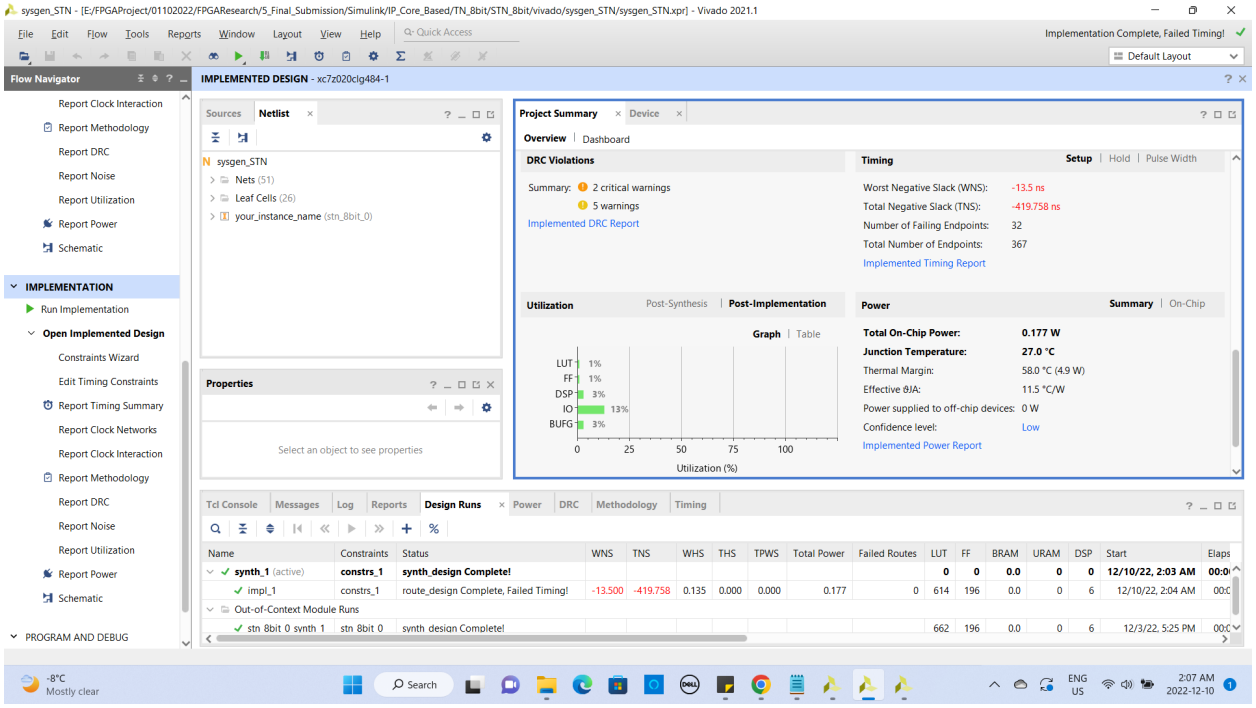
50Mhz



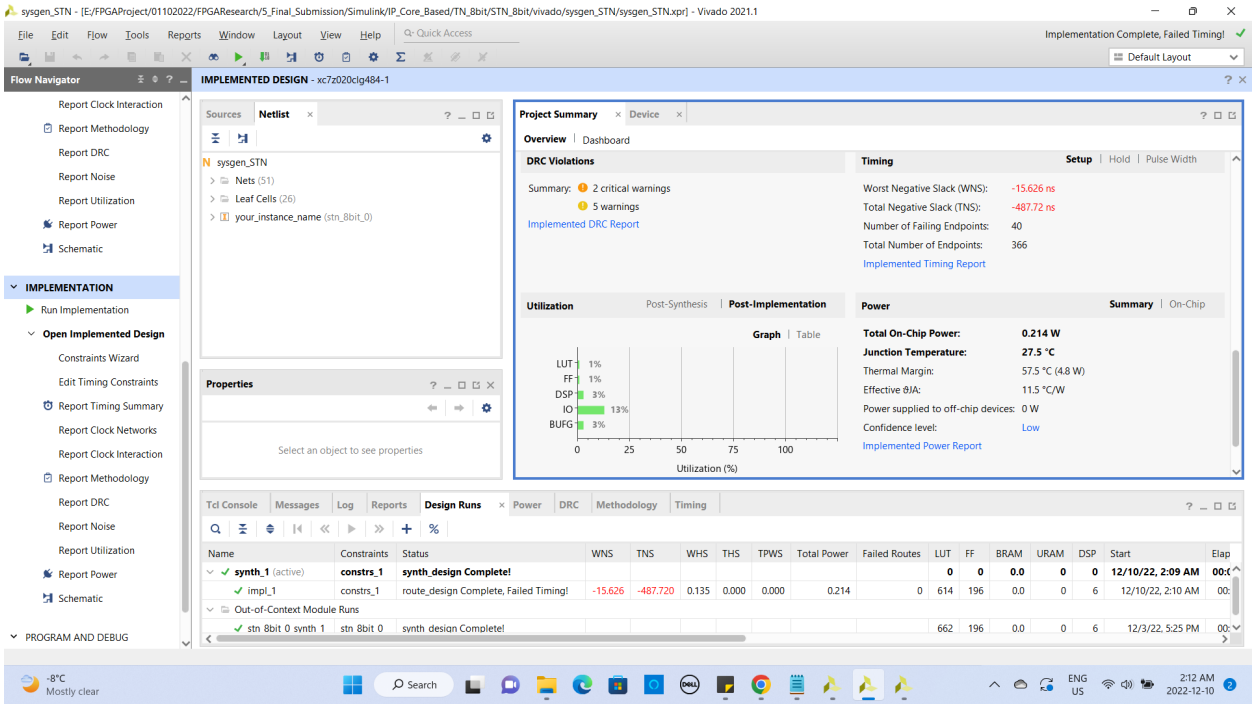
100MHz



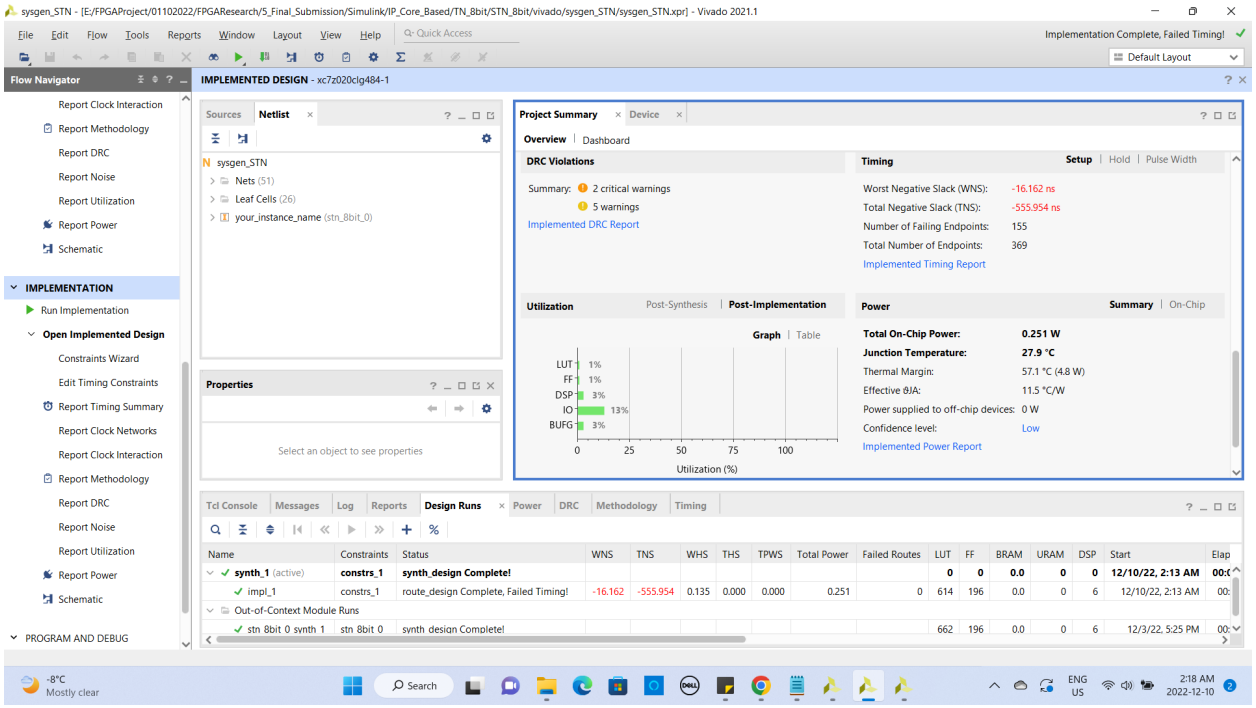
200Mhz



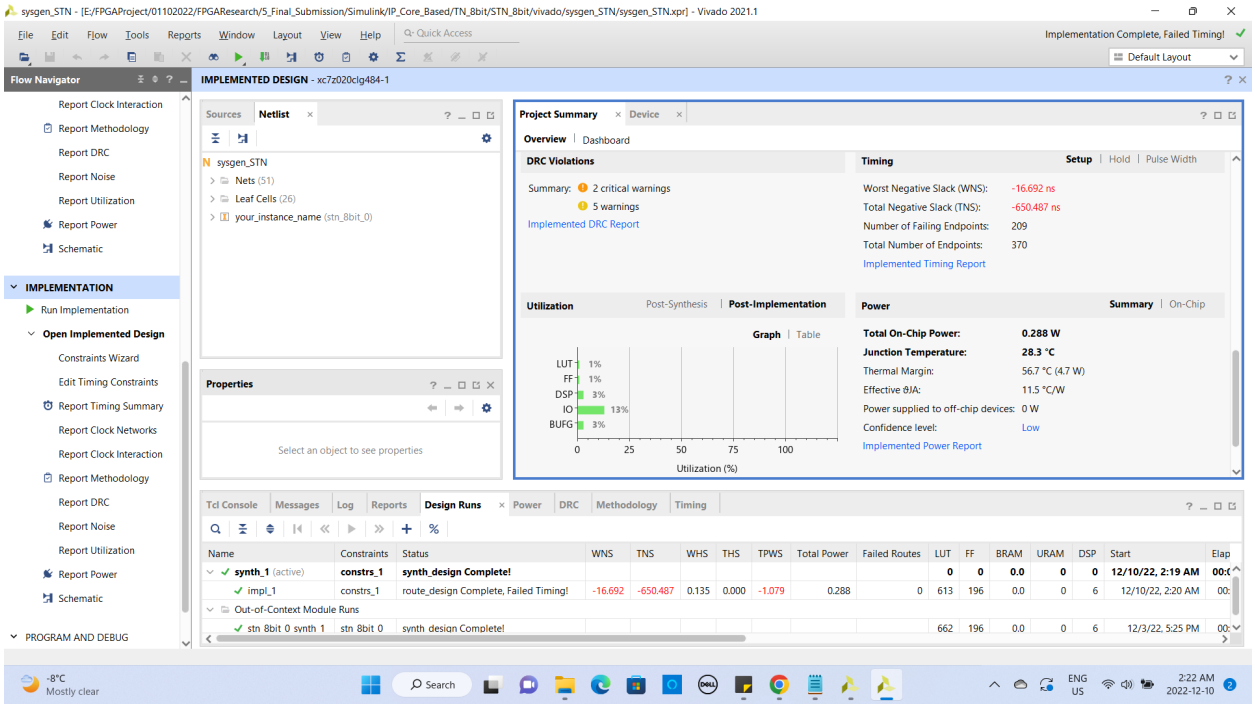
300Mhz



400Mhz

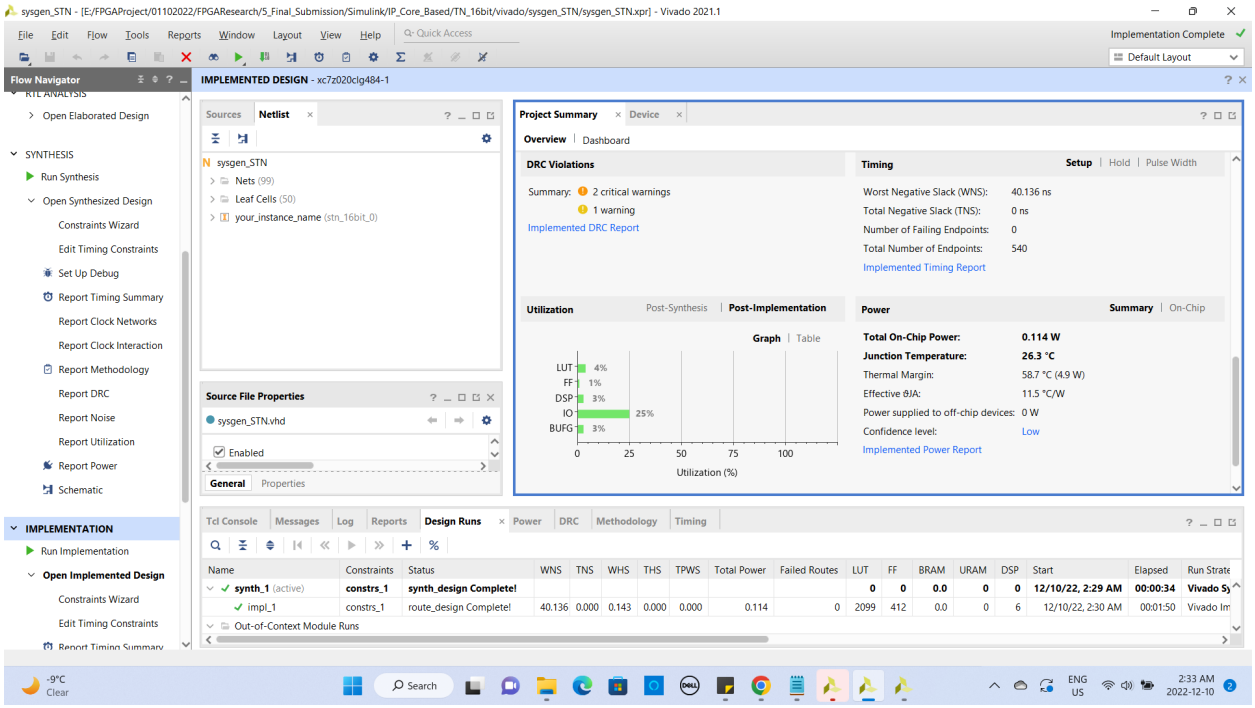


500MHz

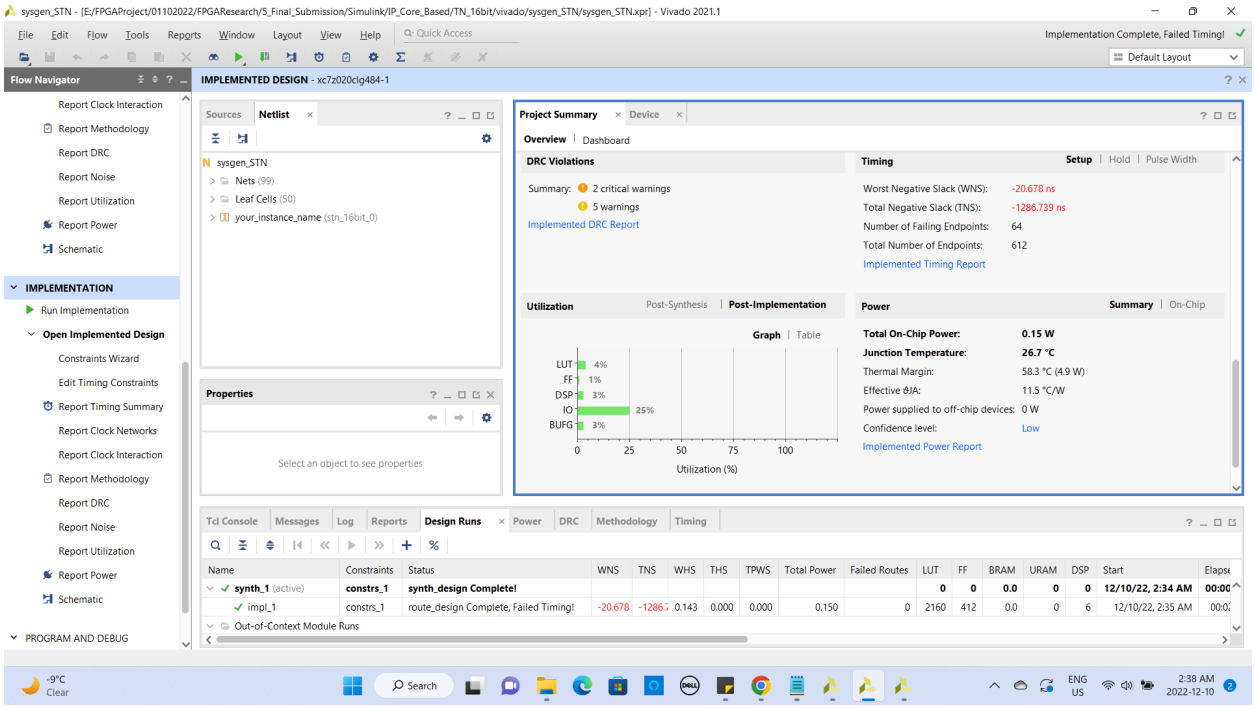


16-bit IP_Core

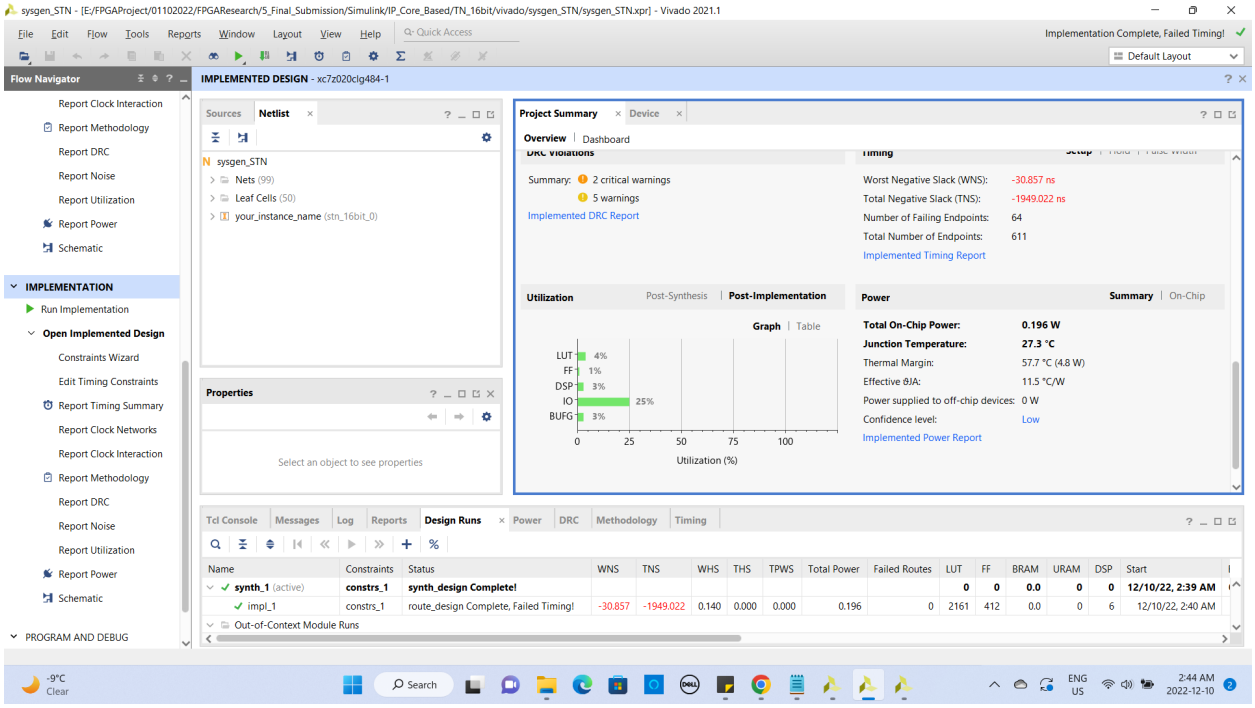
10MHz



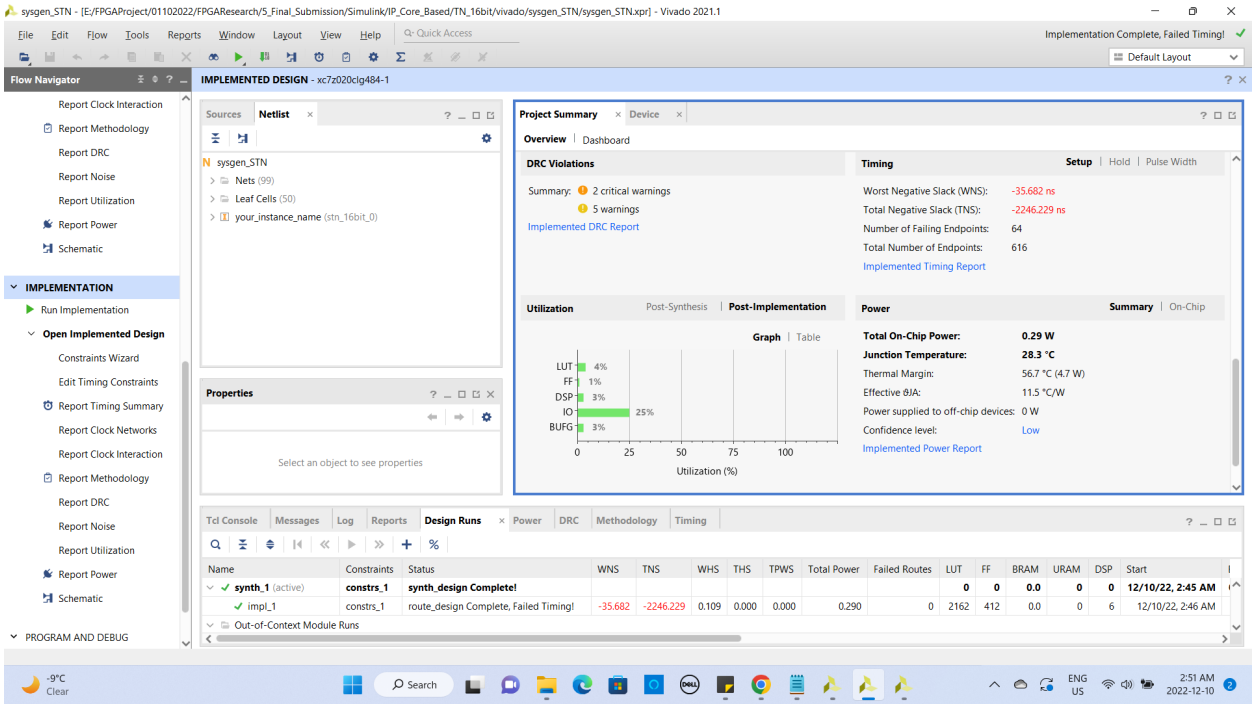
50MHz



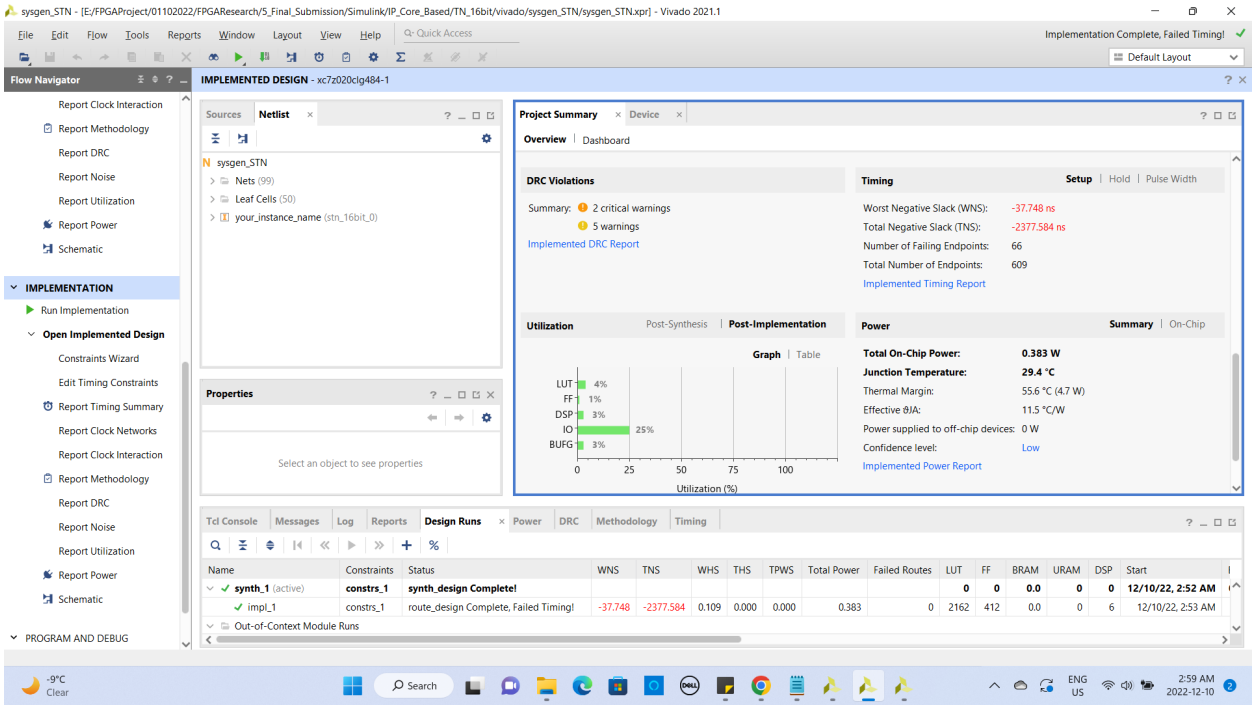
100MHz



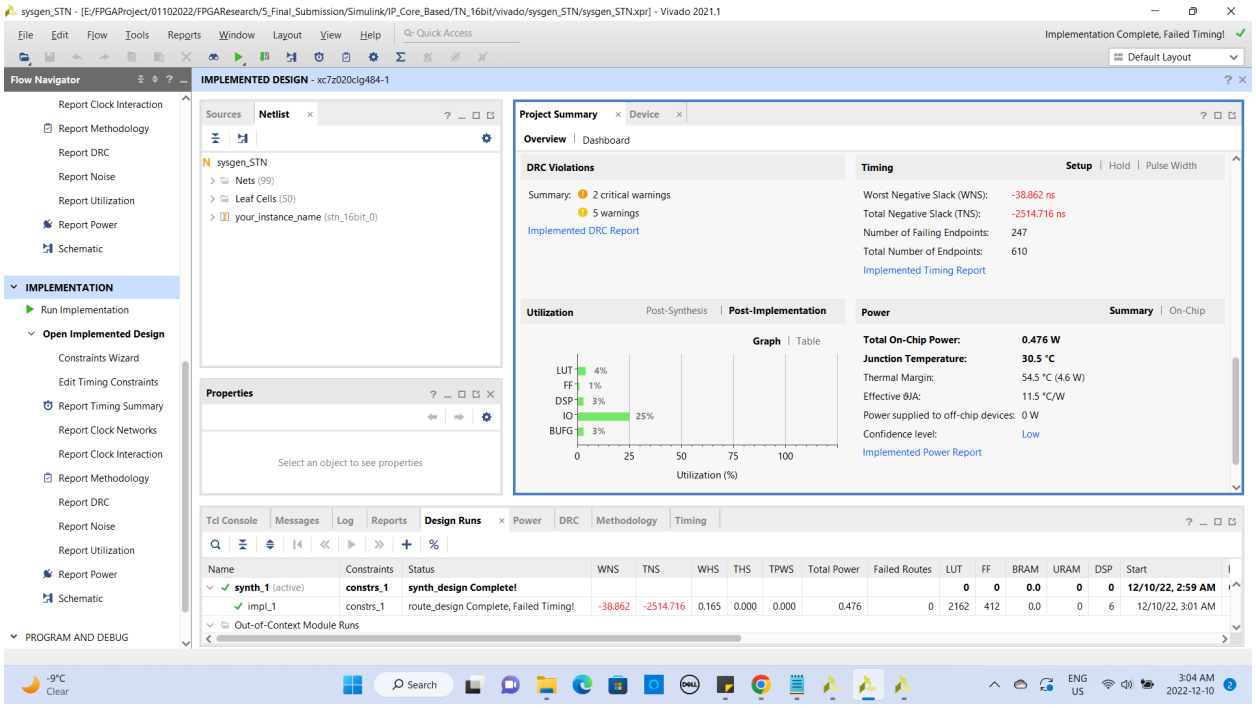
200MHz



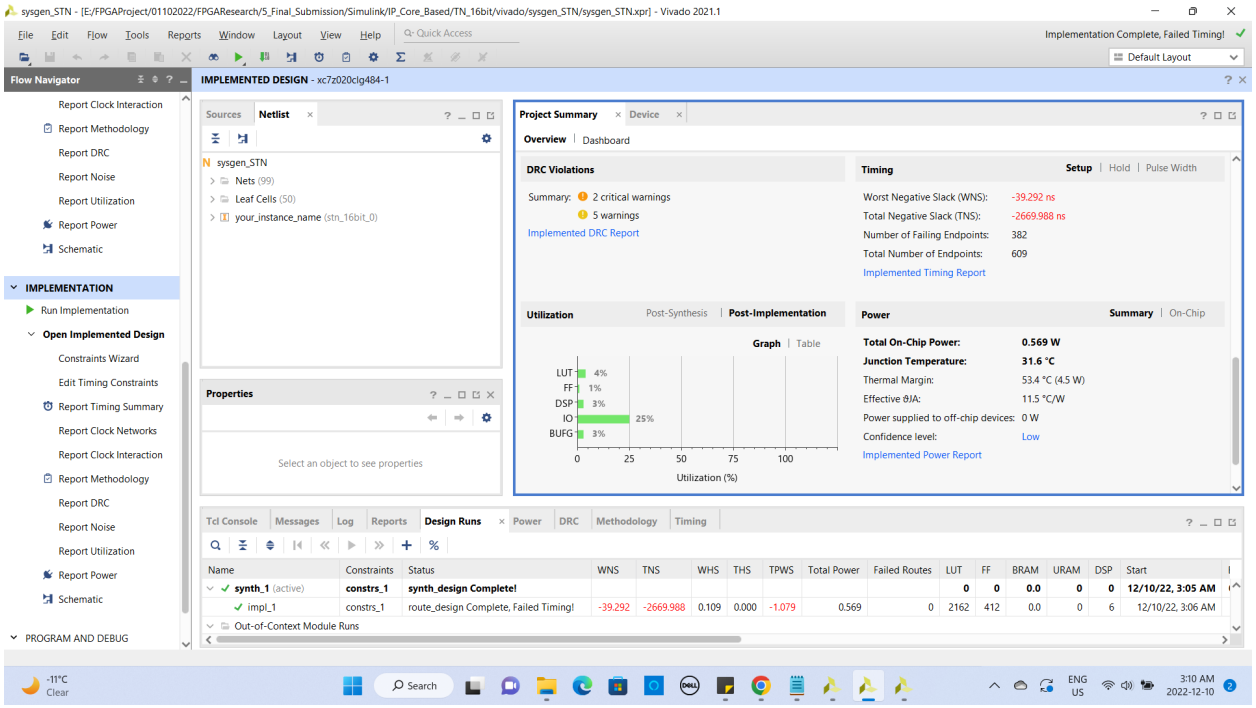
300MHz



400MHz

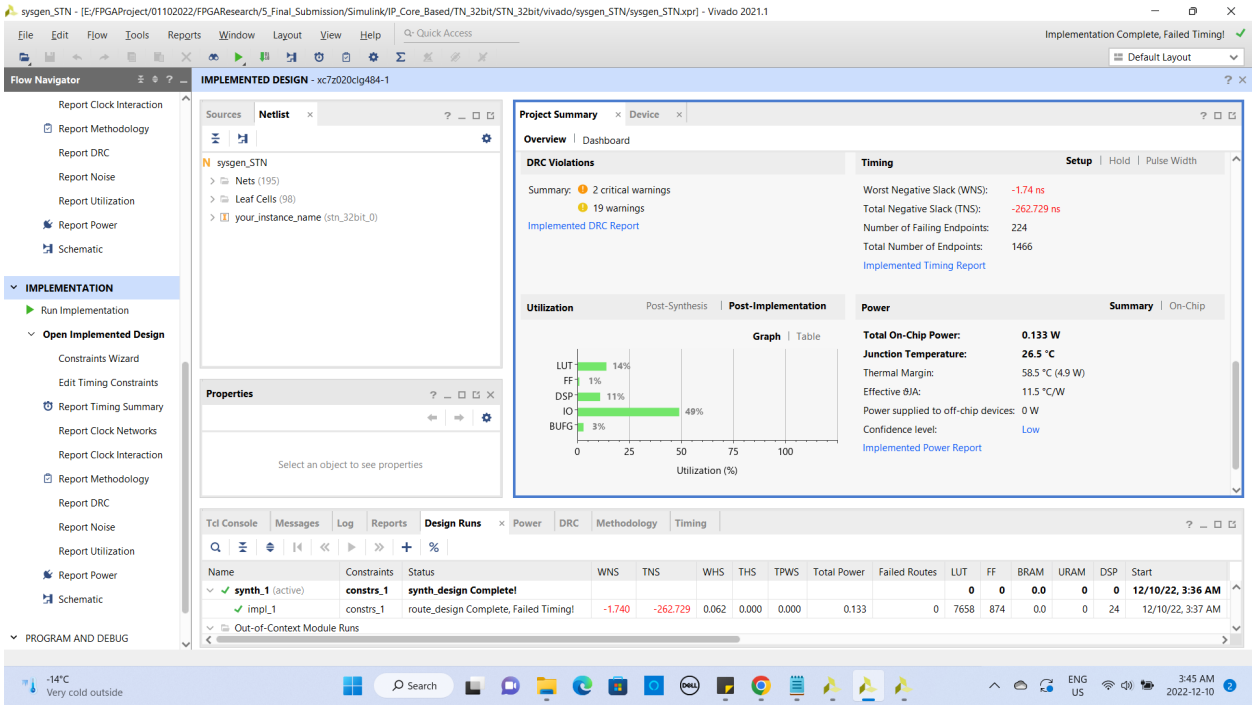


500MHz

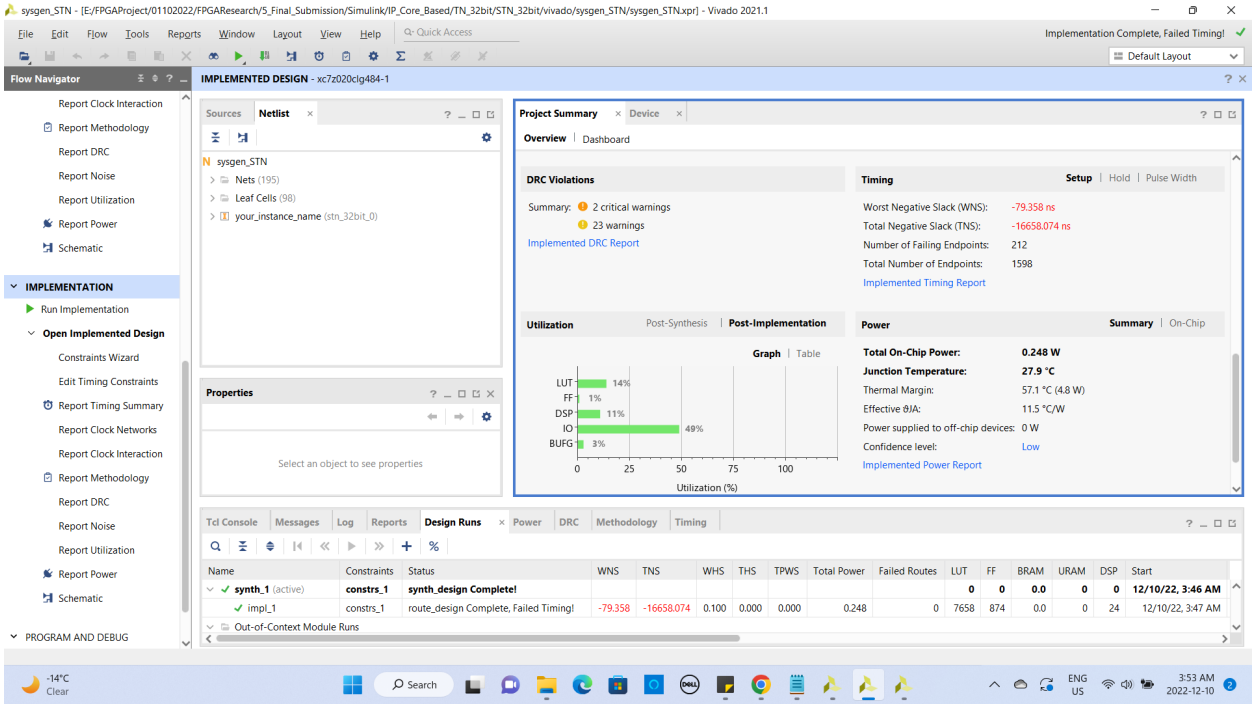


32-bit IP_Core

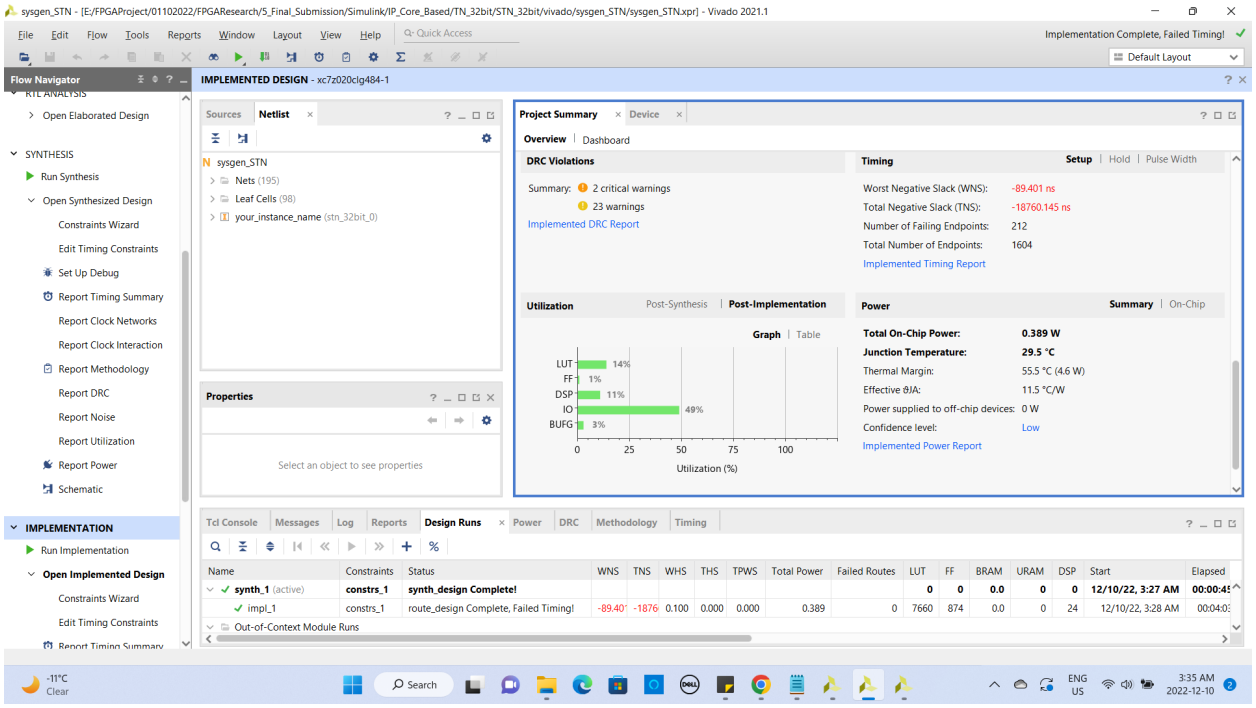
10MHz



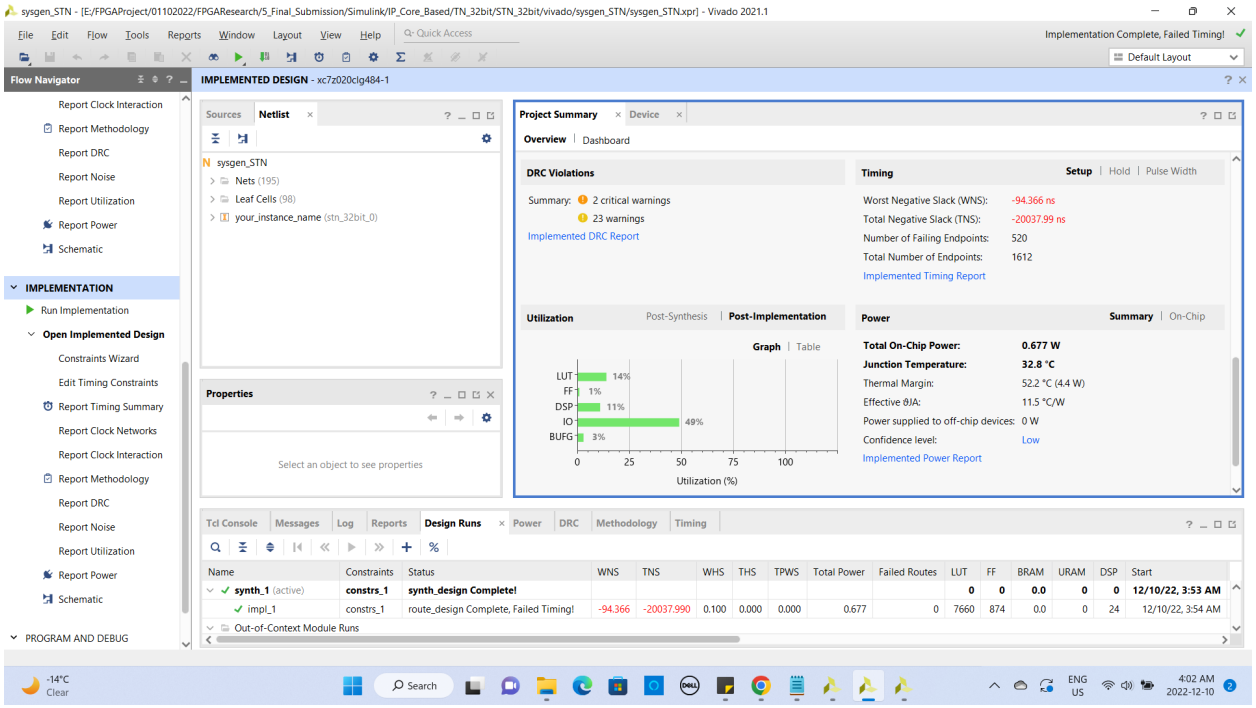
50MHz



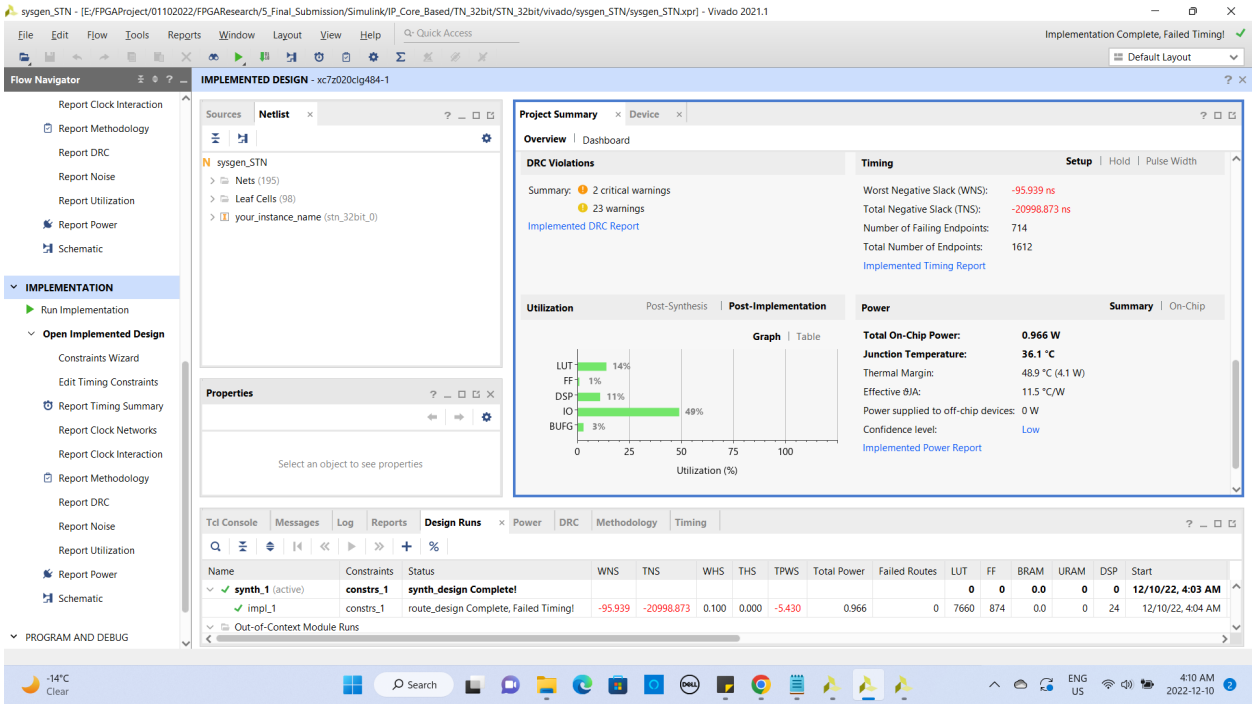
100MHz



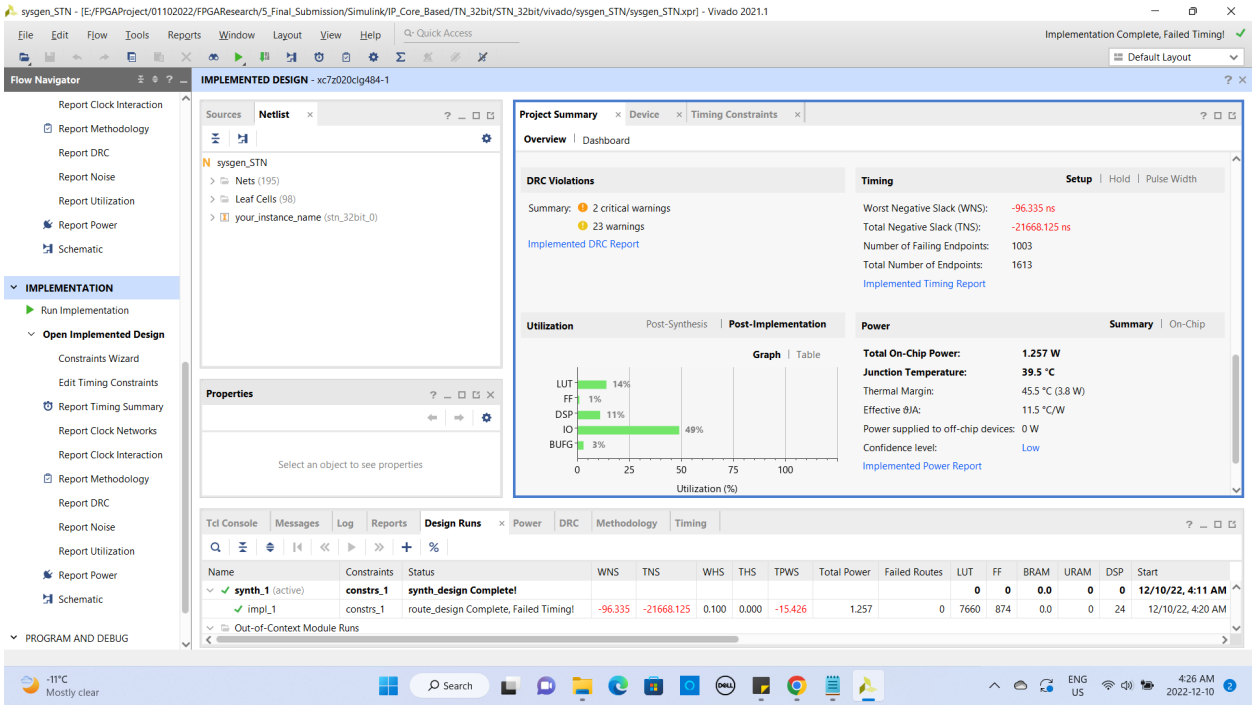
200Mhz



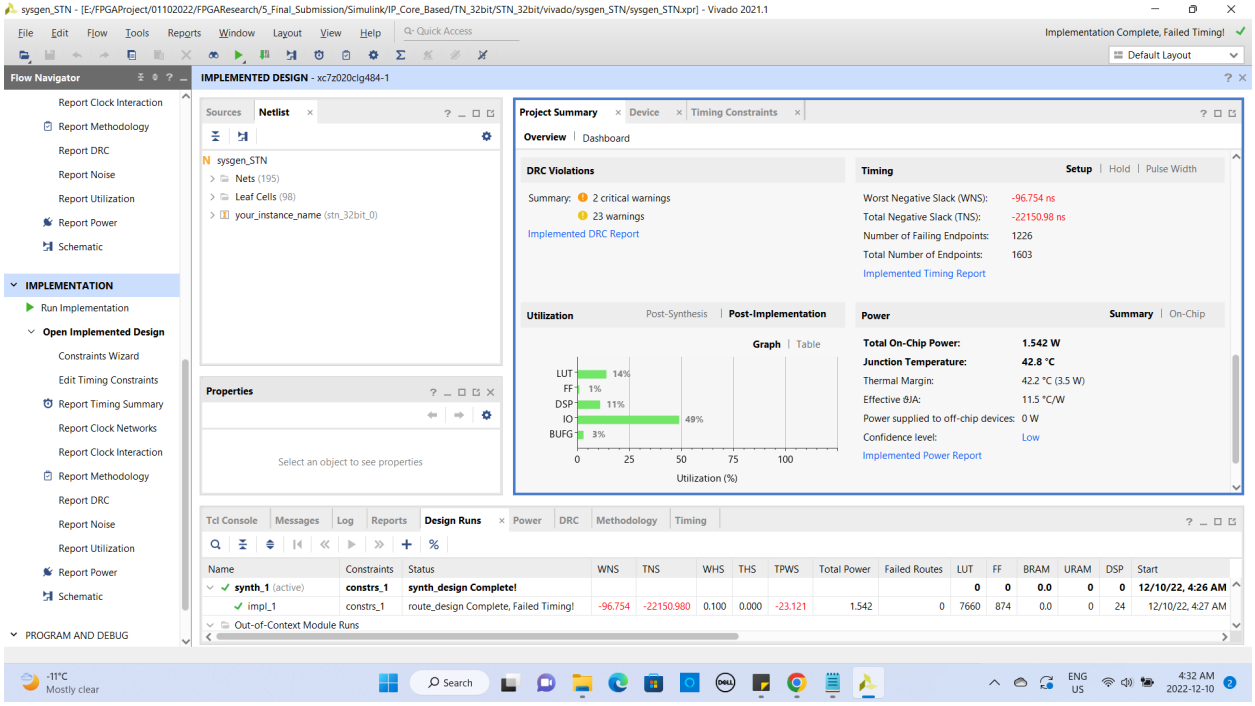
300MHz



400Mhz



500Mhz


sysgen_STN - [E:/FPGAProject/01102022/FPGAResearch/5_Final_Submission/Simulink/IP_Core_Based/TN_32bit/STN_32bit/vivado/sysgen_STN/sysgen_STN.xpr] - Vivado 2021.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete, Failed Timing!
Default Layout
Flow Navigator
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
IMPLEMENTED DESIGN - xc7z020clg484-1
Sources
Netlist
sysgen_STN
Nets (195)
Leaf Cells (98)
your_instance_name (stn_32bit_0)
Properties
Select an object to see properties
Project Summary
Device
Timing Constraints
Overview
Dashboard
DRC Violations
Summary: 2 critical warnings
23 warnings
Implemented DRC Report
Timing
Setup
Hold
Pulse Width
Worst Negative Slack (WNS): -96.754 ns
Total Negative Slack (TNS): -22150.98 ns
Number of Failing Endpoints: 1226
Total Number of Endpoints: 1603
Implemented Timing Report
Utilization
Post-Synthesis
Post-Implementation
Graph
Table
LUT 14%
FF 1%
DSP 11%
IO 49%
BUFG 3%
0 25 50 75 100
Utilization (%)
Power
Summary
On-Chip
Total On-Chip Power: 1.542 W
Junction Temperature: 42.8 °C
Thermal Margin: 42.2 °C (3.5 W)
Effective θJA: 11.5 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Implemented Power Report
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start
synth_1 (active) constrs_1 synth_design Complete! 0 0 0.0 0 0 12/10/22, 4:26 AM
impl_1 constrs_1 route_design Complete, Failed Timing! -96.754 -22150.980 0.100 0.000 -23.121 1.542 0 7660 874 0.0 0 24 12/10/22, 4:27 AM
Out-of-Context Module Runs
-11°C
Mostly clear
Search
ENG
US
4:32 AM
2022-12-10