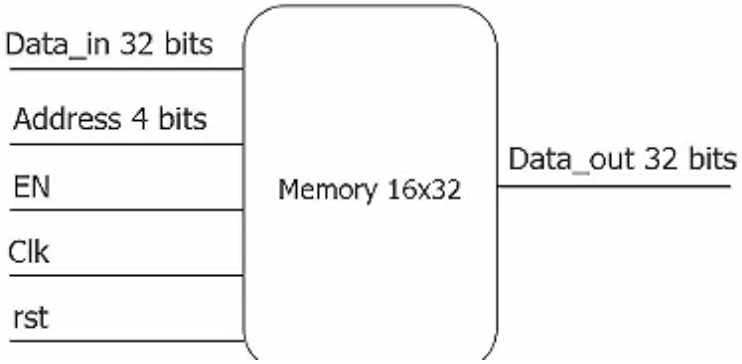
ercise

Create testplan for the memory shown below



Block Info

This design works when positive edge comes:
1) the enable is High, the memory in writing scenario
So it takes the input data and put them in memory[address] and then the output is the data located in memory[address] and also
2) If the enable is LOW the memory in reading scenario
then the output is the data located in memory[address]
3) for reset signal is high the output is zeroes cause all the locations returned to zeroes
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Testing Items

Enable → 0 memory in reading scenario
1 memory in writing scenario

Reset → 0 memory registers has the same old values
1 memory registers returned to zeroes

Address → address 0000 is reading and writing
address 1111 is reading and writing
from address 4 to address 6 reading and writing

Data_in → Data Valid (normal data) {0,(2^32)-1 , {500 : 1000} }
Data in Valid like (32'bx or 32'bz)
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Test Cases

Case	Enable	Address	Data in
Test01	enabled	Address 0000	Data Valid
Test02	Disable	Address 1111	Dara In valid
Test 03	Enable	Normal Address	Data Valid
Test04	Disable	Normal Address	Data Valid
Test05	Disable	Normal Address	Data Valid
Test Reset	enabled	Normal Address	Data Valid
Test Reset	Disable	Normal Address	Dara In valid