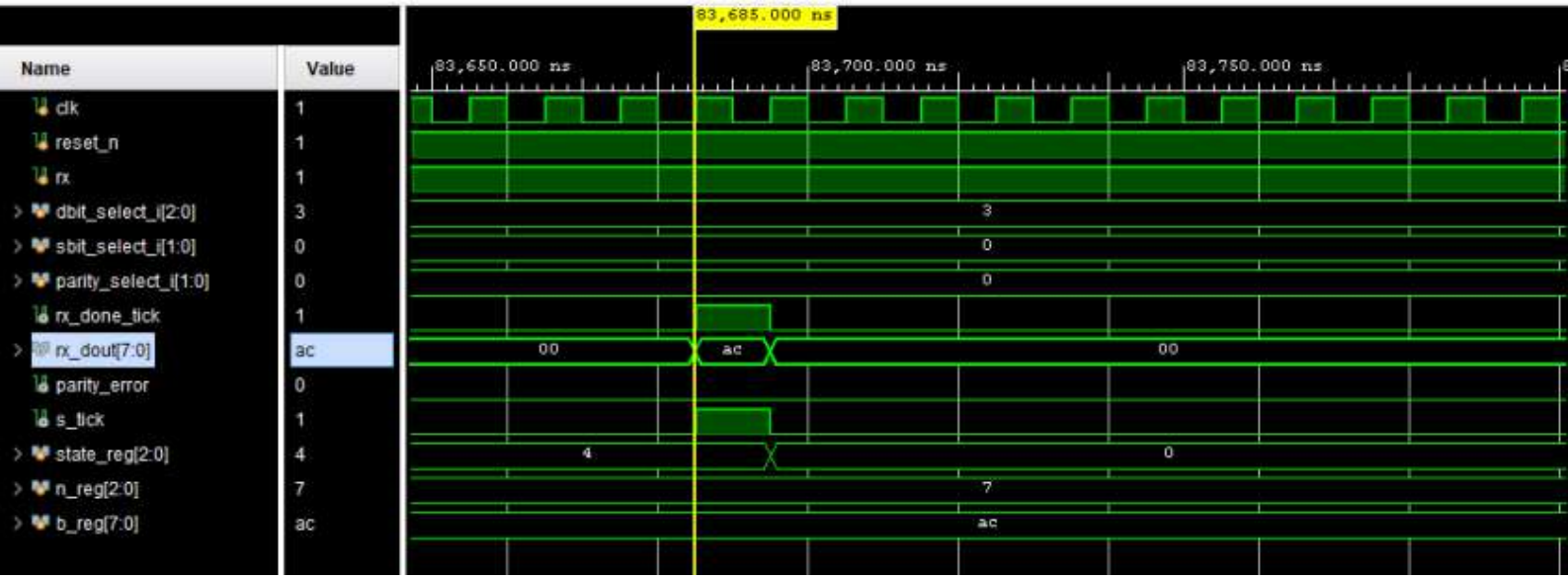
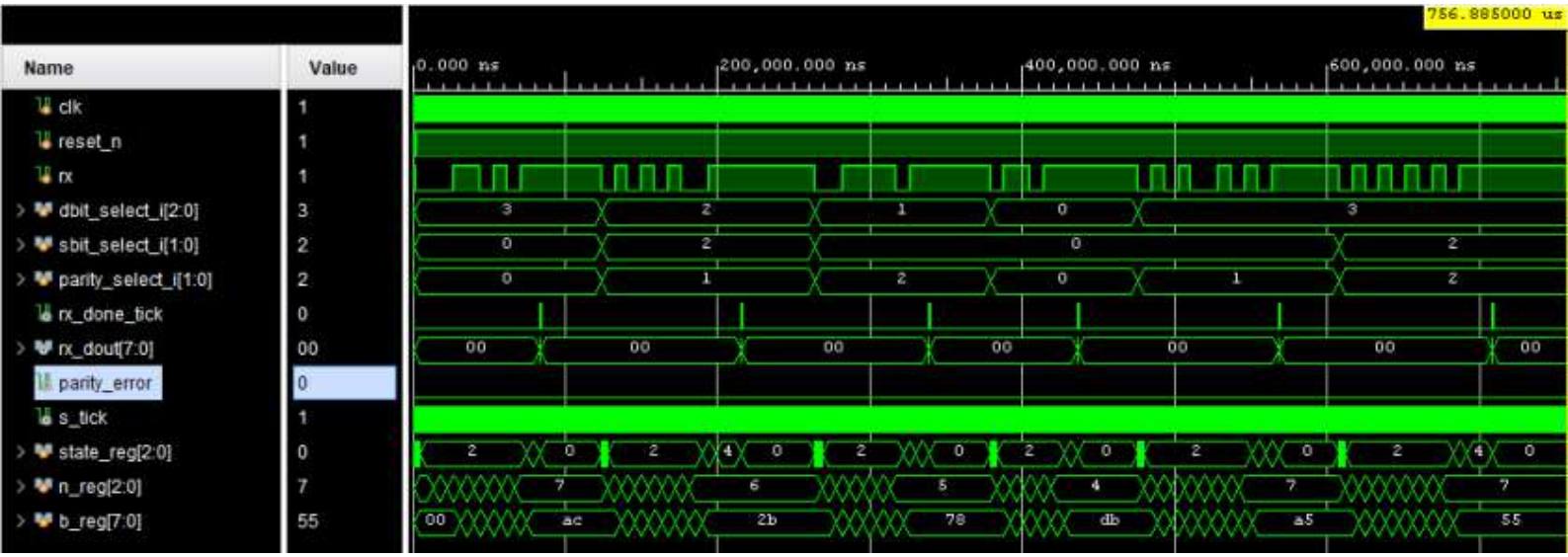
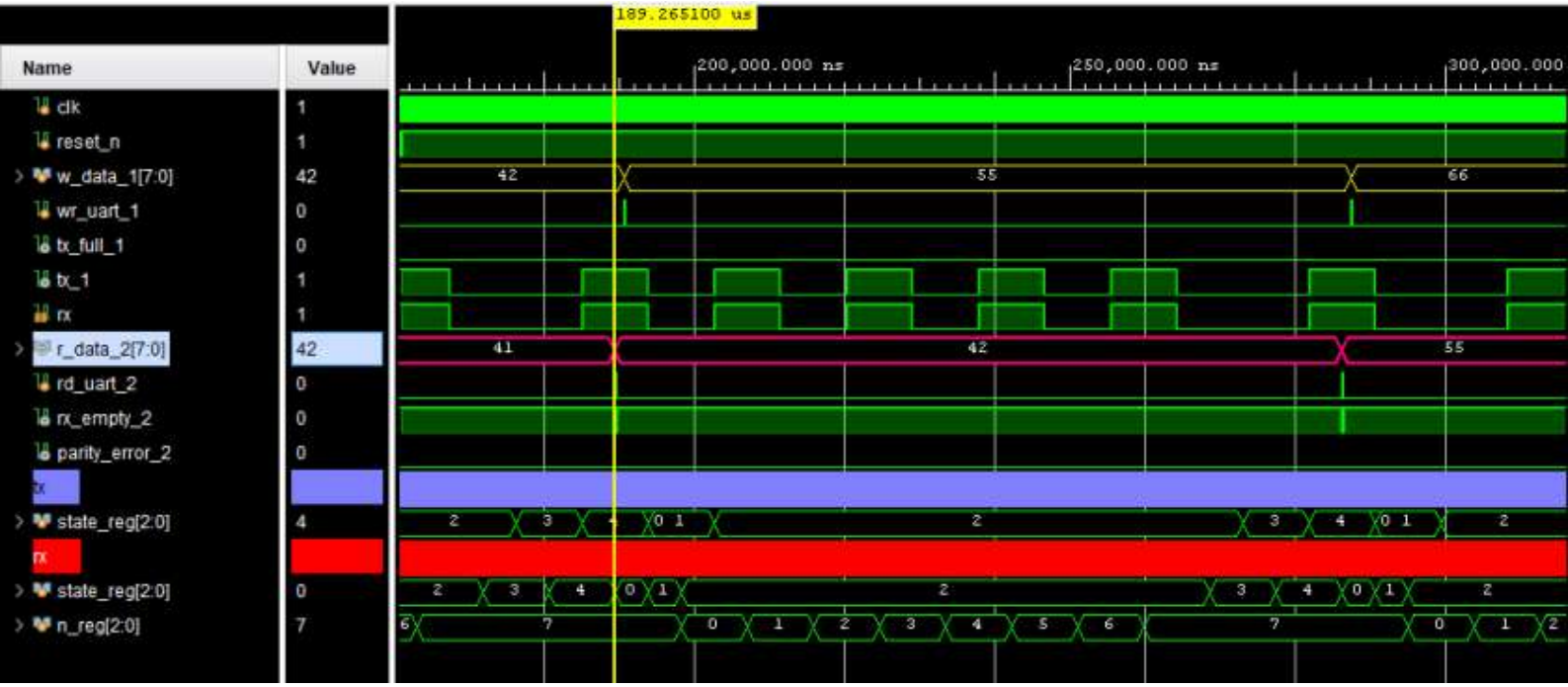

90.000000 us
0.000 ns
50,000.000 ns
100,000.000 ns
Name
Value
clk
0
reset_n
1
dbit_select_i[2:0]
2
sbit_select_i[1:0]
2
parity_select_i[1:0]
1
data_bits_to_tx[2:0]
6
stop_ticks[4:0]
31
tx_start
0
tx_din[7:0]
01010101
tx
0
tx_done_tick
0
s_tick
0
state_reg[2:0]
1
n_reg[2:0]
7
b_reg[7:0]
85
parity_en
1
calculated_parity
0
3
2
0
2
0
1
7
6
15
31
10101100
01010101
1
2
4
1
2
0
1
2
3
4
5
6
7
0
1
2
3
4
172
86
43
21
10
5
2
1
0
85
42
21
10
5


Name
Value
clk
0
reset_n
1
dbit_select_i[2:0]
3
sbit_select_i[1:0]
0
parity_select_i[1:0]
0
data_bits_to_tx[2:0]
7
stop_ticks[4:0]
15
tx_start
0
tx_din[7:0]
01010101
tx
1
tx_done_tick
0
s_tick
0
state_reg[2:0]
0
n_reg[2:0]
7
b_reg[7:0]
0
parity_en
0
calculated_parity
1
604.045000 us
0.000 ns
100,000.000 ns
200,000.000 ns
300,000.000 ns
400,000.000 ns
500,000.000 ns
10101100
01010101
11110000
00010101
00101010
10101010
01010101


83,685.000 ns
Name
Value
83,650.000 ns
83,700.000 ns
83,750.000 ns
clk
1
reset_n
1
rx
1
dbit_select_i[2:0]
3
sbit_select_i[1:0]
0
parity_select_i[1:0]
0
rx_done_tick
1
rx_dout[7:0]
ac
parity_error
0
s_tick
1
state_reg[2:0]
4
n_reg[2:0]
7
b_reg[7:0]
ac
00
ac
00
4
0


Name
Value
clk
reset_n
rx
dbit_select_i[2:0]
sbit_select_i[1:0]
parity_select_i[1:0]
rx_done_tick
rx_dout[7:0]
parity_error
s_tick
state_reg[2:0]
n_reg[2:0]
b_reg[7:0]
1
1
1
3
2
2
0
00
0
1
0
7
55
0.000 ns
200,000.000 ns
400,000.000 ns
600,000.000 ns
756.885000 us
ac
2b
78
db
a5

Name	Slice LUTs (63400)	Slice Registers (126800)	Block RAM Tile (135)	Bonded IOB (210)	BUFGCTRL (32)
N uart_transceiver	209	176	1	36	1
> baud_gen (baud_generator)	29	14	0	0	0
receiver (uart_rx)	49	21	0	0	0
> rx_fifo (fifo_generator_0)	48	60	0.5	0	0
transmitter (uart_tx)	35	21	0	0	0
> tx_fifo (fifo_generator_0)	48	60	0.5	0	0

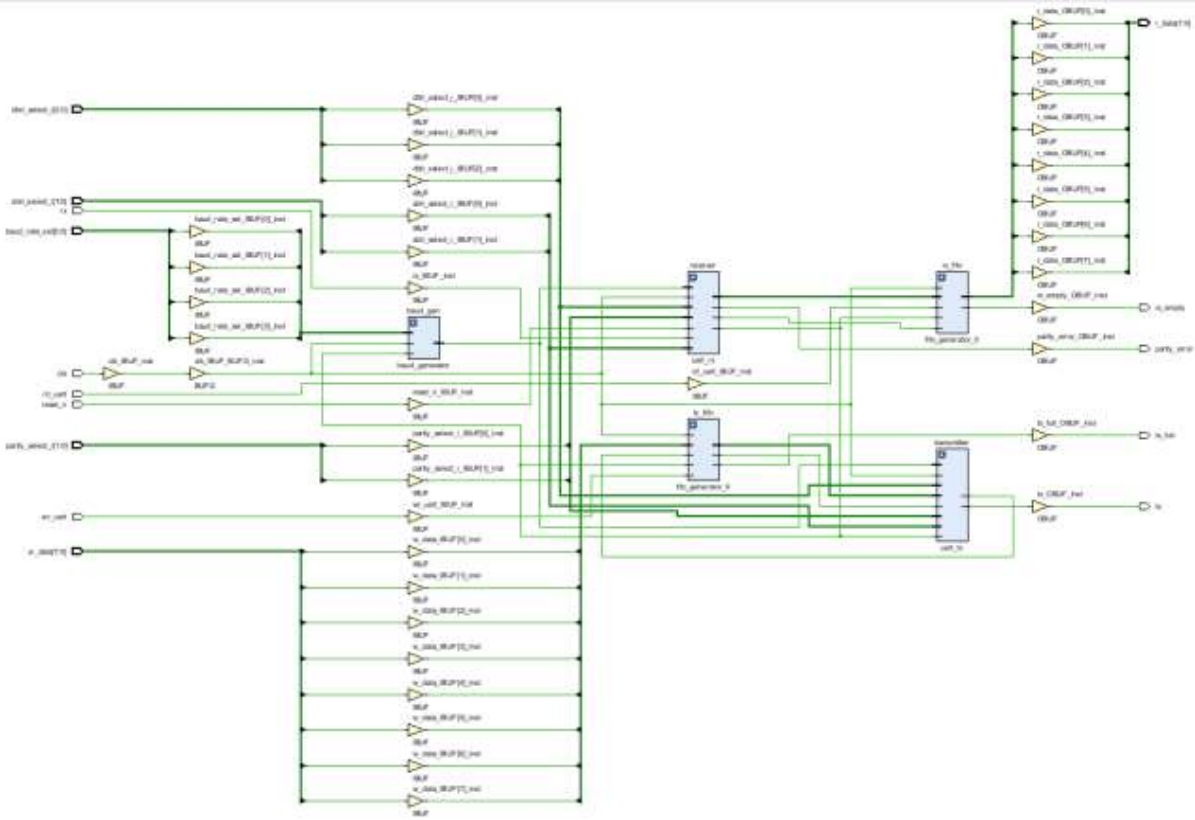

189.265100 us
200,000.000 ns
250,000.000 ns
300,000.000
Name
Value
clk
1
reset_n
1
w_data_1[7:0]
42
wr_uart_1
0
tx_full_1
0
tx_1
1
rx
1
r_data_2[7:0]
42
rd_uart_2
0
rx_empty_2
0
parity_error_2
0
tx
state_reg[2:0]
4
rx
state_reg[2:0]
0
n_reg[2:0]
7
42
55
66
41
42
55


453.285000 us
Name
Value
0.000 ns
100,000.000 ns
200,000.000 ns
300,000.000 ns
400,000.000 ns
clk
1
reset_n
1
w_data_1[7:0]
99
00
42
55
66
99
wr_uart_1
0
tx_full_1
0
tx_1
1
rx
1
r_data_2[7:0]
19
00
41
42
55
66
rd_uart_2
0
rx_empty_2
0
parity_error_2
0
tx
state_reg[2:0]
4
rx
state_reg[2:0]
0
n_reg[2:0]
6

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.782 ns	Worst Hold Slack (WHS):	0.132 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	355	Total Number of Endpoints:	355	Total Number of Endpoints:	181

All user specified timing constraints are met.

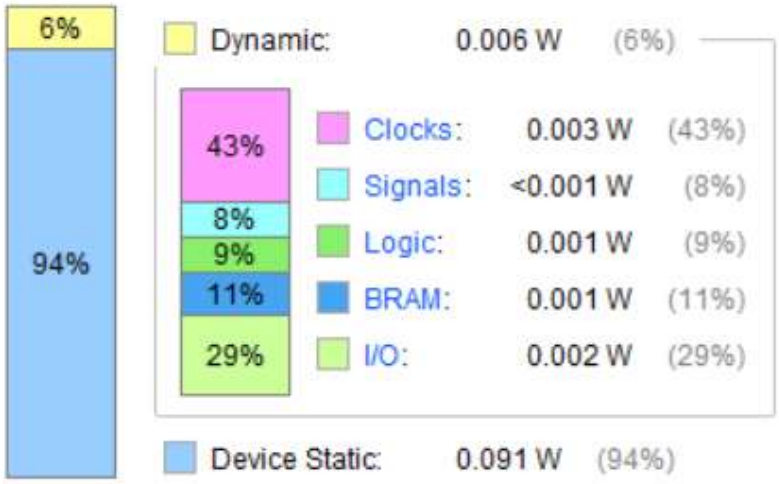


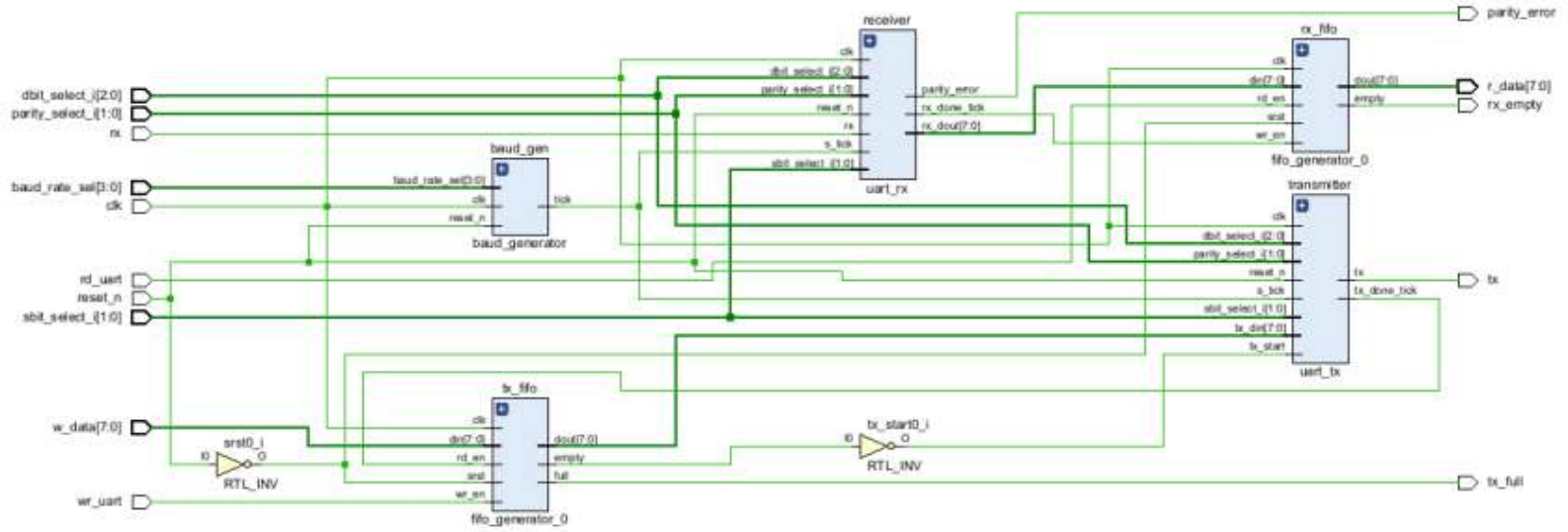
Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.097 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.4°C**
Thermal Margin:	59.6°C (12.9 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

On-Chip Power




receiver
parity_error
rx_fifo
dbit_select_i[2:0]
parity_select_i[1:0]
rx
baud_gen
baud_rate_sel[3:0]
clk
baud_generator
uart_rx
fifo_generator_0
r_data[7:0]
rx_empty
transmitter
rd_uart
reset_n
sbit_select_i[1:0]
tx
tx_done_tick
uart_tx
tx_fifo
w_data[7:0]
srst0_i
RTL_INV
tx_start0_i
RTL_INV
fifo_generator_0
tx_full
wr_uart