

The background features a series of concentric circles in a light gray color, centered on the page. On the left side, there are stylized circuit lines in a teal color, with small circles at the end of the lines, resembling a network or data flow.

# TASK 2

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# WHAT ARE COMPUTING SYSTEM COMPONENTS ?

- Processor
- Memory
- Input Output Peripherals



# WHAT ARE EMBEDDED SYSTEM CHALLENGES ?

- Real-Time Constraints
  - Power Consumption
  - Cost Constraints
  - Size
  - Performance
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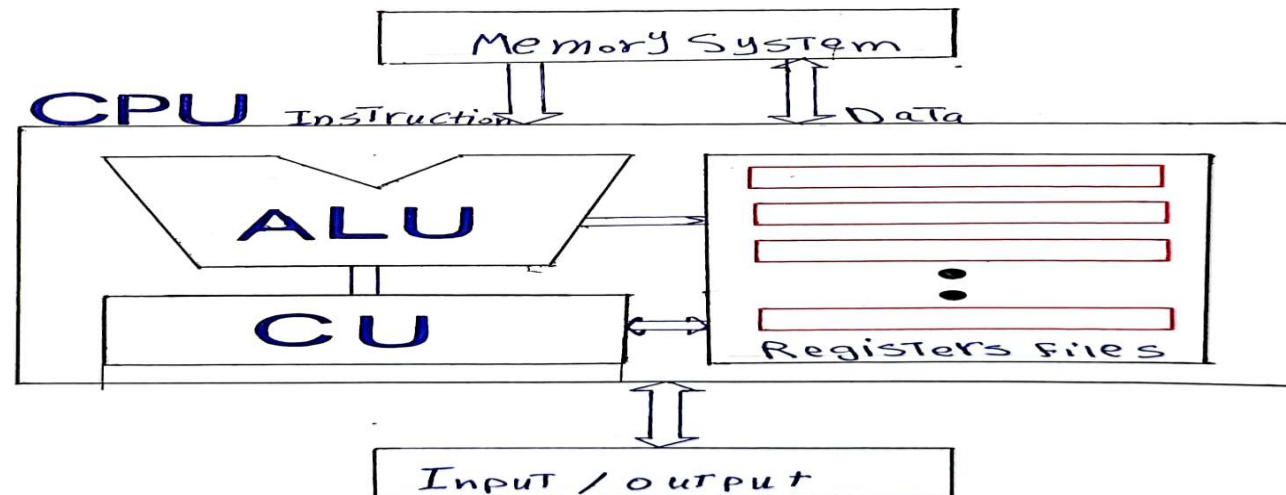
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## DIFFERENCE BETWEEN PROCESSOR, MICROPROCESSOR, AND CPU ?

- Processor : In the past to be made of vacuum tube and has a large size and process fewer operations
- Microprocessor : It made of transistor and has a small size and process many operations
- CPU : (Central Processing Unit) Be the main processor or primary processor in the system and master to other microprocessors slaves like (GPU, DSP, etc....) in the system

## HAND DRAWING OF PROCESSOR COMPONENTS (CU, ALU, REG FILE, ETC...)

CPU : Central processing unit  
ALU : Arithmetic and Logic unit  
CU : Control Unit  
REG : Register Files:  
• PC : Program Counter  
• IR : Instruction Register  
• PSW : Process Status Word  
• ACC : Accumulator  
• SP : Stack pointer



# CISC VS. RISC


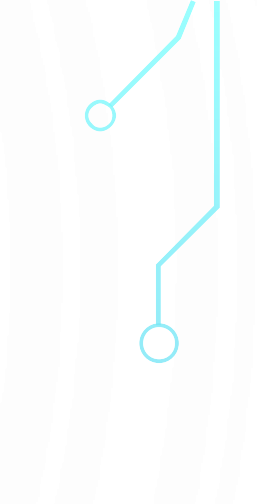
- **RISC** : (Reduce Instruction Set Computing) RISC architectures have a smaller and simpler instruction set
- **CISC** : (Complex Instruction Set Computing) CISC architectures have a large and complex instruction set with a wide variety of instructions.

Embedded System Challenges	RISC	CISC
<b>size</b>	ALU small , ID large	ALU large , ID small
<b>Performance</b>	Almost the same	
<b>Cost</b>	SW large , HW small	SW small , HW large
<b>Power</b>	ALU small , ID large	ALU large , ID small

- SW : Software | HW : Hardware | ID : Instruction Decoder | ALU : Arithmetic and Logic Unit



(BONUS) A CODE IS COMPILED FOR PROCESSOR X, COULD IT BE EXECUTED ON A PROCESSOR Y ? WHY ?

- If Processor X and Processor Y have the same architecture, meaning they share the same instruction set, the compiled code should be directly executable on both processors.
  - If Processor X and Processor Y have different architectures, the compiled code may not be directly executable. Different processor architectures have distinct instruction sets and internal structures, which means that the binary code produced by the compiler for one architecture may not be compatible with the instruction set of the other architecture
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