TASK 3

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WHAT ARE MEMORY TYPES ?

- 1) Volatile 2) Nonvolatile 3) Hybrid
- **Volatile :** RAM (Random Access Memory) Read and Write

SRAM	DRAM
• Static Ram • Based on transistors and the basic element in it is flipflop • Faster than DRAM • High cost per bit • Don't need to refreshment circuit	• Dynamic Ram • Based on capacitor and simple MOSEFT • Needed to refreshment circuit • Low cost per bit and simple HW • Can use it in high density

NONVOLATILE

- **ROM :** (Read Only Memory) and called also program memory slower than RAM and the has a large access time and based on floating gate MOSFET (FGM)

Mask programable ROM	PROM	EPROM
• OTP (one time program) • Used in factories in simple program such as toys • Used in BIOS chips	• OTP (one time program) • But programable by user for one time • Used in simple projects	• Erasable programable • Saved data for long time • But has disadvantages it's effect by noise and radiation due to destroy and corruption data

HYBRID

- **Hybrid :** is mixed of advantages of RAM and ROM and it's read and write memory

EEPROM	FLASH	NVRAM
• Electrical Erasable ROM • Endurance time 100.000 times • Access byte by byte • Expensive • High cost per bit	• Faster than EEPROM • Endurance time 10.000 • Access sector by sector • Low cost per bit • High density	• Consists of SRAM and battery • Or Consists of SRAM and battery and EEPROM

PROCESSOR DIFFERENT BUSES ?

- **Address bus** : It is used to specify a physical address in the system memory where data is to be read from or written to
- **Data bus** : It carries the actual data being transferred between the processor and memory or between different components
- **Control bus** : It carries control signals that manage and coordinate the activities of the various components in the computer system, such as memory read/write signals, interrupt signals, and clock signals

VON NEUMANN VS HARVARD ARCHITECTURE ?

- **Von Neumann :** in Von Neumann architecture the RAM and ROM and Input output all have the same section and connect to CPU by one bus set only (address bus ,data bus, control bus) every one of them has a range of address to dealing with CPU and in this architecture the CPU can't deal with them at the same time
- **Harvard :** in Harvard architecture the RAM and ROM and Input output every one of them has a section and bus set to dealing with CPU and in this architecture the CPU can deal with them at the same time

WHAT IS PIPELINE ?

- A pipeline refers to a technique used in the processor architecture to improve the overall efficiency of instruction execution and can execute more than one instruction at the same cycle (clock)
- (Fetch => Fetching the instruction from memory)
- (Decode => Decoding the instruction to determine the operation to be performed)
- (Execute => Executing the operation specified by the instruction)

(BONUS) OPEN THE DATASHEET OF THE MICROCONTROLLER ATMEL AVR ATMEGA32 AND TAKE A SCREENSHOT

Features

- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- Nonvolatile Program and Data Memories
  - 32K Bytes of In-System Self-Programmable Flash
    Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - 1024 Bytes EEPROM
    Endurance: 100,000 Write/Erase Cycles
  - 2K Byte Internal SRAM
  - Programming Lock for Software Security
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four PWM Channels
  - 8-channel, 10-bit ADC
    8 Single-ended Channels
    7 Differential Channels in TQFP Package Only
    2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages
  - 32 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, and 44-pad MLF
- Operating Voltages
  - 2.7 - 5.5V for ATmega32L
  - 4.5 - 5.5V for ATmega32
- Speed Grades
  - 0 - 8 MHz for ATmega32L
  - 0 - 16 MHz for ATmega32
- Power Consumption at 1 MHz, 3V, 25°C for ATmega32L
  - Active: 1.1 mA
  - Idle Mode: 0.35 mA
  - Power-down Mode: < 1 µA

ATMEL®

8-bit AVR® Microcontroller with 32K Bytes In-System Programmable Flash

ATmega32
ATmega32L

Preliminary

2503F–AVR–12/03

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