Project 2

Verilog Implementation of

SPI Interface with Single Port Synchronous RAM

Digital Design & Verification Diploma

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Ex-Visiting Student at Southern Illinois University Edwardsville, USA [Read my story]

Table of Content:

1. Project Description ………..…………………………………….. ….……………….... 3
2. Questa Sim Snippets ……..……..……………………………….. …………………. 7
3. Linting Results …………..…………………………….……………………….. 8
4. Elaboration ……………..…………………………….……………….. …................... 9
5. Synthesis ………………………………………………………….………………. 10
    a. Sequential Encoding …...………………………………………….…………..... 12
    b. Gray Encoding …………………………………………………….………….... 14
    c. One-hot Encoding ………………………………………………….………….. 16
6. Implementation …………………………………………………………………… 19
    a. Sequential Encoding …...………………………………………….…………… 19
    b. Gray Encoding ……………………………………………………..…………... 21
    c. One-hot Encoding ………………………………………………...………….. 24
7. Bitstream Generation ……………………………………………………………... 26

1. PROJECT DESCRIPTION:

This project implements a **Serial Peripheral Interface (SPI) slave module** integrated with a **single-port asynchronous RAM**. The system is designed to receive serial data from a master device, decode commands, and interact with memory for reading and writing operations. The goal is to simulate, synthesize, and implement a complete digital communication and memory management system on an FPGA platform.

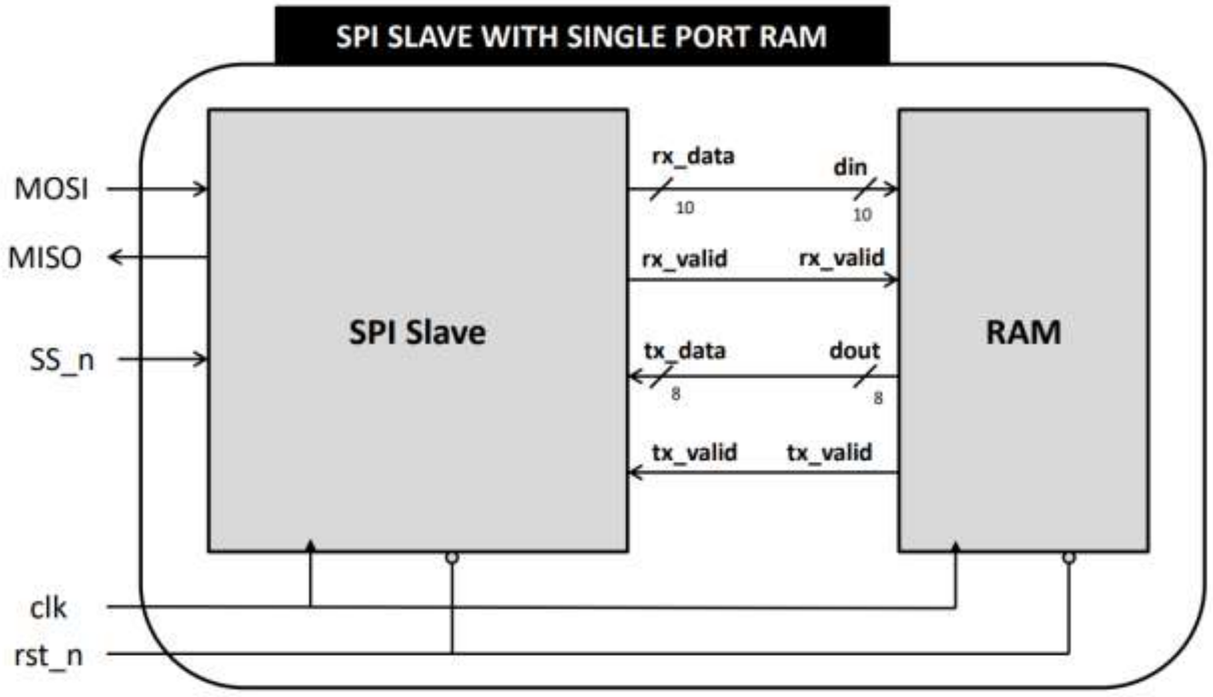


Figure 1 shows the SPI Slave Interface with Single Port Synchronous RAM

System Overview

The design is composed of three primary components, shown in Figure 1:

1. **SPI Slave Module:**
   Handles communication with the SPI master, captures incoming serial data, and forwards it to the memory interface.
2. **Single-Port Async RAM Module:**
   A memory block that executes read and write operations based on encoded instructions in the SPI stream.
3. **Top-Level System Integration Module:**
   Connects the SPI and RAM blocks together and facilitates system-level operation.

Module Interfaces:

a. SPI Slave Module

Signal	**Direction**	**Width**	**Description**
clk	Input	1 bit	System clock
rst_n	Input	1 bit	Active-low reset
SS_n	Input	1 bit	Slave Select from master
MOSI	Input	1 bit	Serial data from master
tx_data	Input	8 bit	Data received from RAM
tx_valid	Input	1 bit	Data validity indicator
MISO	Output	1 bit	Serial data to master
rx_data	Output	10 bit	Parallel data to be sent to RAM (from MOSI)
rx_valid	Output	1 bit	Indicates if rx_data is valid

Table 1 SPI Slave Module I/O Ports

b. Single-Port Sync RAM

Signal	**Direction**	**Width**	**Description**
clk	Input	1 bit	System clock
rst_n	Input	1 bit	Active-low reset
din	Input	10 bit	Command and data from SPI
rx_valid	Input	1 bit	Enables operation based on din[9:8]
dout	Output	8 bit	Data read from memory
tx_valid	Output	1 bit	HIGH when data on dout is valid (read operation)

Table 2 Single-Port Synchronous RAM Module I/O Ports

c. Command Encoding via din[9:8]

din[9:8]	Operation	Description
00	**Set Write Addr**	**Stores din[7:0] as internal write address**
01	**Write Data**	**Writes din[7:0] to stored write address**
10	**Set Read Addr**	**Stores din[7:0] as internal read address**
11	**Read Data**	**Outputs word at stored read address via dout**

Table 3 shows Operation executed for each din[9:8] case

FSM Overview:

The SPI Slave operates based on a **five-state FSM** that responds to the SS_n (Slave Select) and MISO signals. It transitions between states depending on whether data is being written to or read from the RAM and what kind of command is received from the SPI Master.

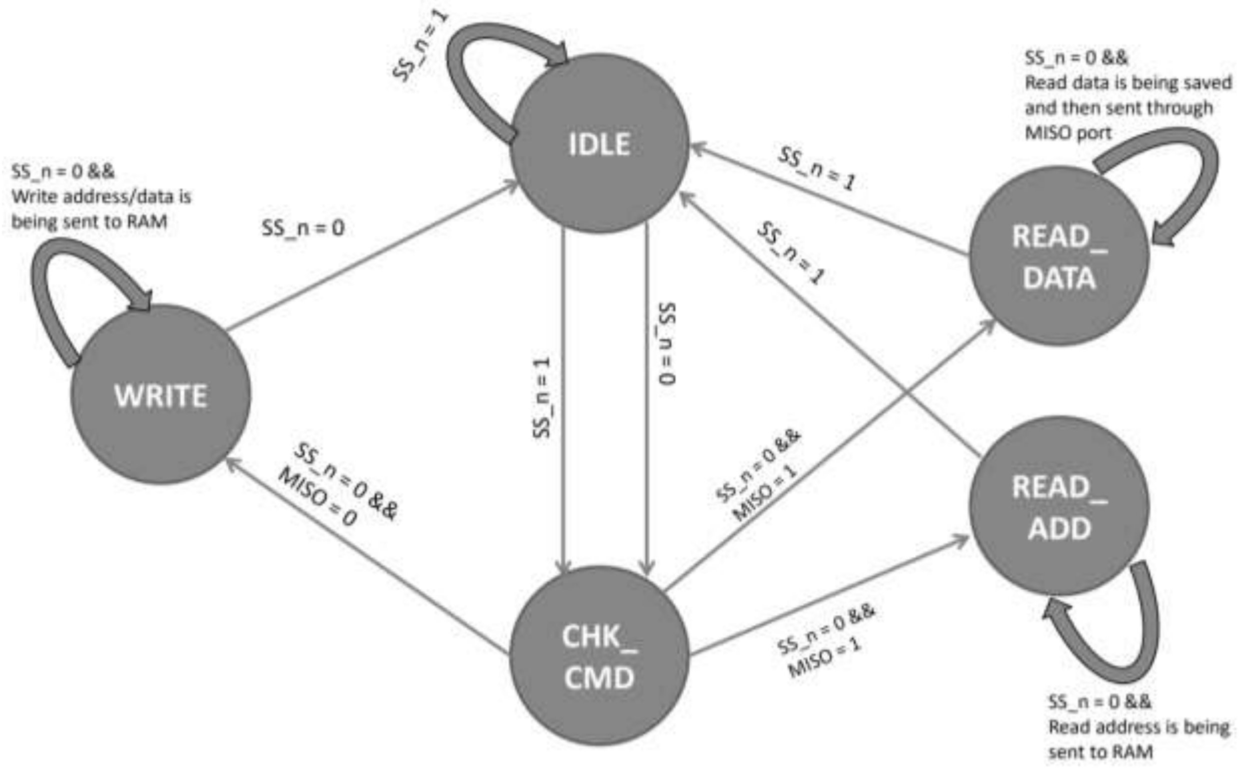

SS_n = 1
IDLE
SS_n = 0 && Write address/data is being sent to RAM
SS_n = 0
WRITE
SS_n = 1
SS_n = 0
SS_n = 1
SS_n = 1
SS_n = 0 && Read data is being saved and then sent through MISO port
READ_ DATA
SS_n = 0 && MISO = 0
SS_n = 0 && MISO = 1
READ_ ADD
CHK_ CMD
SS_n = 0 && MISO = 1
SS_n = 0 && Read address is being sent to RAM

Figure 2 shows the Finite State Machine Diagram describing SPI State Transitions

Testbench Plan:

1. **Reset Behavior:**

The testbench starts with rst_n = 0, MOSI = 0, and SS_n = 1 to simulate an idle SPI bus during reset. After 10 time units, rst_n is set to 1, releasing the system from reset. Although no direct self-check is included for reset, we expect internal signals like wr_address, rd_address, dout, and memory contents to initialize to ZERO. The success of all the following operations indirectly confirms that reset behavior is correct.

2. **Write Address Command:**

To test the Write Address command, a 10-bit SPI word 00_11110001 is sent via MOSI, with SS_n = 0 held low for the duration. Here, din[9:8] = 00 indicates a write address operation, and din[7:0] = 0xF1 is the target address. After all bits are shifted in, SS_n is raised to 1. The testbench then checks the value of uut.ram_inst.wr_address, which should be set to 8'hF1. This confirms that the SPI slave properly decoded and passed the address to the RAM module.

3. **Write Data Command:**

In this test, the value 01_01110111 is transmitted bit-by-bit through MOSI with SS_n = 0. The command prefix din[9:8] = 01 represents a write operation, and din[7:0] = 0x77 is the data to be stored. The RAM is expected to write this data at the previously stored wr_address = 0xF1. After transmission, SS_n is set to 1, and the testbench verifies that uut.ram_inst.ram[uut.ram_inst.wr_address] holds 8'h77. This confirms that the write command was correctly processed and executed.

4. **Read Address Command:**

To initiate a read, the SPI slave receives the command 10_11110001, with SS_n = 0 during transmission. Here, din[9:8] = 10 signals a read address setup, and din[7:0] = 0xF1 is the target address. After the 10-bit word is sent and SS_n is pulled high, the testbench checks uut.ram_inst.rd_address, which should now equal 8'hF1. This verifies that the SPI interface correctly captured and routed the read address to the RAM.

5. **Read Data Command:**

The final test transmits 11_00011011 through MOSI with SS_n = 0. The prefix din[9:8] = 11 triggers a memory read, and the lower din[7:0] bits are ignored. The RAM module uses the previously set rd_address = 0xF1 to fetch data and outputs it on dout. After SS_n is set to 1, the testbench checks if uut.ram_inst.dout is equal to 8'h77. If so, this confirms that the full read operation—from SPI command to memory access—was completed correctly.

2. QUESTA SIM SNIPPETS: SUCCESS

The output waveform of the simulation in Questa Sim shows correct transitions between states as intended: 0 → 3 → 4 → 0 → 3 → 4 → 0 → 3 → 2 → 0 → 3 → 1 → 0, as shown in Figures 3 - 4.

WHERE, 0 → IDLE, 1 → READ_DATA, 2 → READ_ADD, 3 → CHK_MD, 4 → WRITE

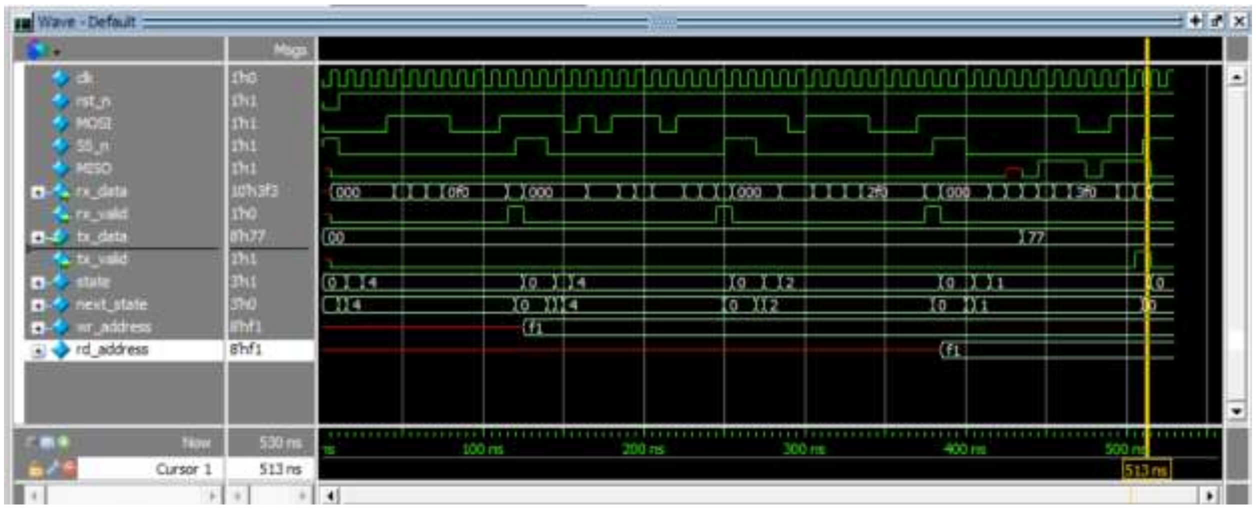
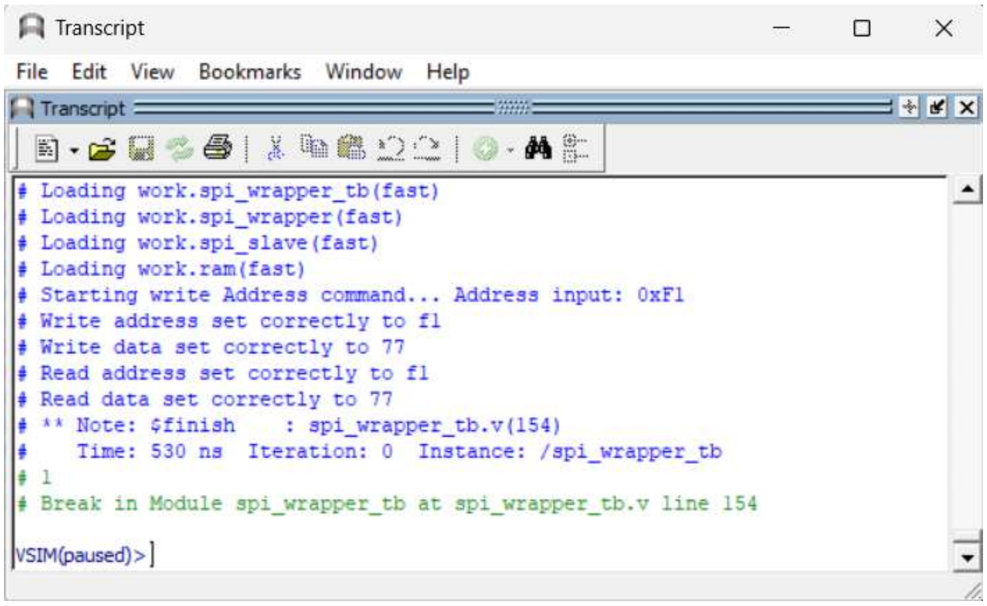


Figure 3 shows simulation output in Questa Sim Verifying successful State transitions and Logic Outputs

The output waveform also shows the correct Reading and Storage of the Input Write Address, followed by successful writing in RAM at the stored Address, as shown in Figures 3 - 4.

In Addition, the SPI and RAM Modules designed have successfully read and stored the Input Read Address, followed by successful Reading from the stored Address as shown in Figures 3 - 4.



```
# Loading work.spi_wrapper_tb(fast)
# Loading work.spi_wrapper(fast)
# Loading work.spi_slave(fast)
# Loading work.ram(fast)
# Starting write Address command... Address input: 0xF1
# Write address set correctly to f1
# Write data set correctly to 77
# Read address set correctly to f1
# Read data set correctly to 77
# ** Note: $finish    : spi_wrapper_tb.v(154)
#    Time: 530 ns  Iteration: 0  Instance: /spi_wrapper_tb
# 1
# Break in Module spi_wrapper_tb at spi_wrapper_tb.v line 154

VSIM(paused)>
```

Figure 4 shows the self-checking conditions outputs in the Transcript Tab

3. LINTING RESULTS: SUCCESS

Figures 5-6 show the generated Schematic of the SPI interface with the RAM, and the "Lint Checks" with no Errors, respectively.

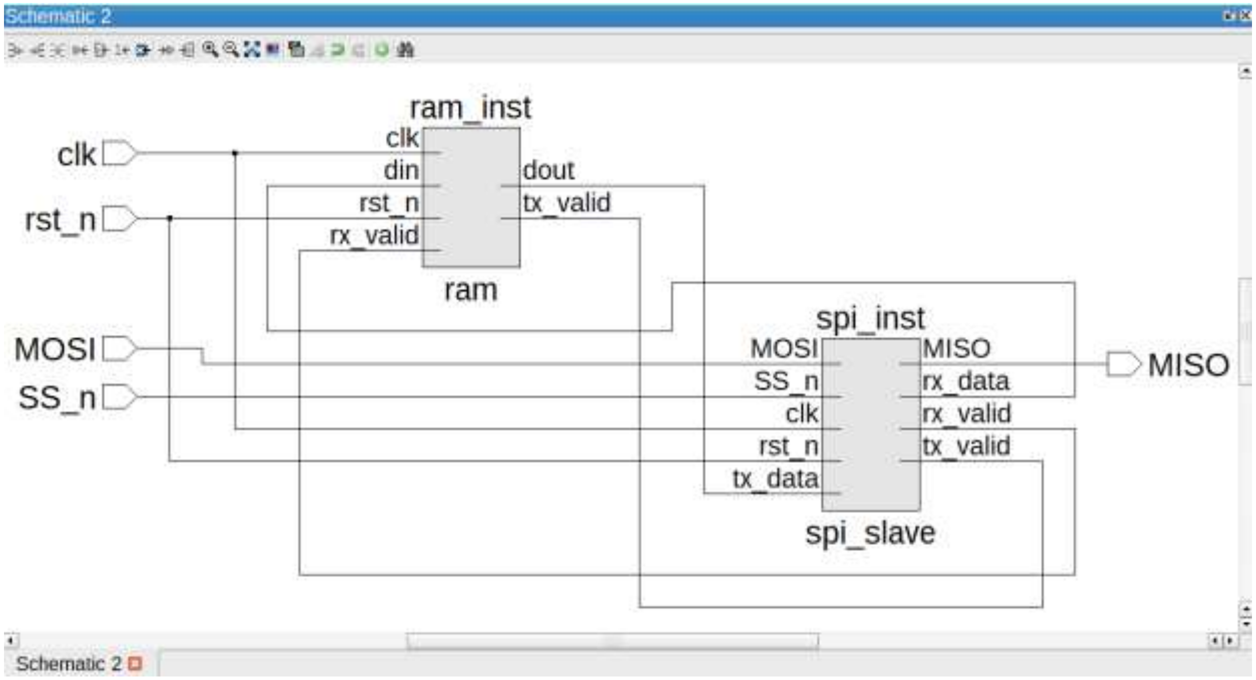
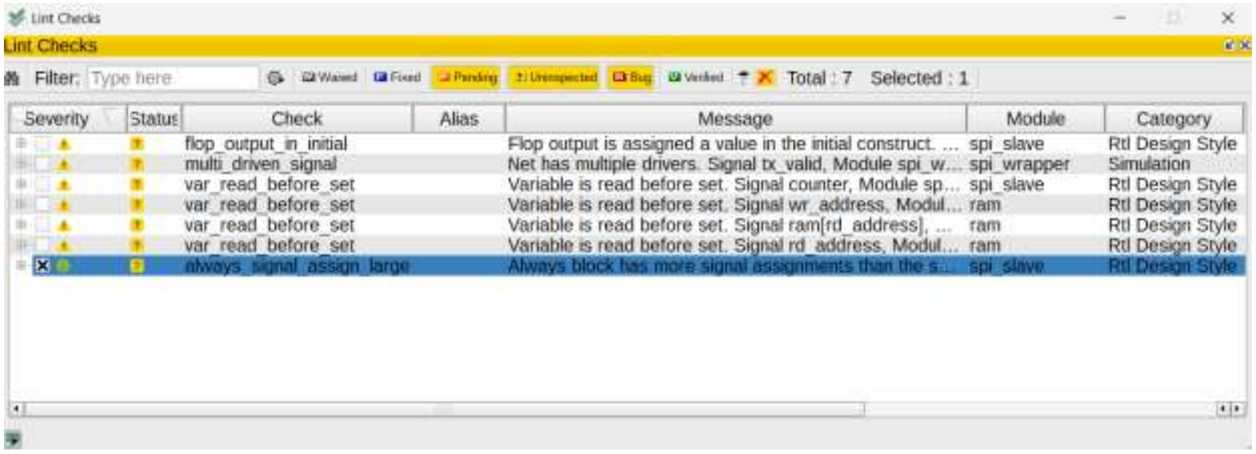


Figure 5 shows the SPI interface with RAM Schematic generated by Questa Lint



Total : 7 Selected : 1

Severity	Status	Check	Alias	Message	Module	Category
▲	?	flop_output_in_initial		Flop output is assigned a value in the initial construct. ...	spi_slave	Rtl Design Style
▲	?	multi_driven_signal		Net has multiple drivers. Signal tx_valid, Module spi_w...	spi_wrapper	Simulation
▲	?	var_read_before_set		Variable is read before set. Signal counter, Module sp...	spi_slave	Rtl Design Style
▲	?	var_read_before_set		Variable is read before set. Signal wr_address, Modul...	ram	Rtl Design Style
▲	?	var_read_before_set		Variable is read before set. Signal ram[rd_address], ...	ram	Rtl Design Style
▲	?	var_read_before_set		Variable is read before set. Signal rd_address, Modul...	ram	Rtl Design Style
☒ ●	?	always_signal_assign_large		Always block has more signal assignments than the s...	spi_slave	Rtl Design Style

Figure 6 shows the Lint Checks outputs - ZERO Errors

4. ELABORATION:

System Level Schematic:

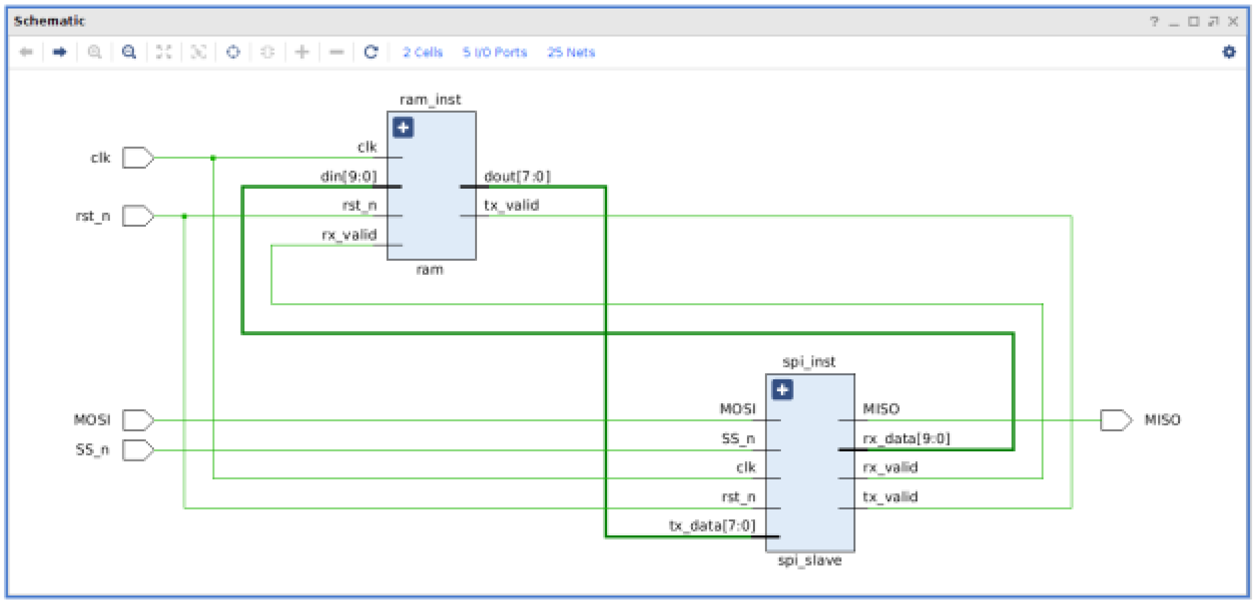


Figure 7 shows output system level schematic generated in Elaboration

SPI Level Schematic:

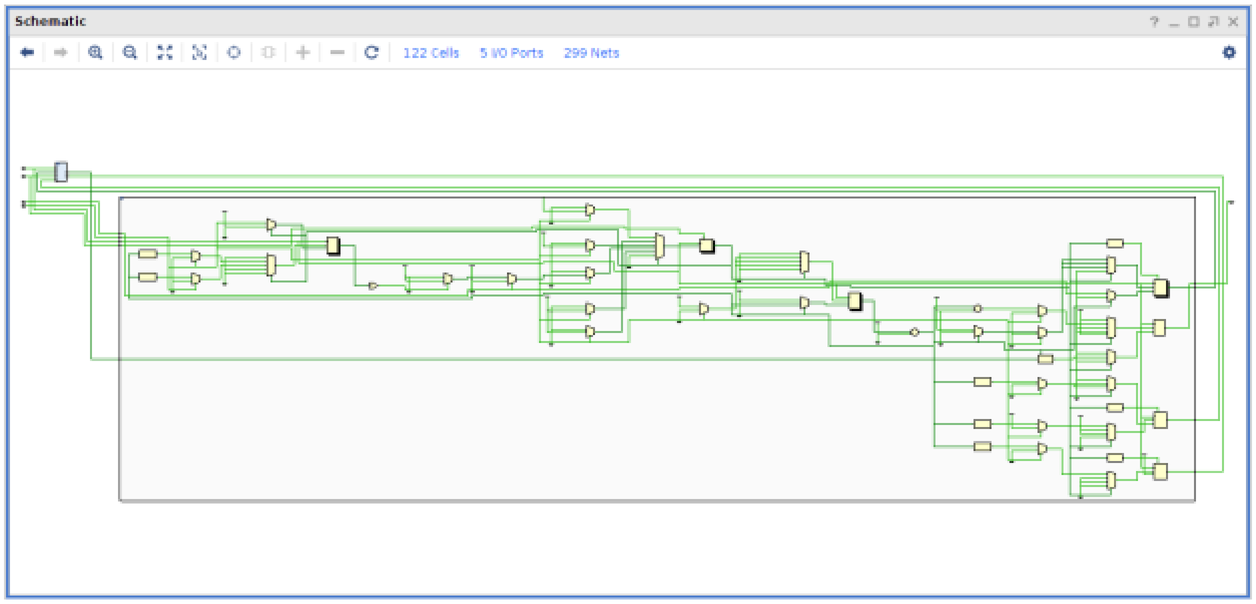


Figure 8 shows the SPI Level Schematic generated in Elaboration

RAM Level Schematic:

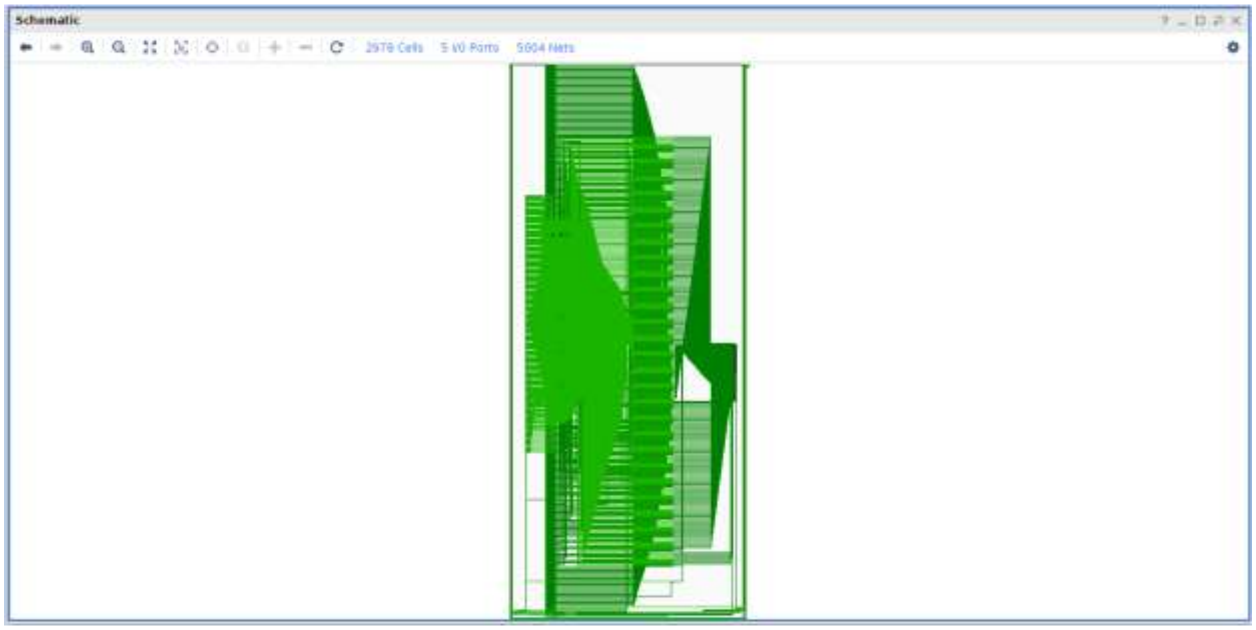


Figure 9 shows the RAM Level Schematic generated in Elaboration

5. SYNTHESIS:

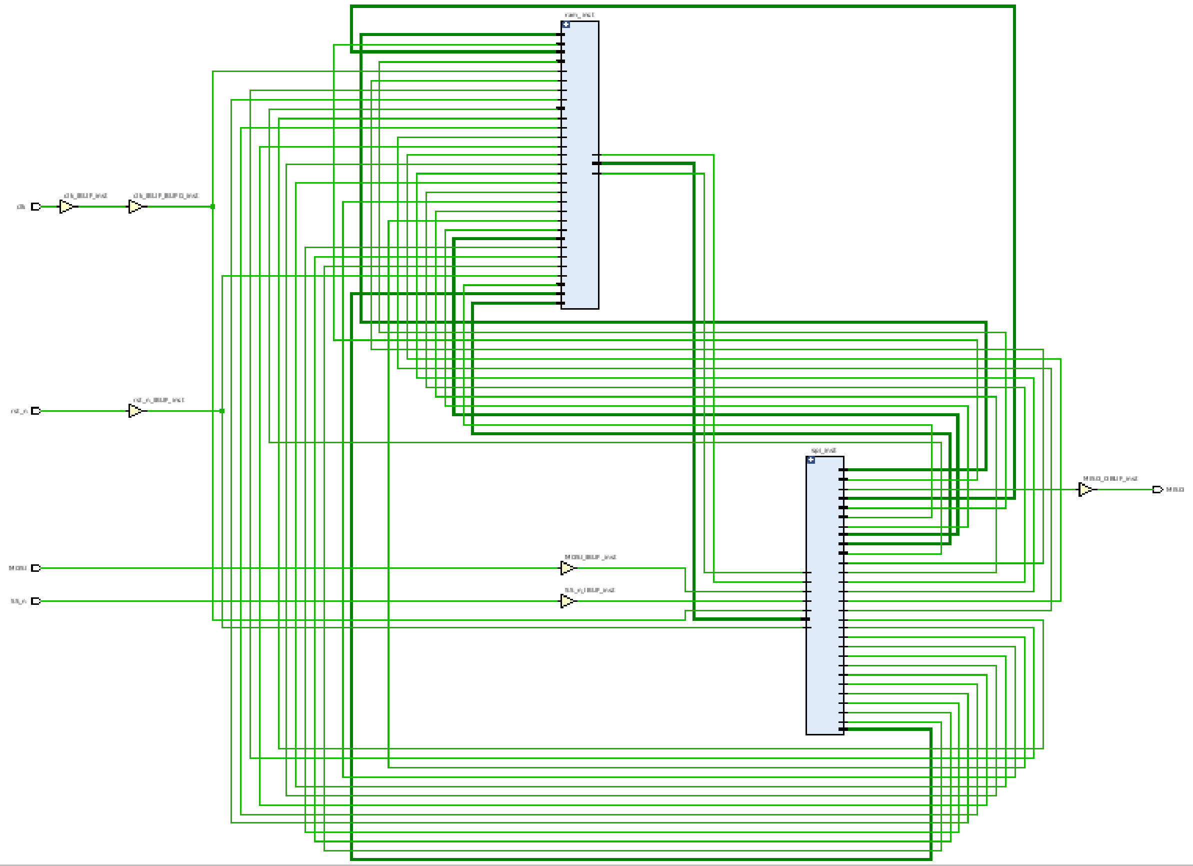
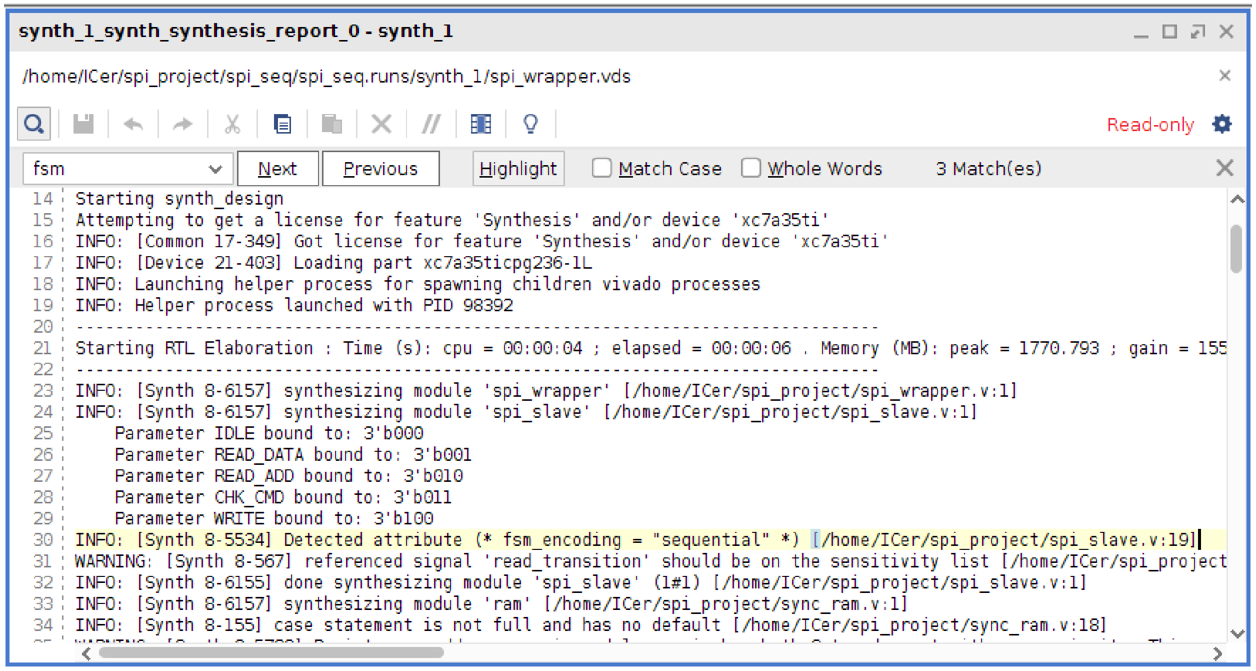


Figure 10 shows the schematic generated through Synthesis

a. Seq Encoding:

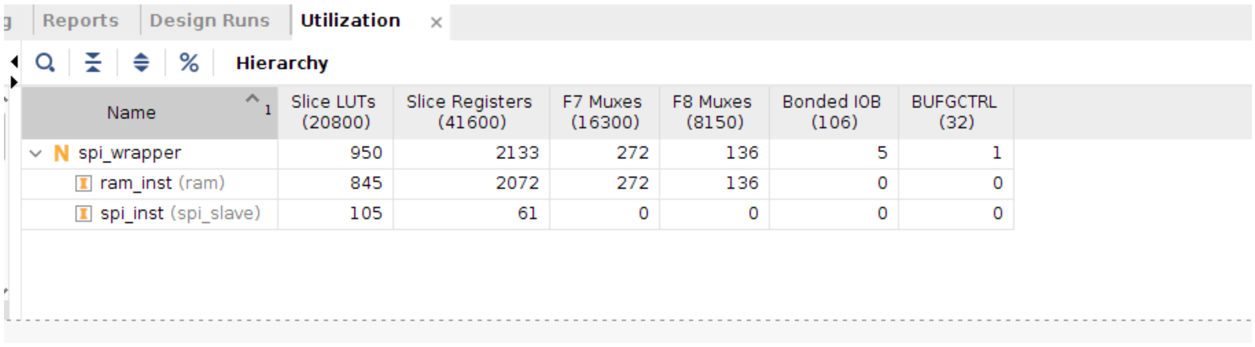


synth_1_synth_synthesis_report_0 - synth_1

/home/ICer/spi_project/spi_seq/spi_seq.runs/synth_1/spi_wrapper.vds

```
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35ti'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
INFO: [Device 21-403] Loading part xc7a35ticpg236-1L
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 98392
---------------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:04 ; elapsed = 00:00:06 . Memory (MB): peak = 1770.793 ; gain = 155
---------------------------------------------------------------------------------
INFO: [Synth 8-6157] synthesizing module 'spi_wrapper' [/home/ICer/spi_project/spi_wrapper.v:1]
INFO: [Synth 8-6157] synthesizing module 'spi_slave' [/home/ICer/spi_project/spi_slave.v:1]
    Parameter IDLE bound to: 3'b000
    Parameter READ_DATA bound to: 3'b001
    Parameter READ_ADD bound to: 3'b010
    Parameter CHK_CMD bound to: 3'b011
    Parameter WRITE bound to: 3'b100
INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "sequential" *) [/home/ICer/spi_project/spi_slave.v:19]
WARNING: [Synth 8-567] referenced signal 'read_transition' should be on the sensitivity list [/home/ICer/spi_project
INFO: [Synth 8-6155] done synthesizing module 'spi_slave' (1#1) [/home/ICer/spi_project/spi_slave.v:1]
INFO: [Synth 8-6157] synthesizing module 'ram' [/home/ICer/spi_project/sync_ram.v:1]
INFO: [Synth 8-155] case statement is not full and has no default [/home/ICer/spi_project/sync_ram.v:18]
```

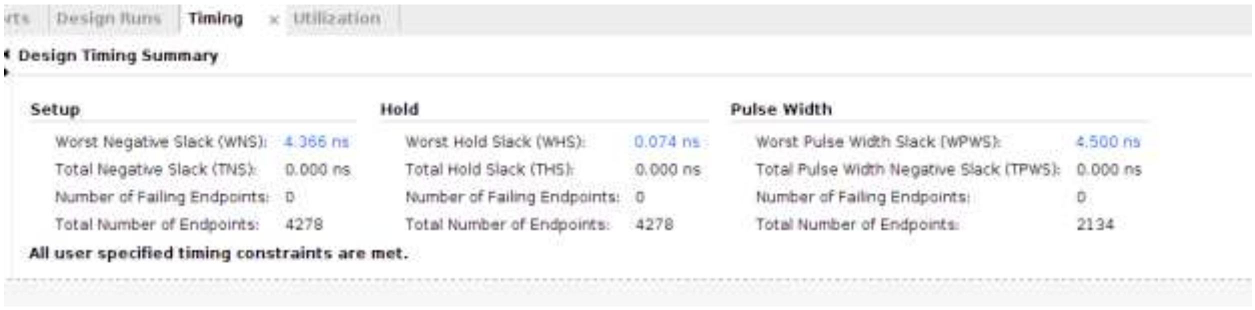
Figure 11 shows the report synthesis of Sequential Encoding highlighted in yellow



Utilization — Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Bonded IOB (106)	BUFGCTRL (32)
spi_wrapper	950	2133	272	136	5	1
ram_inst (ram)	845	2072	272	136	0	0
spi_inst (spi_slave)	105	61	0	0	0	0

Figure 12 shows the Utilization Report generated through Synthesis of Seq encoded SPI

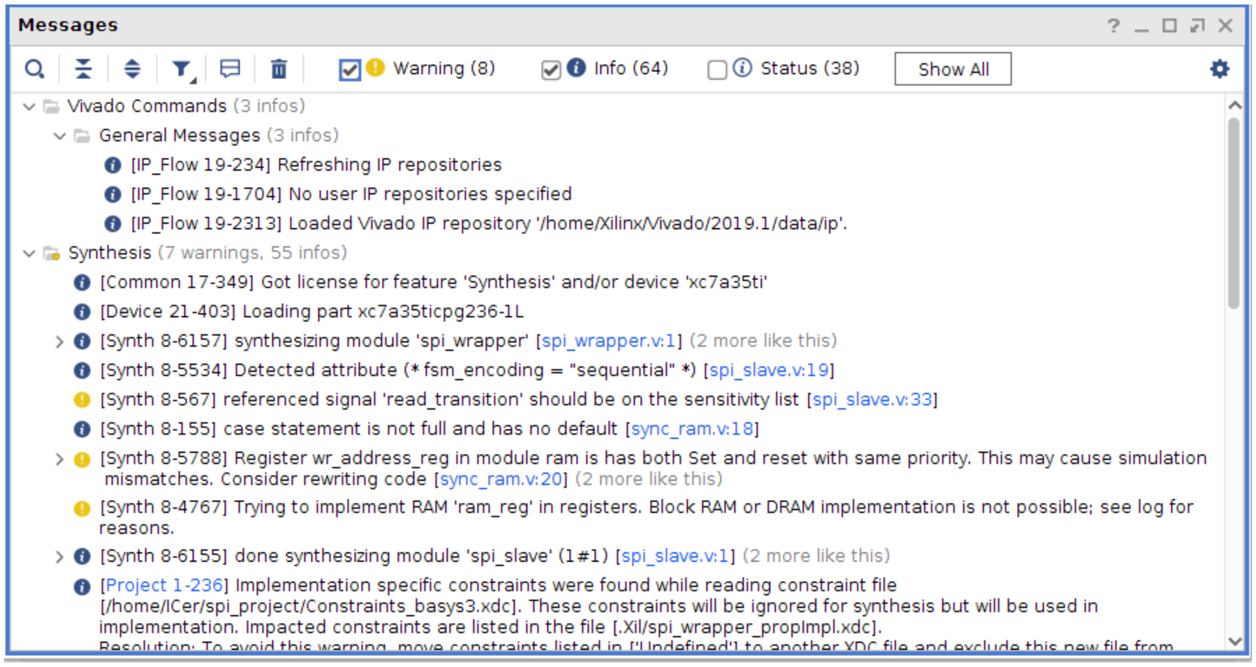


Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	4.366 ns	Worst Hold Slack (WHS):	0.074 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4278	Total Number of Endpoints:	4278	Total Number of Endpoints:	2134

All user specified timing constraints are met.

Figure 13 shows the Timing Report generated through Synthesis of Seq encoded SPI

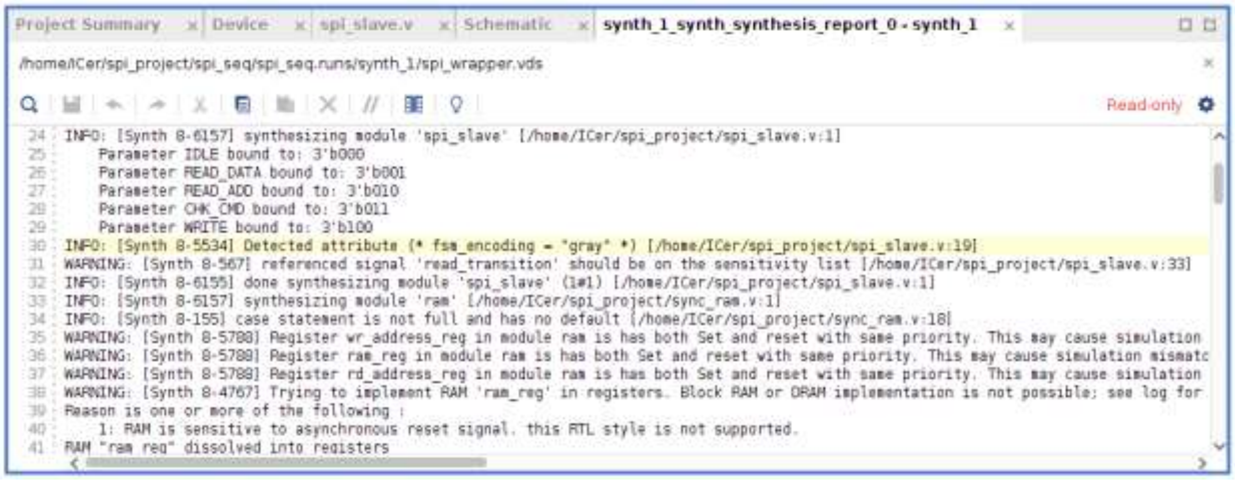

Messages

Warning (8) Info (64) Status (38) Show All

```
Vivado Commands (3 infos)
  General Messages (3 infos)
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository '/home/Xilinx/Vivado/2019.1/data/ip'.
Synthesis (7 warnings, 55 infos)
  [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
  [Device 21-403] Loading part xc7a35ticpg236-1L
  [Synth 8-6157] synthesizing module 'spi_wrapper' [spi_wrapper.v:1] (2 more like this)
  [Synth 8-5534] Detected attribute (* fsm_encoding = "sequential" *) [spi_slave.v:19]
  [Synth 8-567] referenced signal 'read_transition' should be on the sensitivity list [spi_slave.v:33]
  [Synth 8-155] case statement is not full and has no default [sync_ram.v:18]
  [Synth 8-5788] Register wr_address_reg in module ram is has both Set and reset with same priority. This may cause simulation
   mismatches. Consider rewriting code [sync_ram.v:20] (2 more like this)
  [Synth 8-4767] Trying to implement RAM 'ram_reg' in registers. Block RAM or DRAM implementation is not possible; see log for
  reasons.
  [Synth 8-6155] done synthesizing module 'spi_slave' (1#1) [spi_slave.v:1] (2 more like this)
  [Project 1-236] Implementation specific constraints were found while reading constraint file
  [/home/ICer/spi_project/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in
  implementation. Impacted constraints are listed in the file [.Xil/spi_wrapper_propImpl.xdc].
  Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file from
```

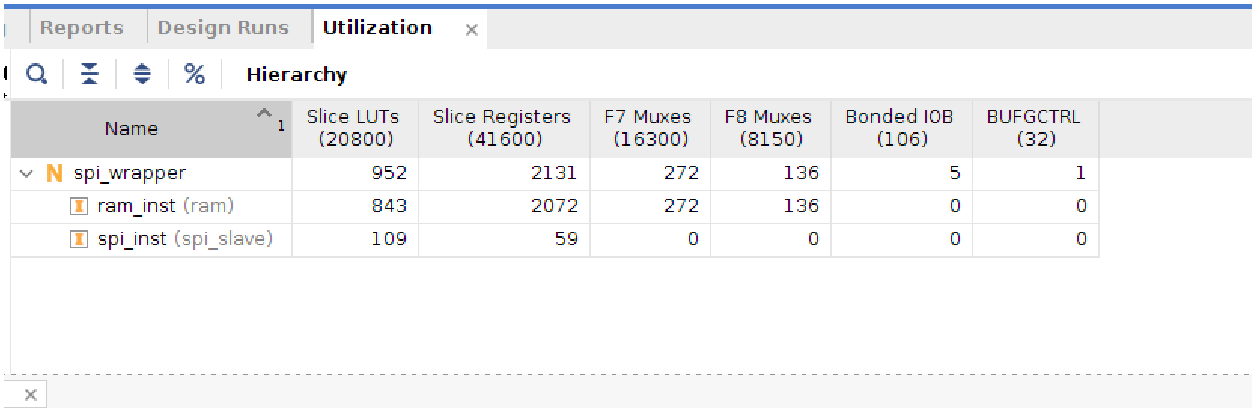
Figure 14 shows the "Messages" Tab with no Errors After Seq Encoding Synthesis

b. Gray Encoding



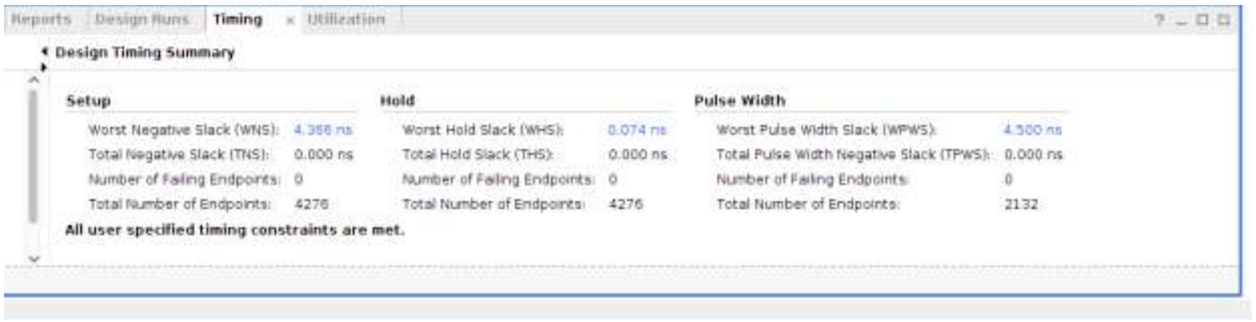
```
/home/ICer/spi_project/spi_seq/spi_seq.runs/synth_1/spi_wrapper.vds
INFO: [Synth 8-6157] synthesizing module 'spi_slave' [/home/ICer/spi_project/spi_slave.v:1]
    Parameter IDLE bound to: 3'b000
    Parameter READ_DATA bound to: 3'b001
    Parameter READ_ADD bound to: 3'b010
    Parameter CHK_CMD bound to: 3'b011
    Parameter WRITE bound to: 3'b100
INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [/home/ICer/spi_project/spi_slave.v:19]
WARNING: [Synth 8-567] referenced signal 'read_transition' should be on the sensitivity list [/home/ICer/spi_project/spi_slave.v:33]
INFO: [Synth 8-6155] done synthesizing module 'spi_slave' (1#1) [/home/ICer/spi_project/spi_slave.v:1]
INFO: [Synth 8-6157] synthesizing module 'ram' [/home/ICer/spi_project/sync_ram.v:1]
INFO: [Synth 8-155] case statement is not full and has no default [/home/ICer/spi_project/sync_ram.v:18]
WARNING: [Synth 8-5788] Register wr_address_reg in module ram is has both Set and reset with same priority. This may cause simulation
WARNING: [Synth 8-5788] Register ram_reg in module ram is has both Set and reset with same priority. This may cause simulation mismatc
WARNING: [Synth 8-5788] Register rd_address_reg in module ram is has both Set and reset with same priority. This may cause simulation
WARNING: [Synth 8-4767] Trying to implement RAM 'ram_reg' in registers. Block RAM or DRAM implementation is not possible; see log for
Reason is one or more of the following :
    1: RAM is sensitive to asynchronous reset signal. this RTL style is not supported.
RAM "ram_reg" dissolved into registers
```

Figure 15 shows the report synthesis of Gray Encoding highlighted in yellow



Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Bonded IOB (106)	BUFGCTRL (32)
spi_wrapper	952	2131	272	136	5	1
ram_inst (ram)	843	2072	272	136	0	0
spi_inst (spi_slave)	109	59	0	0	0	0

Figure 16 shows the Utilization Report generated through Synthesis of gray encoded SPI

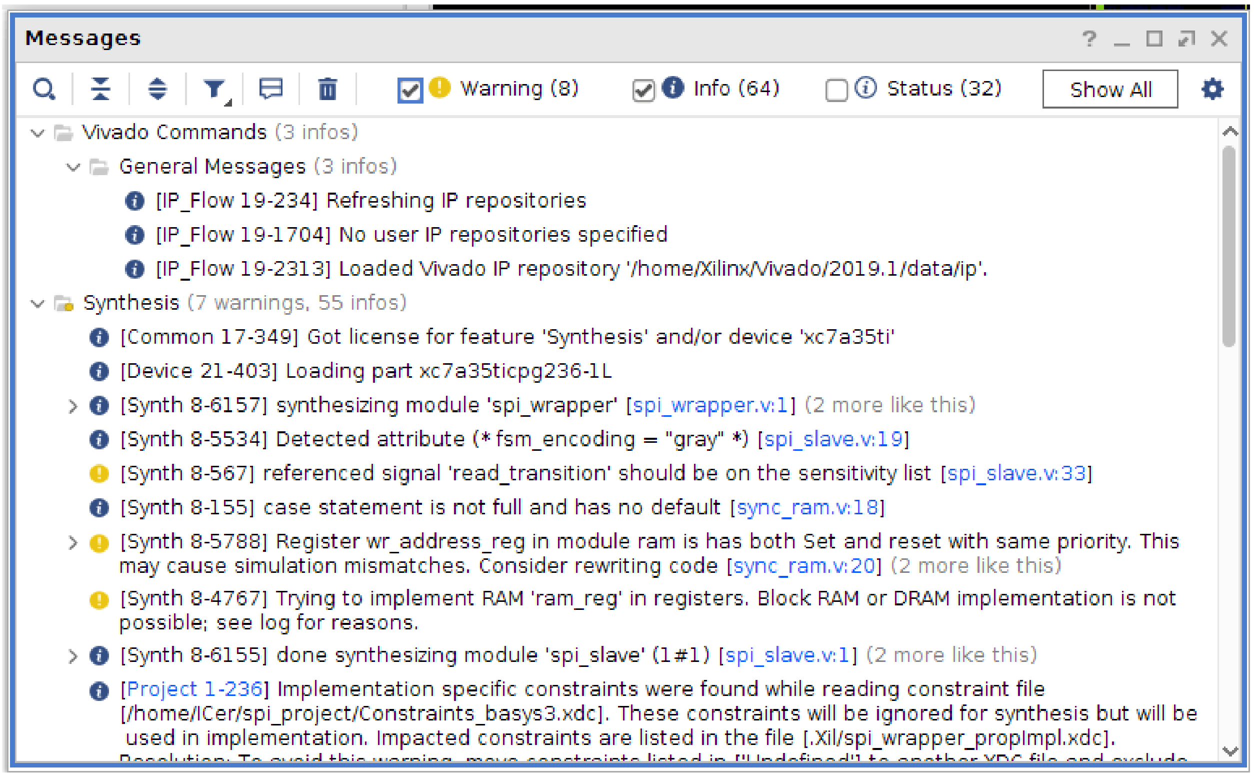


Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	4.366 ns	Worst Hold Slack (WHS):	0.074 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4276	Total Number of Endpoints:	4276	Total Number of Endpoints:	2132

All user specified timing constraints are met.

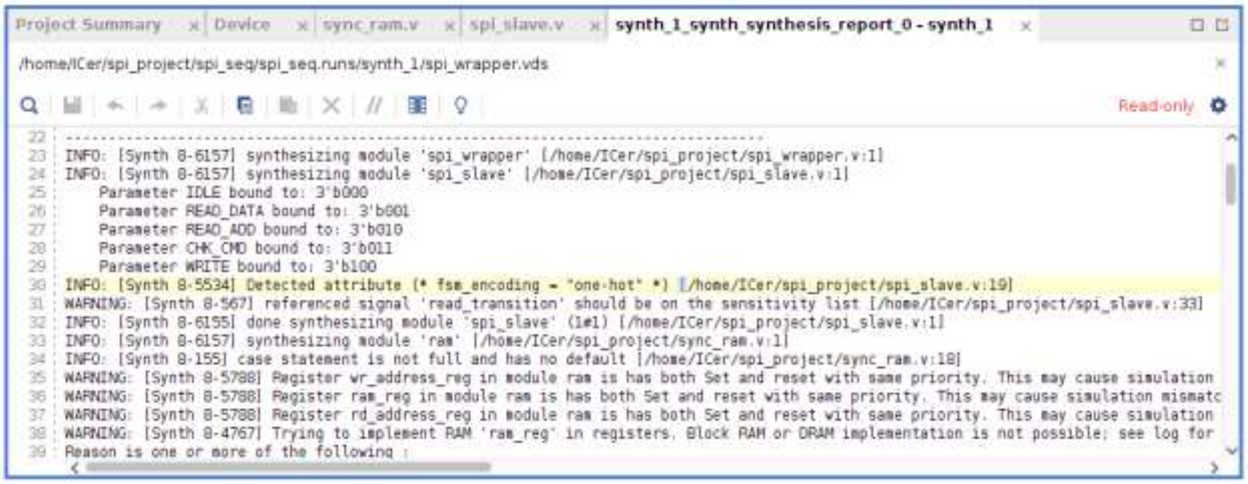
Figure 17 shows the Timing Report generated through Synthesis of gray encoded SPI



```
Vivado Commands (3 infos)
  General Messages (3 infos)
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository '/home/Xilinx/Vivado/2019.1/data/ip'.
Synthesis (7 warnings, 55 infos)
  [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
  [Device 21-403] Loading part xc7a35ticpg236-1L
  [Synth 8-6157] synthesizing module 'spi_wrapper' [spi_wrapper.v:1] (2 more like this)
  [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [spi_slave.v:19]
  [Synth 8-567] referenced signal 'read_transition' should be on the sensitivity list [spi_slave.v:33]
  [Synth 8-155] case statement is not full and has no default [sync_ram.v:18]
  [Synth 8-5788] Register wr_address_reg in module ram is has both Set and reset with same priority. This
  may cause simulation mismatches. Consider rewriting code [sync_ram.v:20] (2 more like this)
  [Synth 8-4767] Trying to implement RAM 'ram_reg' in registers. Block RAM or DRAM implementation is not
  possible; see log for reasons.
  [Synth 8-6155] done synthesizing module 'spi_slave' (1#1) [spi_slave.v:1] (2 more like this)
  [Project 1-236] Implementation specific constraints were found while reading constraint file
  [/home/ICer/spi_project/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be
   used in implementation. Impacted constraints are listed in the file [.Xil/spi_wrapper_propImpl.xdc].
```

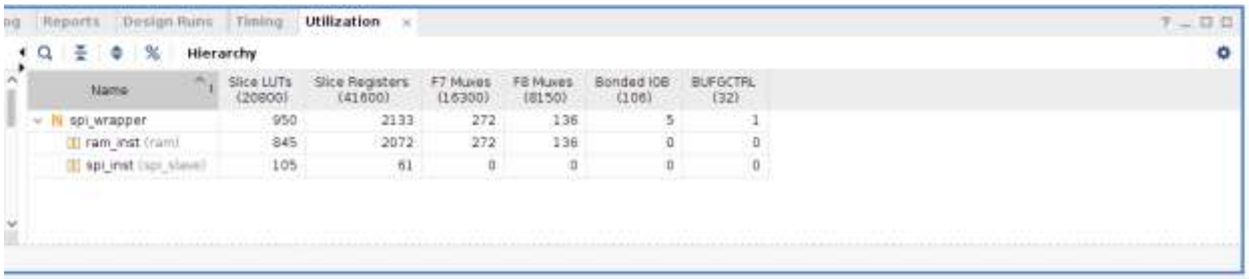
Figure 18 shows the "Messages" Tab with no Errors After Gray Encoding Synthesis

c. One-hot Encoding



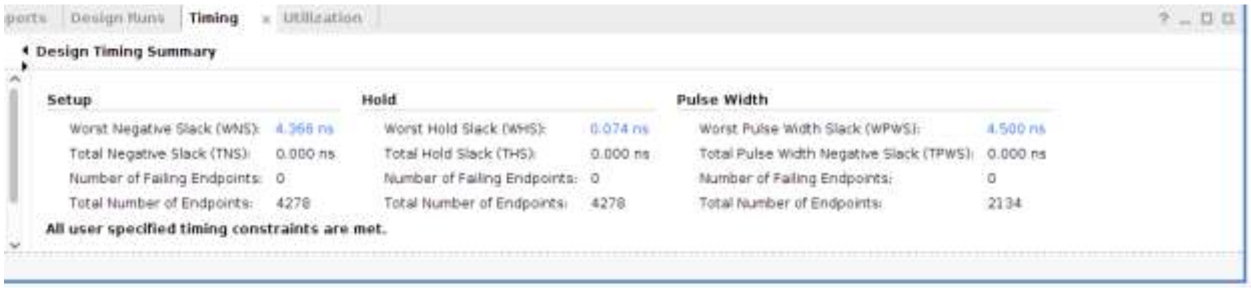
```
/home/ICer/spi_project/spi_seq/spi_seq.runs/synth_1/spi_wrapper.vds

---------------------------------------------------------------------------------
INFO: [Synth 8-6157] synthesizing module 'spi_wrapper' [/home/ICer/spi_project/spi_wrapper.v:1]
INFO: [Synth 8-6157] synthesizing module 'spi_slave' [/home/ICer/spi_project/spi_slave.v:1]
    Parameter IDLE bound to: 3'b000
    Parameter READ_DATA bound to: 3'b001
    Parameter READ_ADD bound to: 3'b010
    Parameter CHK_CMD bound to: 3'b011
    Parameter WRITE bound to: 3'b100
INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "one-hot" *) [/home/ICer/spi_project/spi_slave.v:19]
WARNING: [Synth 8-567] referenced signal 'read_transition' should be on the sensitivity list [/home/ICer/spi_project/spi_slave.v:33]
INFO: [Synth 8-6155] done synthesizing module 'spi_slave' (1#1) [/home/ICer/spi_project/spi_slave.v:1]
INFO: [Synth 8-6157] synthesizing module 'ram' [/home/ICer/spi_project/sync_ram.v:1]
INFO: [Synth 8-155] case statement is not full and has no default [/home/ICer/spi_project/sync_ram.v:18]
WARNING: [Synth 8-5788] Register wr_address_reg in module ram is has both Set and reset with same priority. This may cause simulation
WARNING: [Synth 8-5788] Register ram_reg in module ram is has both Set and reset with same priority. This may cause simulation mismatc
WARNING: [Synth 8-5788] Register rd_address_reg in module ram is has both Set and reset with same priority. This may cause simulation
WARNING: [Synth 8-4767] Trying to implement RAM 'ram_reg' in registers. Block RAM or DRAM implementation is not possible; see log for
Reason is one or more of the following :
```

Figure 20 shows the report synthesis of One-Hot Encoding highlighted in yellow



Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Bonded IOB (106)	BUFGCTRL (32)
spi_wrapper	950	2133	272	136	5	1
ram_inst (ram)	845	2072	272	136	0	0
spi_inst (spi_slave)	105	61	0	0	0	0

Figure 19 shows the Utilization Report generated through Synthesis of one-hot encoded SPI

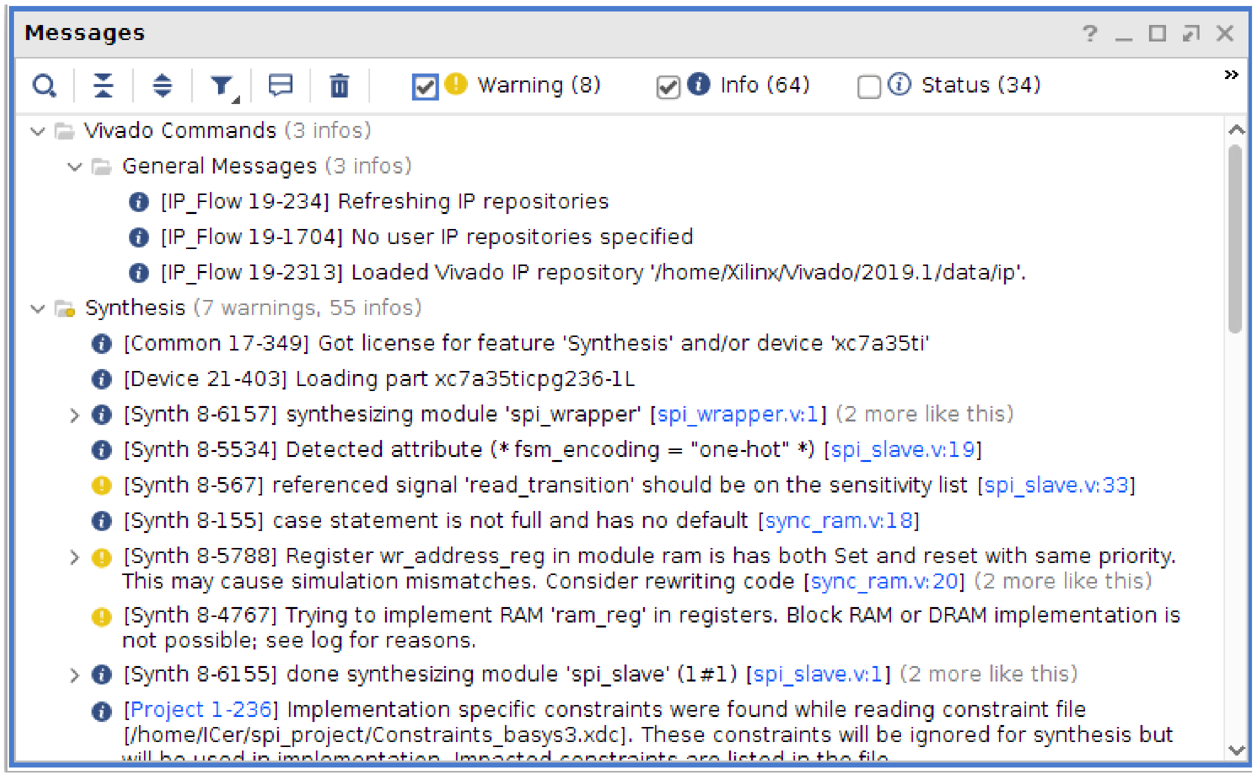


Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	4.368 ns	Worst Hold Slack (WHS):	0.074 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4278	Total Number of Endpoints:	4278	Total Number of Endpoints:	2134

All user specified timing constraints are met.

Figure 21 shows the Timing Report generated through Synthesis of one-hot encoded SPI



```
Vivado Commands (3 infos)
  General Messages (3 infos)
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository '/home/Xilinx/Vivado/2019.1/data/ip'.
Synthesis (7 warnings, 55 infos)
  [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
  [Device 21-403] Loading part xc7a35ticpg236-1L
  [Synth 8-6157] synthesizing module 'spi_wrapper' [spi_wrapper.v:1] (2 more like this)
  [Synth 8-5534] Detected attribute (* fsm_encoding = "one-hot" *) [spi_slave.v:19]
  [Synth 8-567] referenced signal 'read_transition' should be on the sensitivity list [spi_slave.v:33]
  [Synth 8-155] case statement is not full and has no default [sync_ram.v:18]
  [Synth 8-5788] Register wr_address_reg in module ram is has both Set and reset with same priority.
  This may cause simulation mismatches. Consider rewriting code [sync_ram.v:20] (2 more like this)
  [Synth 8-4767] Trying to implement RAM 'ram_reg' in registers. Block RAM or DRAM implementation is
  not possible; see log for reasons.
  [Synth 8-6155] done synthesizing module 'spi_slave' (1#1) [spi_slave.v:1] (2 more like this)
  [Project 1-236] Implementation specific constraints were found while reading constraint file
  [/home/ICer/spi_project/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but
```

Figure 22 shows the "Messages" Tab with no Errors After One-Hot Encoding Synthesis

Critical Path:

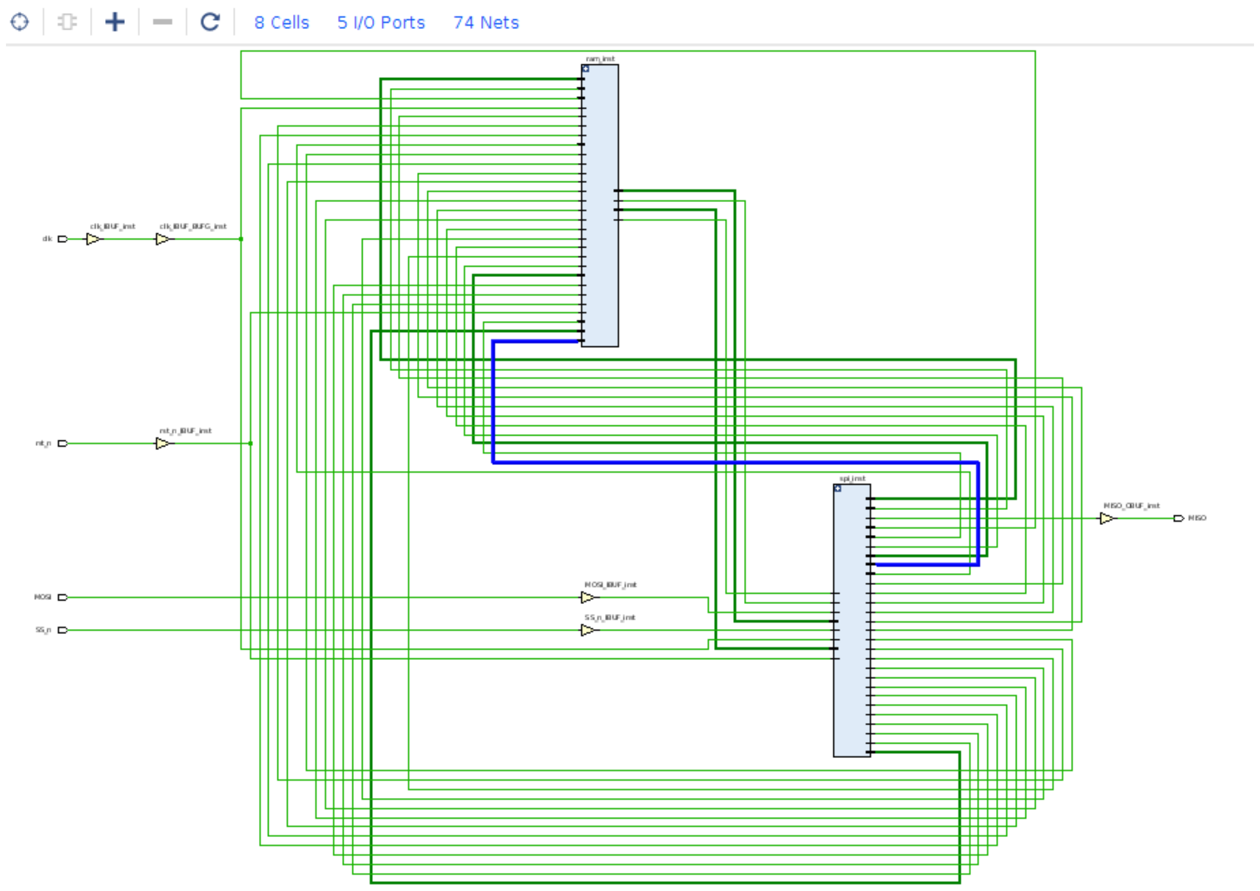


Figure 23 shows the critical path as calculated after Synthesis

6. IMPLEMENTATION:

a. Gray Encoding:

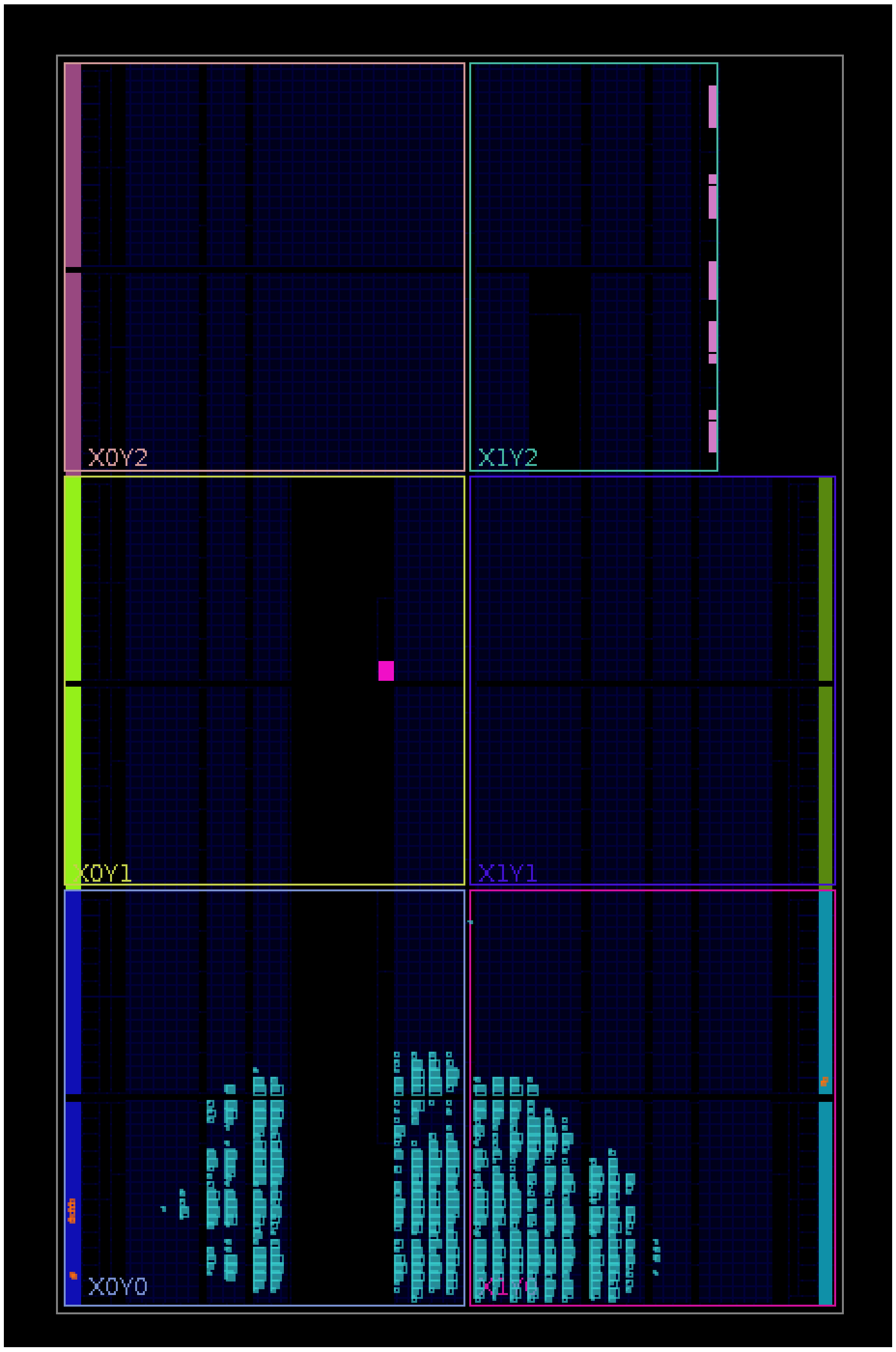
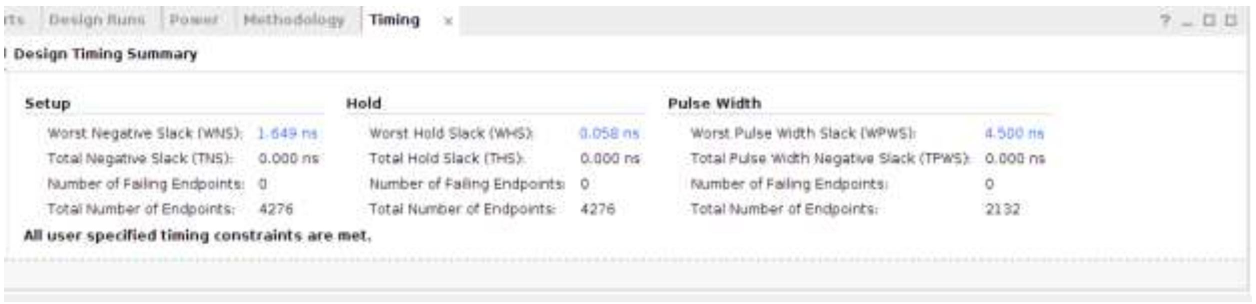


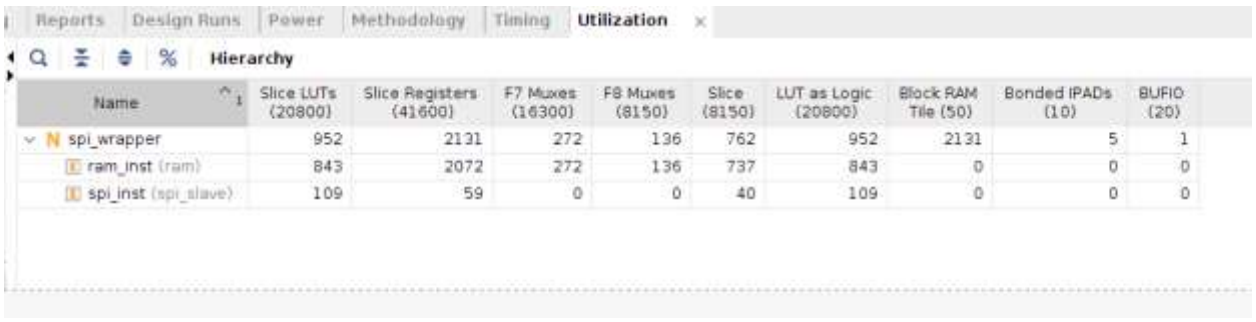
Figure 24 shows the FPGA Device Snippets generated for Gray Encoded SPI



Design Timing Summary

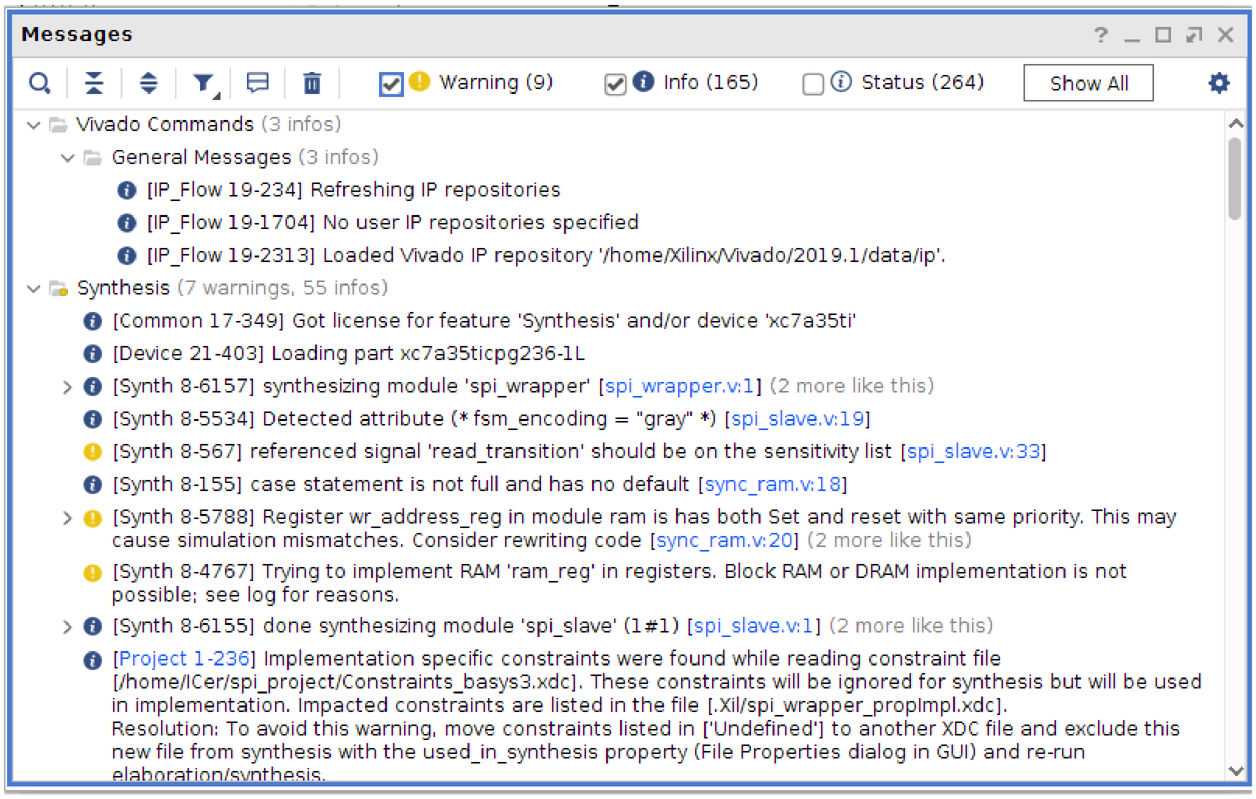
```
Setup                                        Hold                                      Pulse Width
  Worst Negative Slack (WNS):       1.649 ns   Worst Hold Slack (WHS):          0.058 ns   Worst Pulse Width Slack (WPWS):          4.500 ns
  Total Negative Slack (TNS):       0.000 ns   Total Hold Slack (THS):          0.000 ns   Total Pulse Width Negative Slack (TPWS): 0.000 ns
  Number of Failing Endpoints:      0          Number of Failing Endpoints:     0          Number of Failing Endpoints:             0
  Total Number of Endpoints:        4276       Total Number of Endpoints:       4276       Total Number of Endpoints:               2132
All user specified timing constraints are met.
```

Figure 25 shows the Timing Report after implementation of the gray encoded SPI



Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	Block RAM Tile (50)	Bonded IPADs (10)	BUFIO (20)
spi_wrapper	952	2131	272	136	762	952	2131	5	1
ram_inst (ram)	843	2072	272	136	737	843	0	0	0
spi_inst (spi_slave)	109	59	0	0	40	109	0	0	0

Figure 26 shows the Utilization Report after implementation of the gray encoded SPI



```
Vivado Commands (3 infos)
  General Messages (3 infos)
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository '/home/Xilinx/Vivado/2019.1/data/ip'.
Synthesis (7 warnings, 55 infos)
  [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
  [Device 21-403] Loading part xc7a35ticpg236-1L
  [Synth 8-6157] synthesizing module 'spi_wrapper' [spi_wrapper.v:1] (2 more like this)
  [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [spi_slave.v:19]
  [Synth 8-567] referenced signal 'read_transition' should be on the sensitivity list [spi_slave.v:33]
  [Synth 8-155] case statement is not full and has no default [sync_ram.v:18]
  [Synth 8-5788] Register wr_address_reg in module ram is has both Set and reset with same priority. This may
  cause simulation mismatches. Consider rewriting code [sync_ram.v:20] (2 more like this)
  [Synth 8-4767] Trying to implement RAM 'ram_reg' in registers. Block RAM or DRAM implementation is not
  possible; see log for reasons.
  [Synth 8-6155] done synthesizing module 'spi_slave' (1#1) [spi_slave.v:1] (2 more like this)
  [Project 1-236] Implementation specific constraints were found while reading constraint file
  [/home/ICer/spi_project/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used
  in implementation. Impacted constraints are listed in the file [.Xil/spi_wrapper_propImpl.xdc].
  Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this
  new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run
  elaboration/synthesis.
```

Figure 27 shows the Messages Tab with NO Errors after implementation of the gray encoded SPI

b. One-hot Encoding: Lowest worst Negative Slack

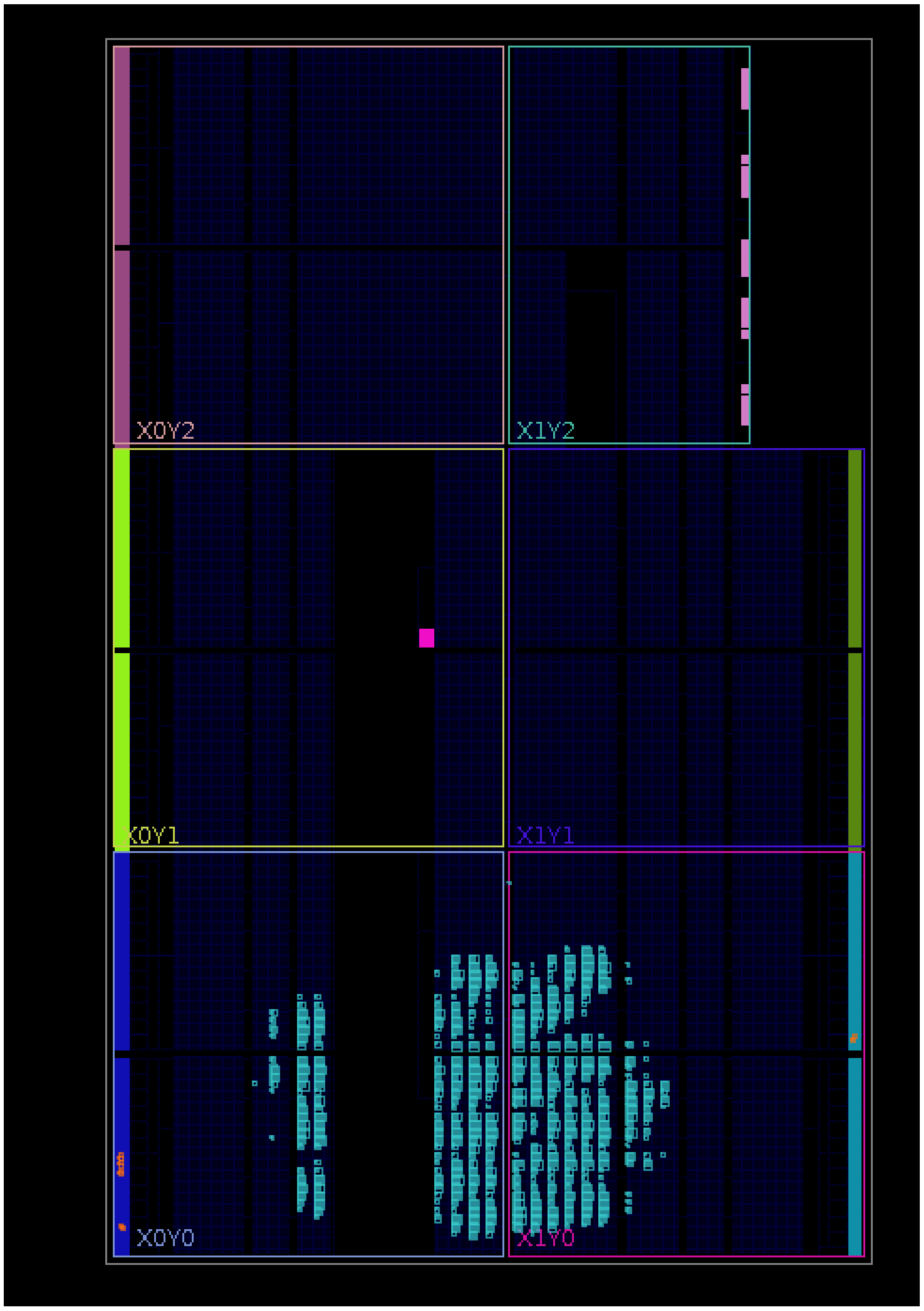
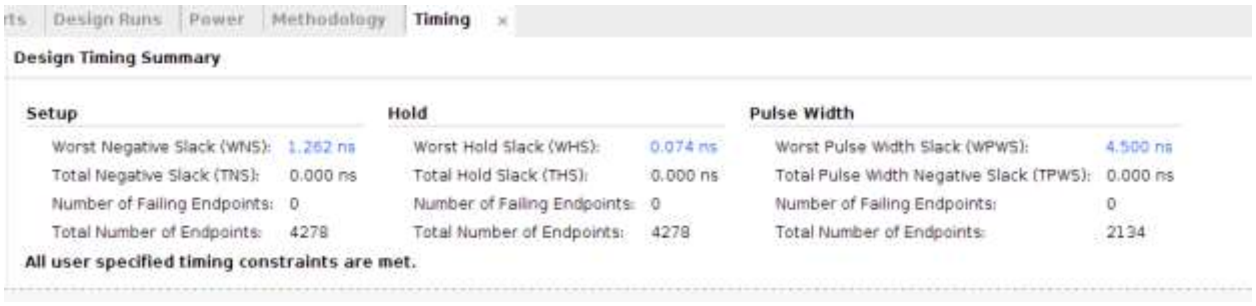


Figure 28 shows the FPGA Device Snippets of the one-hot encoded SPI

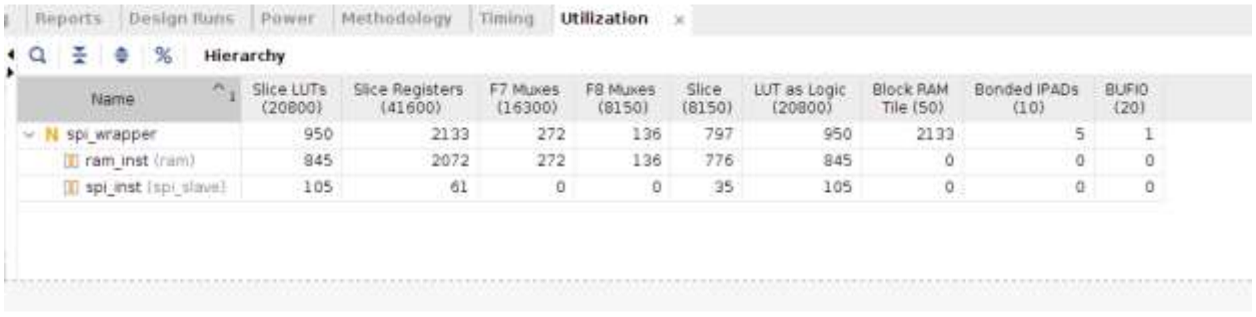


Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	1.262 ns	Worst Hold Slack (WHS):	0.074 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4278	Total Number of Endpoints:	4278	Total Number of Endpoints:	2134

All user specified timing constraints are met.

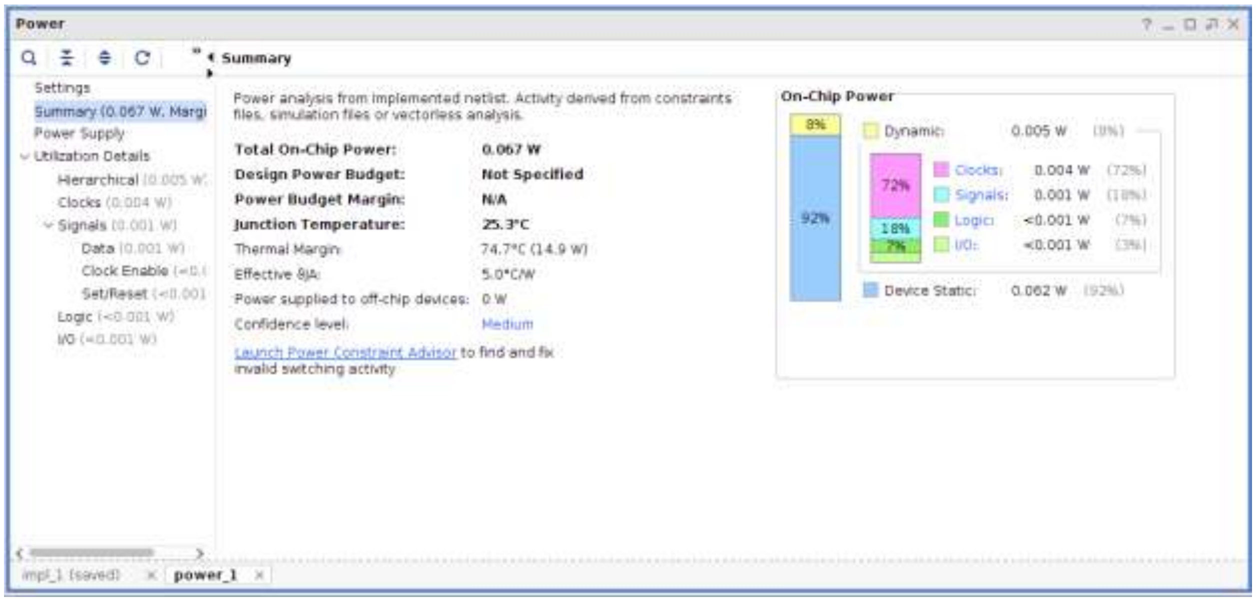
Figure 29 shows the Timing Report after implementation of the one-hot encoded SPI



Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	Block RAM Tile (50)	Bonded IPADs (10)	BUFIO (20)
spi_wrapper	950	2133	272	136	797	950	2133	5	1
ram_inst (ram)	845	2072	272	136	776	845	0	0	0
spi_inst (spi_slave)	105	61	0	0	35	105	0	0	0

Figure 30 shows the Utilization Report after implementation of the one-hot encoded SPI



Power

Summary

Power analysis from implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

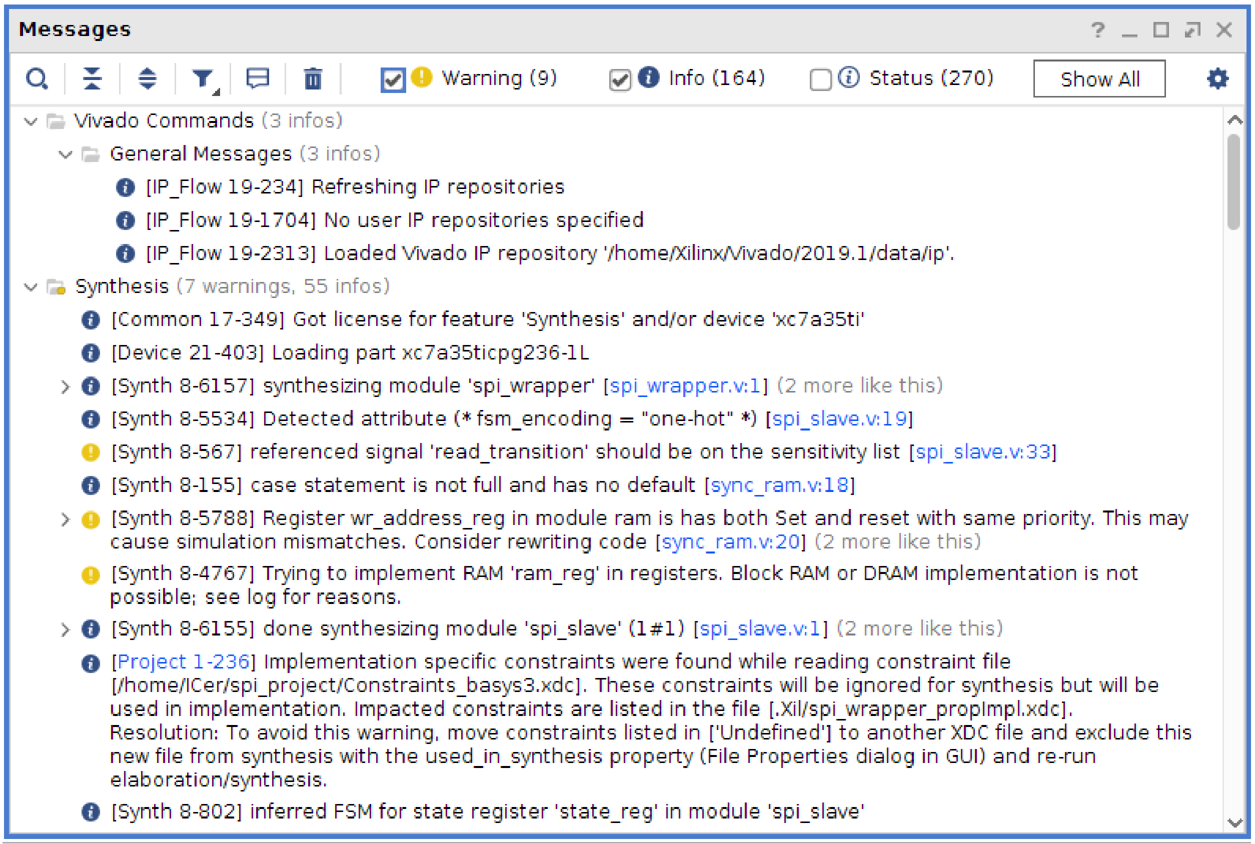
Total On-Chip Power:	**0.067 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.3°C**
Thermal Margin:	74.7°C (14.9 W)
Effective ϑJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	0.005 W	(8%)
Clocks:	0.004 W	(72%)
Signals:	0.001 W	(18%)
Logic:	<0.001 W	(7%)
I/O:	<0.001 W	(3%)
Device Static:	0.062 W	(92%)

Figure 31 shows the Power Report after implementation of the one-hot encoded SPI



Messages

Warning (9) Info (164) Status (270) Show All

```
Vivado Commands (3 infos)
  General Messages (3 infos)
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository '/home/Xilinx/Vivado/2019.1/data/ip'.
Synthesis (7 warnings, 55 infos)
  [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
  [Device 21-403] Loading part xc7a35ticpg236-1L
  [Synth 8-6157] synthesizing module 'spi_wrapper' [spi_wrapper.v:1] (2 more like this)
  [Synth 8-5534] Detected attribute (* fsm_encoding = "one-hot" *) [spi_slave.v:19]
  [Synth 8-567] referenced signal 'read_transition' should be on the sensitivity list [spi_slave.v:33]
  [Synth 8-155] case statement is not full and has no default [sync_ram.v:18]
  [Synth 8-5788] Register wr_address_reg in module ram is has both Set and reset with same priority. This may
  cause simulation mismatches. Consider rewriting code [sync_ram.v:20] (2 more like this)
  [Synth 8-4767] Trying to implement RAM 'ram_reg' in registers. Block RAM or DRAM implementation is not
  possible; see log for reasons.
  [Synth 8-6155] done synthesizing module 'spi_slave' (1#1) [spi_slave.v:1] (2 more like this)
  [Project 1-236] Implementation specific constraints were found while reading constraint file
  [/home/ICer/spi_project/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be
  used in implementation. Impacted constraints are listed in the file [.Xil/spi_wrapper_propImpl.xdc].
  Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this
  new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run
  elaboration/synthesis.
  [Synth 8-802] inferred FSM for state register 'state_reg' in module 'spi_slave'
```

Figure 32 shows the Messages Tab with NO Errors after implementation of the one-hot encoded SPI

c. Sequential Encoding: Highest Worst Negative Slack

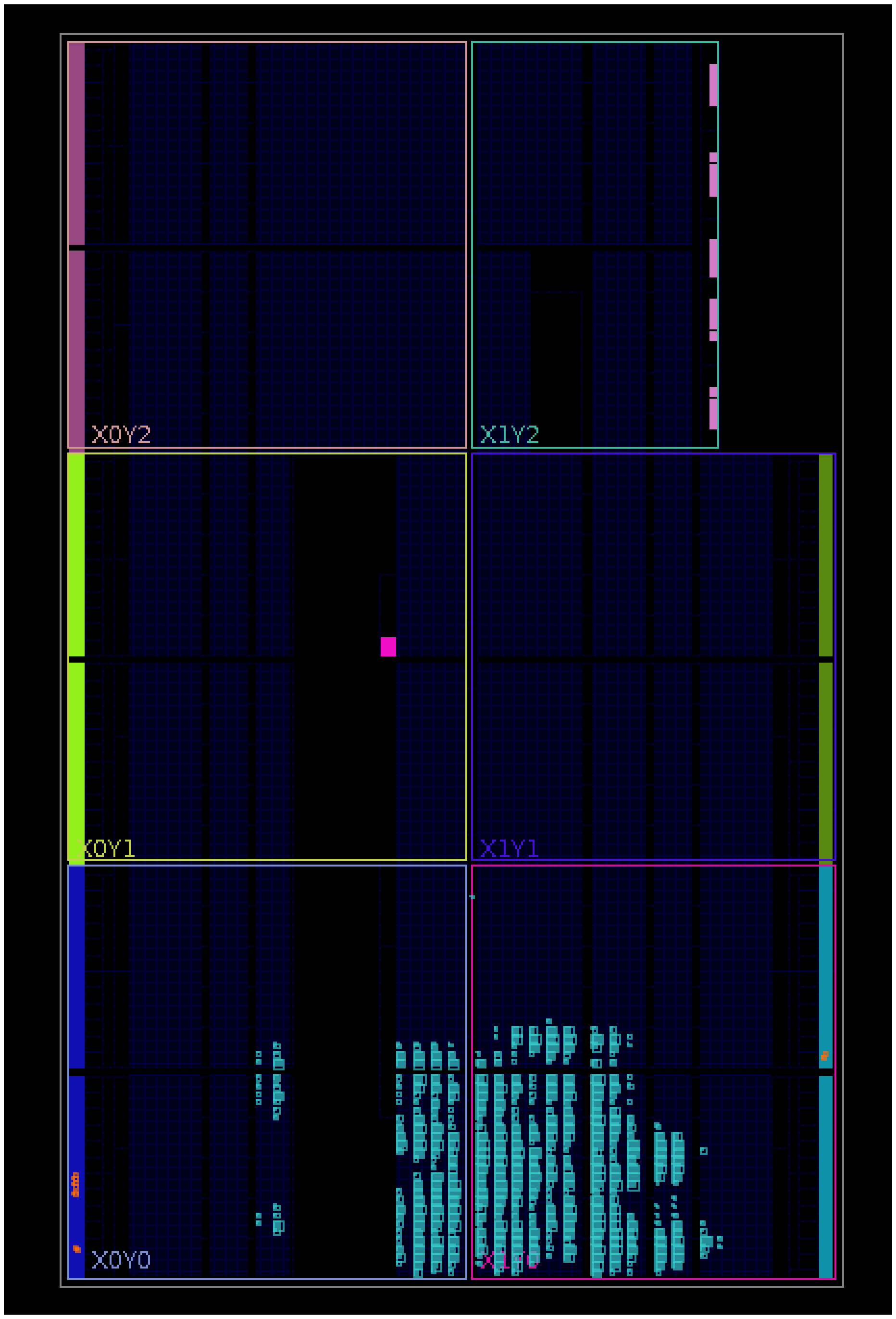
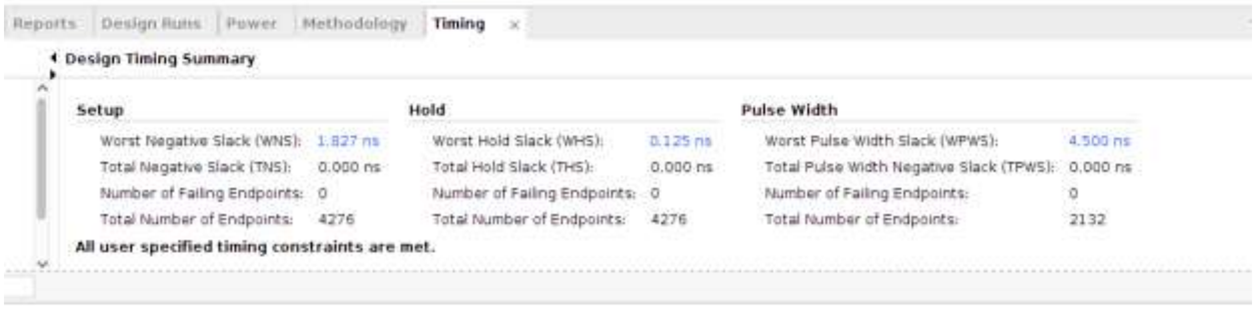


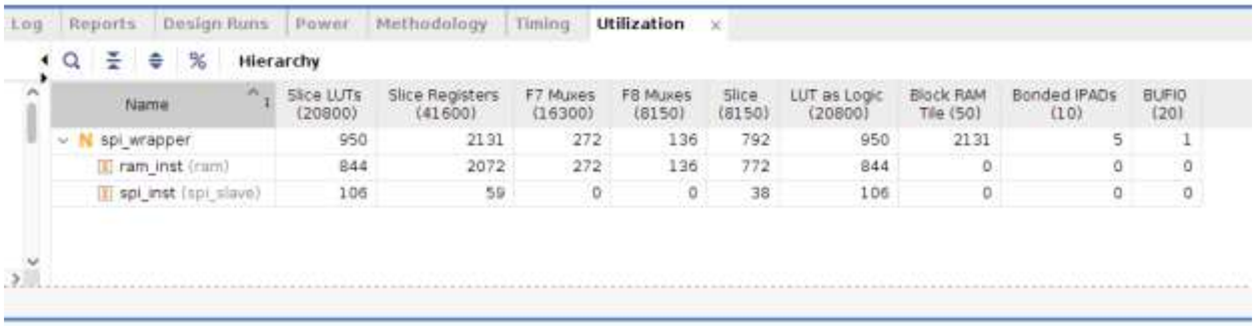
Figure 33 shows the FPGA Device Snippets generated for Sequential Encoded SPI



Design Timing Summary

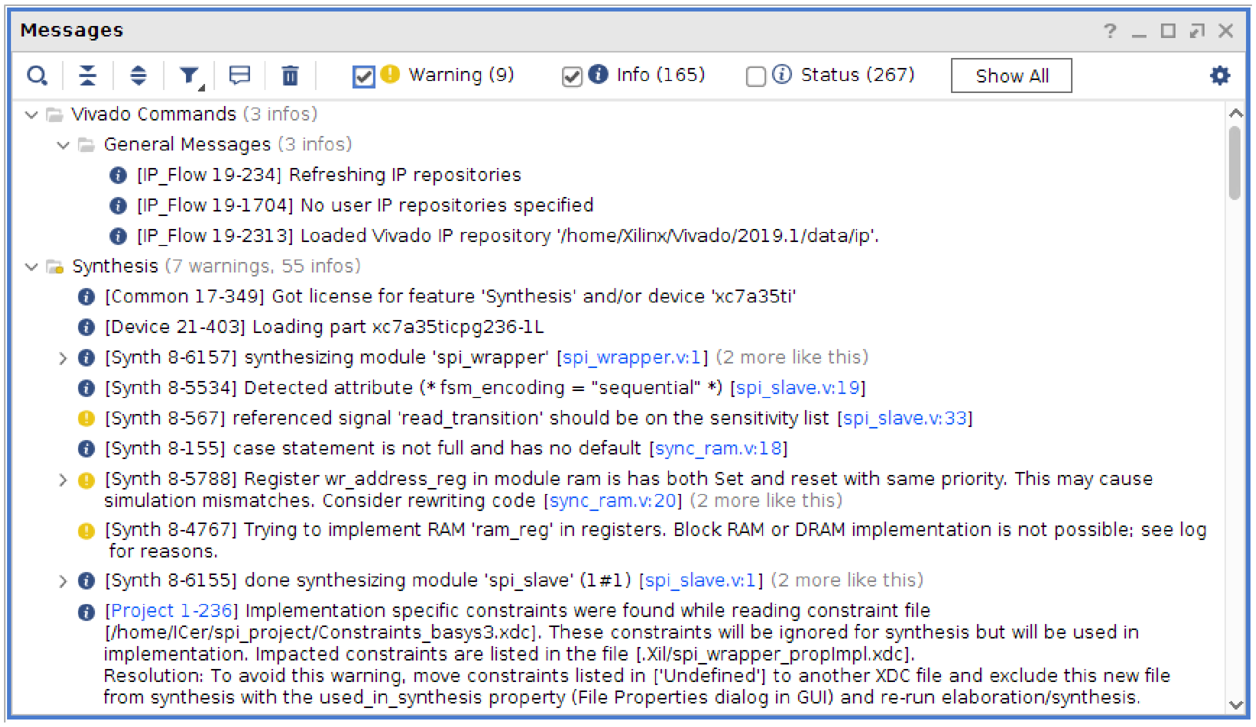
```
Setup                                        Hold                                        Pulse Width
Worst Negative Slack (WNS):      1.827 ns    Worst Hold Slack (WHS):         0.125 ns    Worst Pulse Width Slack (WPWS):            4.500 ns
Total Negative Slack (TNS):      0.000 ns    Total Hold Slack (THS):         0.000 ns    Total Pulse Width Negative Slack (TPWS):   0.000 ns
Number of Failing Endpoints:     0           Number of Failing Endpoints:    0           Number of Failing Endpoints:               0
Total Number of Endpoints:       4276        Total Number of Endpoints:      4276        Total Number of Endpoints:                 2132
All user specified timing constraints are met.
```

Figure 34 shows the Timing Report after implementation of the sequential encoded SPI



Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	Block RAM Tile (50)	Bonded IPADs (10)	BUFIO (20)
spi_wrapper	950	2131	272	136	792	950	2131	5	1
ram_inst (ram)	844	2072	272	136	772	844	0	0	0
spi_inst (spi_slave)	106	59	0	0	38	106	0	0	0

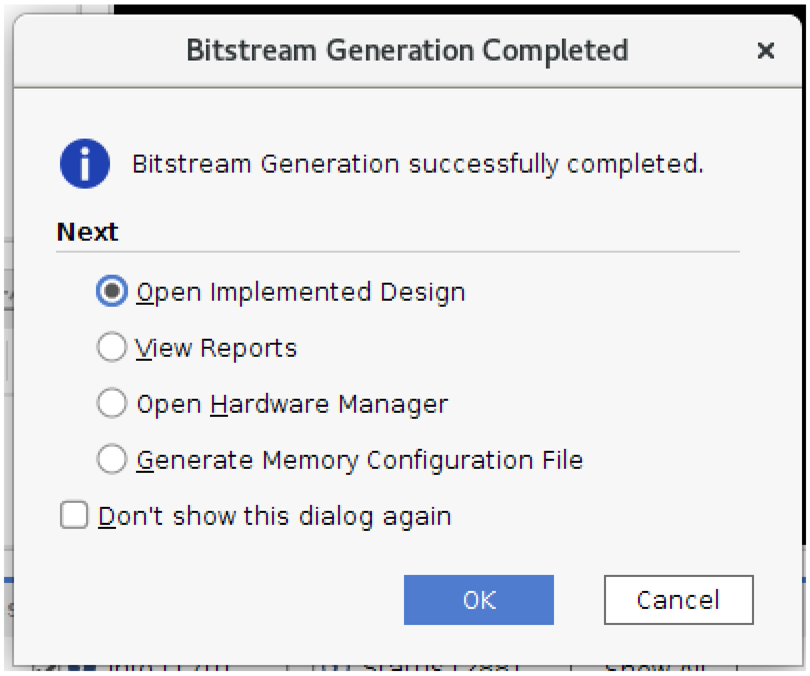
Figure 35 shows the Utilization Report after implementation of the sequential encoded SPI



```
Vivado Commands (3 infos)
  General Messages (3 infos)
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository '/home/Xilinx/Vivado/2019.1/data/ip'.
Synthesis (7 warnings, 55 infos)
  [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
  [Device 21-403] Loading part xc7a35ticpg236-1L
  [Synth 8-6157] synthesizing module 'spi_wrapper' [spi_wrapper.v:1] (2 more like this)
  [Synth 8-5534] Detected attribute (* fsm_encoding = "sequential" *) [spi_slave.v:19]
  [Synth 8-567] referenced signal 'read_transition' should be on the sensitivity list [spi_slave.v:33]
  [Synth 8-155] case statement is not full and has no default [sync_ram.v:18]
  [Synth 8-5788] Register wr_address_reg in module ram is has both Set and reset with same priority. This may cause
  simulation mismatches. Consider rewriting code [sync_ram.v:20] (2 more like this)
  [Synth 8-4767] Trying to implement RAM 'ram_reg' in registers. Block RAM or DRAM implementation is not possible; see log
   for reasons.
  [Synth 8-6155] done synthesizing module 'spi_slave' (1#1) [spi_slave.v:1] (2 more like this)
  [Project 1-236] Implementation specific constraints were found while reading constraint file
  [/home/ICer/spi_project/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in
  implementation. Impacted constraints are listed in the file [.Xil/spi_wrapper_propImpl.xdc].
  Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file
  from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
```

Figure 36 shows the Messages Tab with NO Errors after Implementation of the sequential encoded SPI

7. Bitstream Generation:



Bitstream Generation Completed

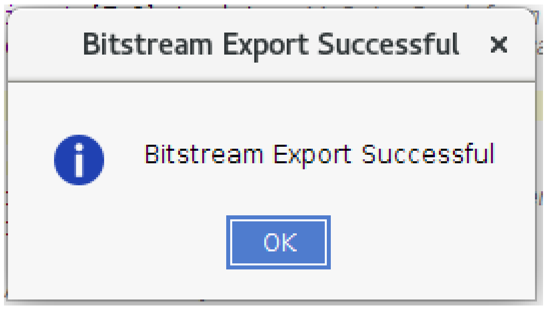
Bitstream Generation successfully completed.

Next

- [✓ Open Implemented Design]
- View Reports
- Open Hardware Manager
- Generate Memory Configuration File

☐ Don't show this dialog again

Figure 38 shows successful generation of bitstream file With No Errors



Bitstream Export Successful

Bitstream Export Successful

Figure 37 shows successful exportation of bitstream file