Assignment 4

Current mode control

Name: Mahmoud Nasser Hanafy

Submitted to Prof. Abdelmomen Mahgoub

$$(G_{vc}(s) = \frac{\widehat{v_o}}{\widehat{v_c}} \approx \frac{R}{R_i} \times \frac{1}{1 + \frac{RT_s}{L} \times \left(m_c\widehat{D} - 0.5\right)} F_p(s)F_h(s))$$

$$(F_p(s) = \frac{1 + sT_sRC}{1 + s/\omega_p}$$

$$\omega_p = \frac{1}{RC} + \frac{T_s}{L} \times \left(m_c\widehat{D} - 0.5\right)) \text{ low freq pole of power stage}$$

$$F_h(s) = \frac{1}{1 + \frac{s}{Q_p\omega_n} + \left(\frac{s}{\omega_n}\right)^2} \quad ; \quad \omega_n = \frac{\pi}{T_s} \quad ; \quad Q_p$$

$$= \frac{1}{\pi\left(m_c\widehat{D} - 0.5\right)} \text{ high freq poles due to sampling}$$

For $Q = 0.64 = Q_p = \frac{1}{\pi(m_c\widehat{D} - 0.5)}$ …. $m_c = 1.108$ *and* $\widehat{D} = 1 - \frac{V_o}{V_g} = 0.9$

$$(m_c = 1 + \frac{S_e}{S_n})$$

$$(S_e = (m_c - 1) \times S_n = 11.6 \times 10^4 \frac{V}{S})$$

$$(S_n = \frac{\widehat{D}V_g}{L} \times R_i = 108 \times 10^4 \frac{V}{S})$$

Current loop gain

$$(T_i(s) = \frac{L}{RT_sm_c\widehat{D}} \times \frac{1 + sRC}{\Delta(s)} \times H_e(s))$$

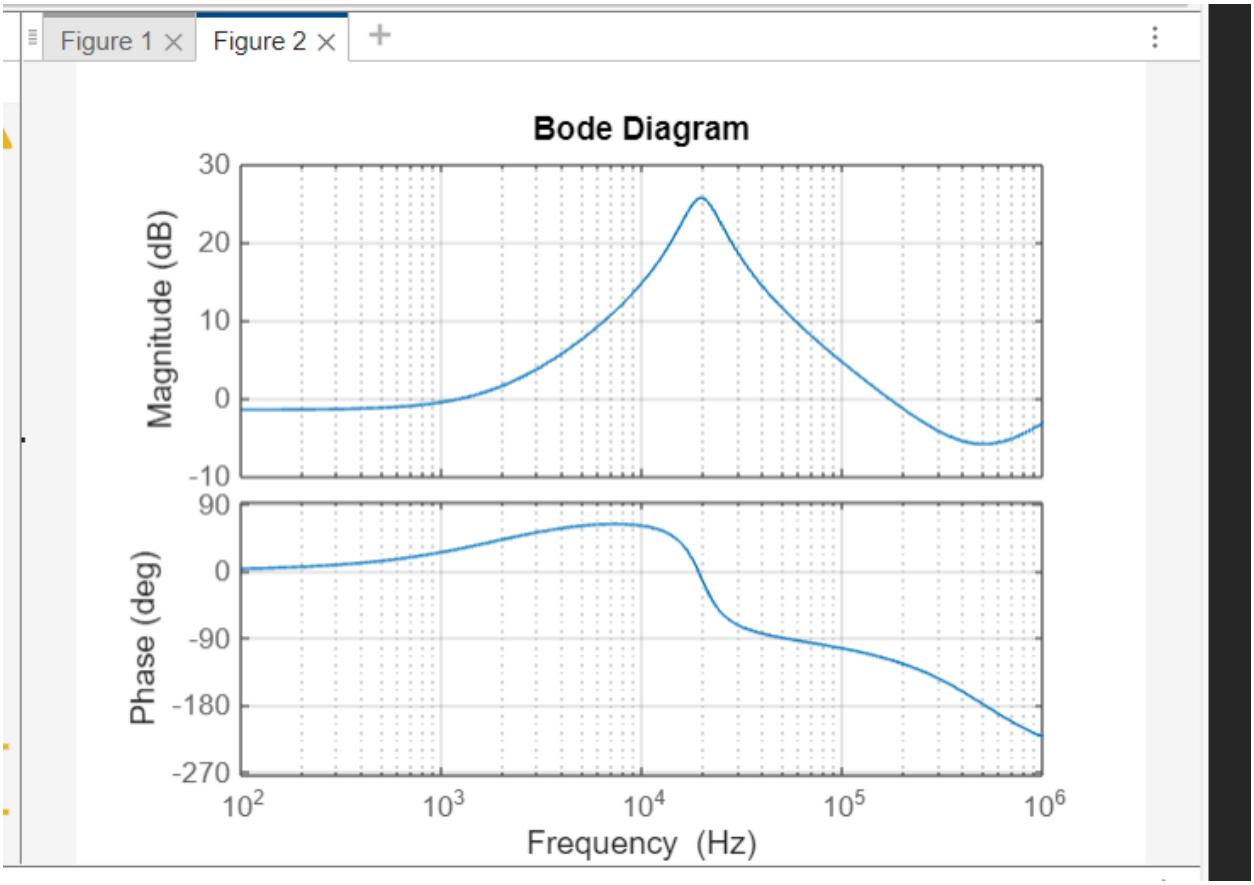
$$(\Delta(s) = 1 + \frac{s}{Q_{ps}\omega_0} + \left(\frac{s}{\omega_0}\right)^2) \text{ characteristic eqn of the open loop system}$$

$$(\omega_0 = \frac{1}{\sqrt{LC}} \sqrt{\frac{1 + \frac{R_L}{R}}{1 + \frac{R_c}{R}}} \approx \frac{1}{\sqrt{LC}})$$

$$(Q_{ps} = \omega_0 \times \frac{1}{(R_c + R \parallel R_L) \times C + \frac{L}{R + R_L}} \approx \frac{1}{\omega_0} \times \frac{1}{R_cC + \frac{L}{R}})$$

$$(H_e(s) = 1 + \frac{s}{Q_z \omega_n} + \left(\frac{s}{\omega_n}\right)^2$$

$$(Q_z = \frac{-2}{\pi})$$



Discussion

Bandwidth of the current loop is 160.7 kHz and Phase margin is 62.2°

Discussion: For wide input and output range applications, for example, Vin=9V-- 15V, Vo=0.8V—1.8V, with other parameters unchanged, how do you choose external ramp such that the stability is guaranteed for the whole operation range?

$$\mathrm{Se} = \frac{\mathrm{V_{gmin}}}{\mathrm{L/R_i}} \times \left(\mathrm{D_{max}} + \frac{1}{\mathrm{Q\pi}} - 0.5\right)$$

$$V_{gmin} = 9\,V$$

$$D_{max} = \frac{V_{o_{max}}}{V_{gmin}}\left(1 + \frac{R_l}{R}\right) = 0.2 \times 1.004 = 0.2008$$

Se to ensure system stability is equal to $17.76 \times 10^4\, V/s$

Q2

2. Design the voltage-loop compensator A(s). Please design the compensator to achieve 50kHz bandwidth for voltage loop gain T_2 (your bandwidth should be within 5kHz window, i.e, 45kHz to 55kHz) while keeping at least 60 degree phase margin and at least 10dB gain margin. *Show your critical design steps* and verify the bode plots of the compensator and loop gain T_2 by simplis simulation. (20%)

$$A(s) = \frac{V_c}{V_o} = -\frac{Z_c}{Z_f}$$

$$A(s) = -\frac{1}{R_1 C_3} \times \frac{(1 + s(R_1 + R_3)C_2)}{s \times (1 + sR_3C_2)}$$

$$A(s) = A_0 \frac{(1 + s/\omega_{za1})}{s \times (1 + s/\omega_{pa1})}$$

$$f_{za1} = \frac{1}{2\pi(R_1 + R_3)C_2}$$

$$f_{pa1} = \frac{1}{2\pi R_3 C_2}$$

$$A_0 = -\frac{1}{R_1 C_3}$$

Design Steps

1. External ramp value is selected to achieve Q=0.64Q=0.64
2. Control to output is measured (fp,$fesr$,fn)

$$f_p = \frac{1}{2\pi} \times \left(\frac{1}{RC} + \frac{T_s}{LC} \times (m_c\overline{D} - 0.5)\right) = 1.199\,\mathrm{KHz}$$

$$f_{esr} = \frac{1}{2\,\pi\,R_{esr}\,C} = 60.29\ \text{KHz}$$

$$f_n = \frac{f_{sw}}{2} = 500\,\text{KHz}$$

Compensator design

$$f_{pa1} = \frac{1}{2\pi R_3 C_2} \quad \text{to cancel ESR zero}$$

$$f_{za1} = \frac{1}{2\pi(R_1 + R_3)C_2} = f_p \quad \text{to cancel dominant low freq pole}$$

Compensator network design

$$\text{Let } C_2 = 2.2\,\text{nF}$$

$$R_3 = R_C C_2 = 1.2\,\text{k}$$

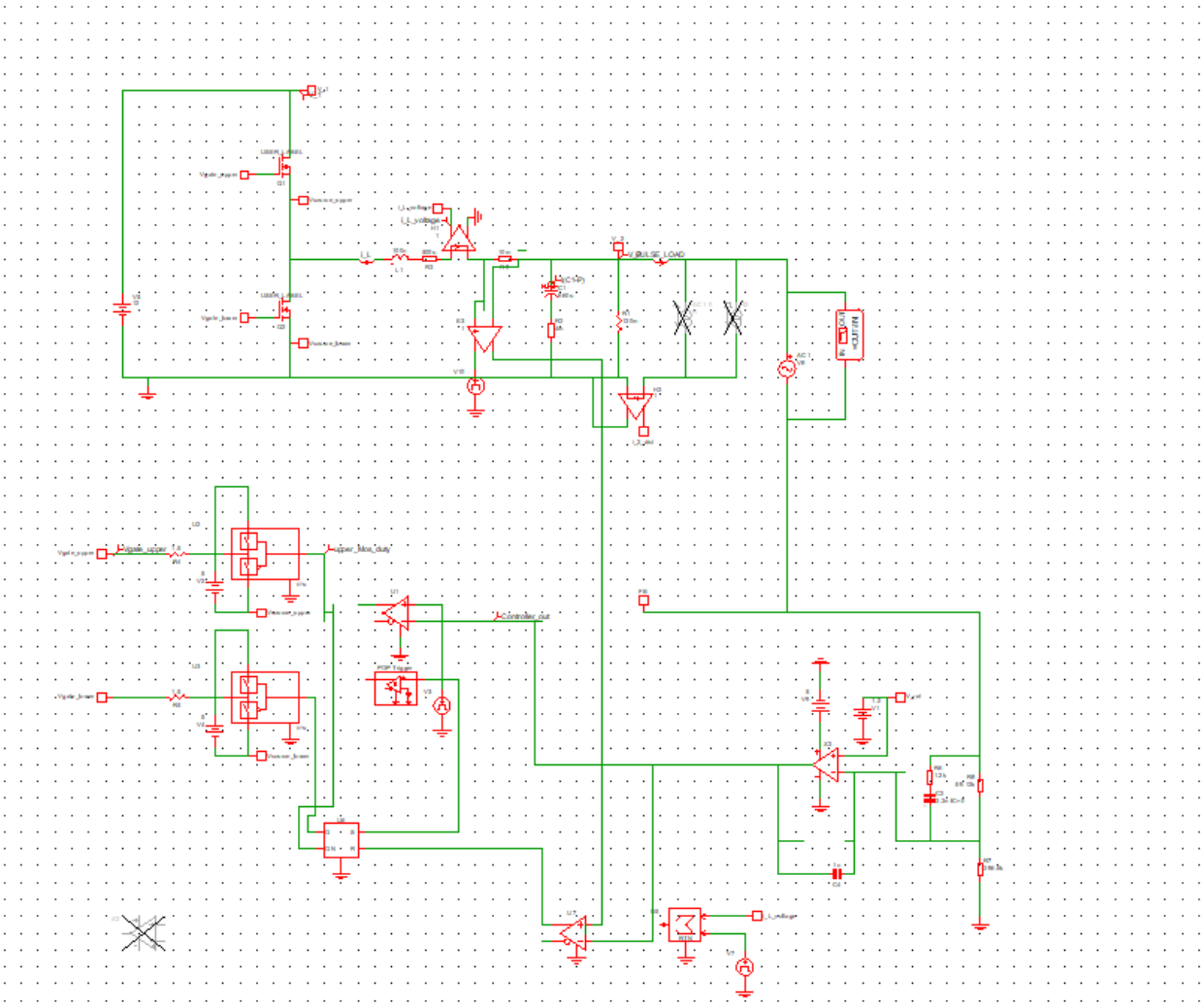
$$R_1 = \frac{1}{\omega_0 C_2} - R_3 = 59.12\,\text{k}$$

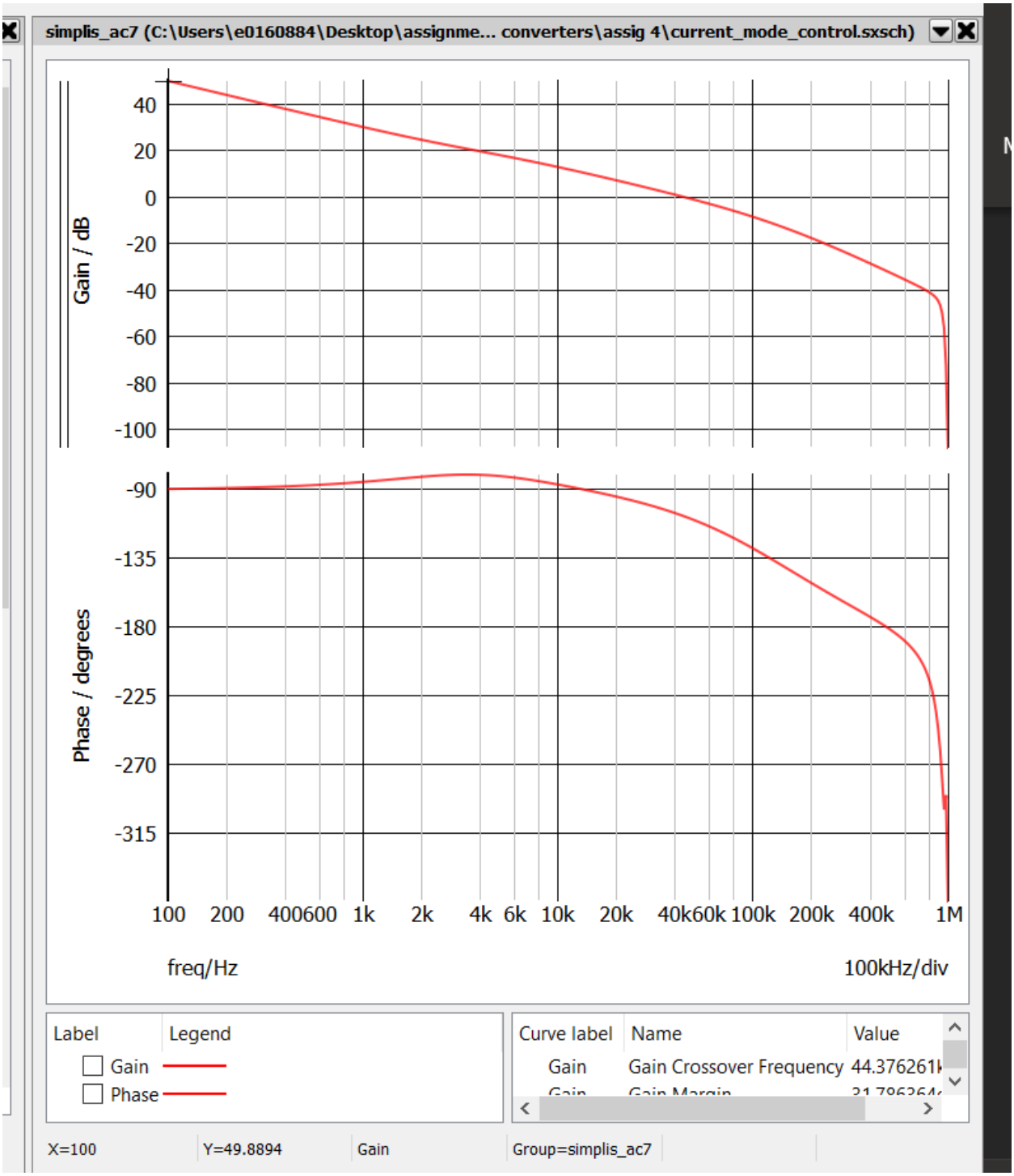
$$R_2 = \frac{R_1 \times V_{ref}}{V_o - V_{ref}} = 295.6\,\text{k}\Omega$$

$$V_{ref} = 1.2$$

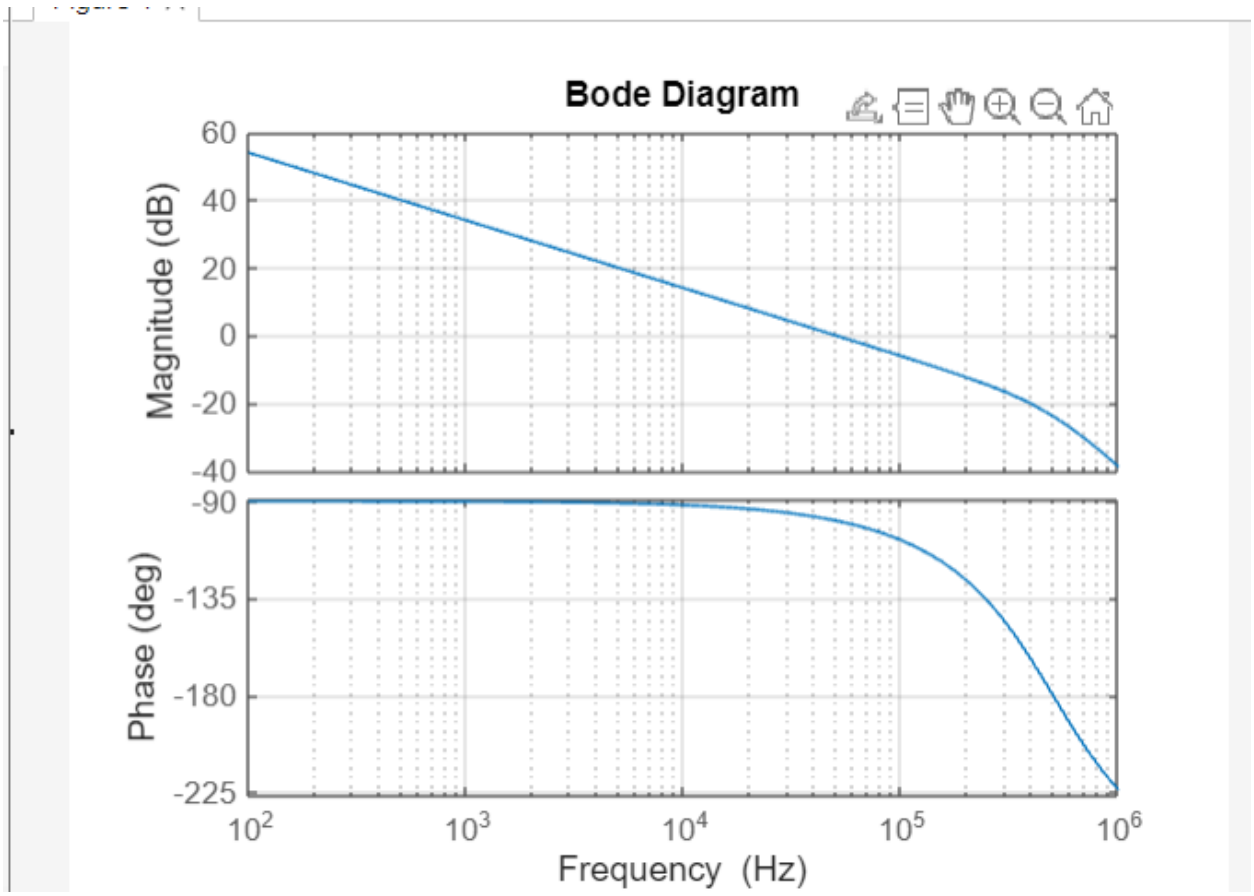
$$C_3 = 1\,\text{nF}$$

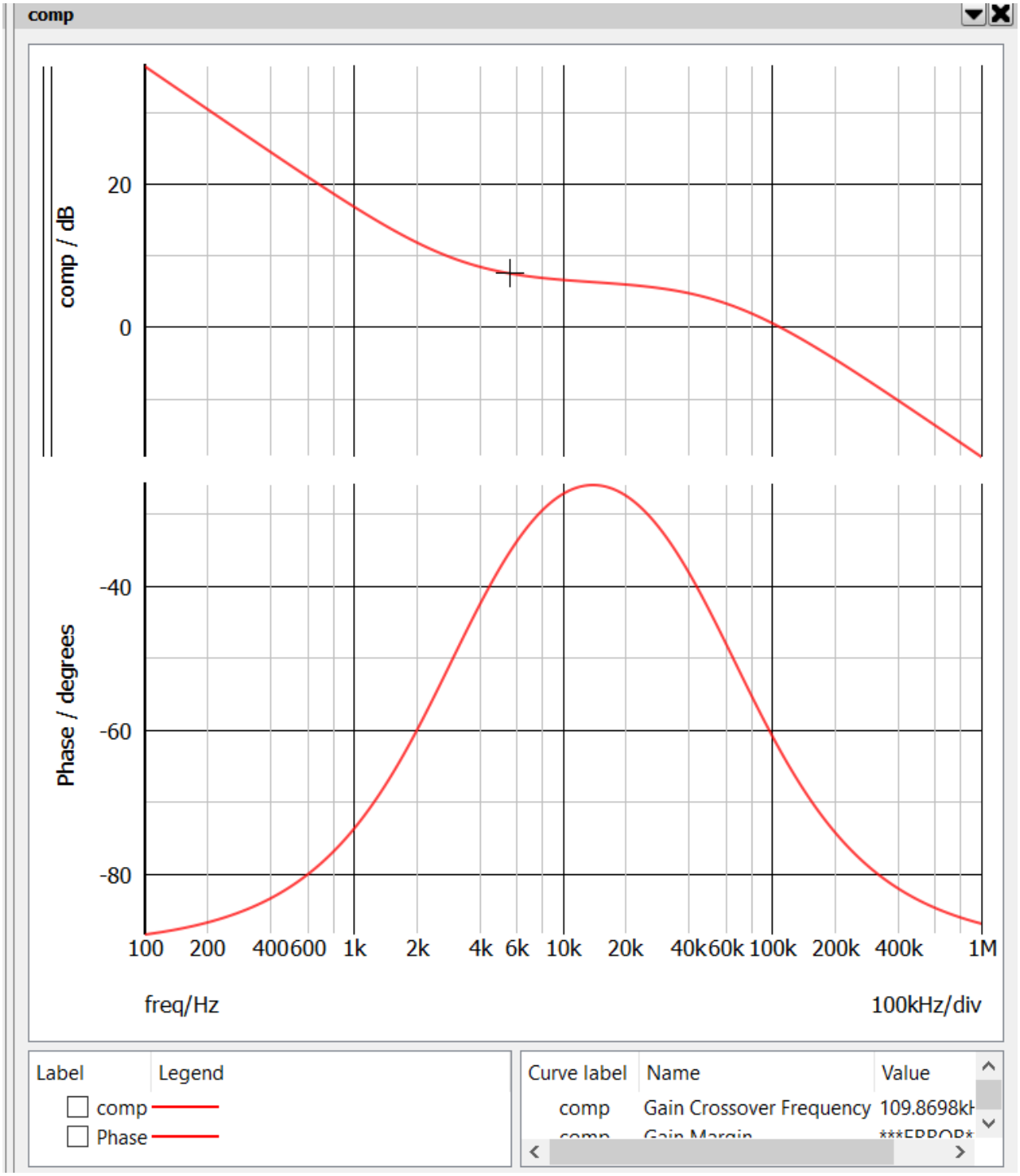
to adjust DC Gain level (50KHz bandwidth)





Loop gain response

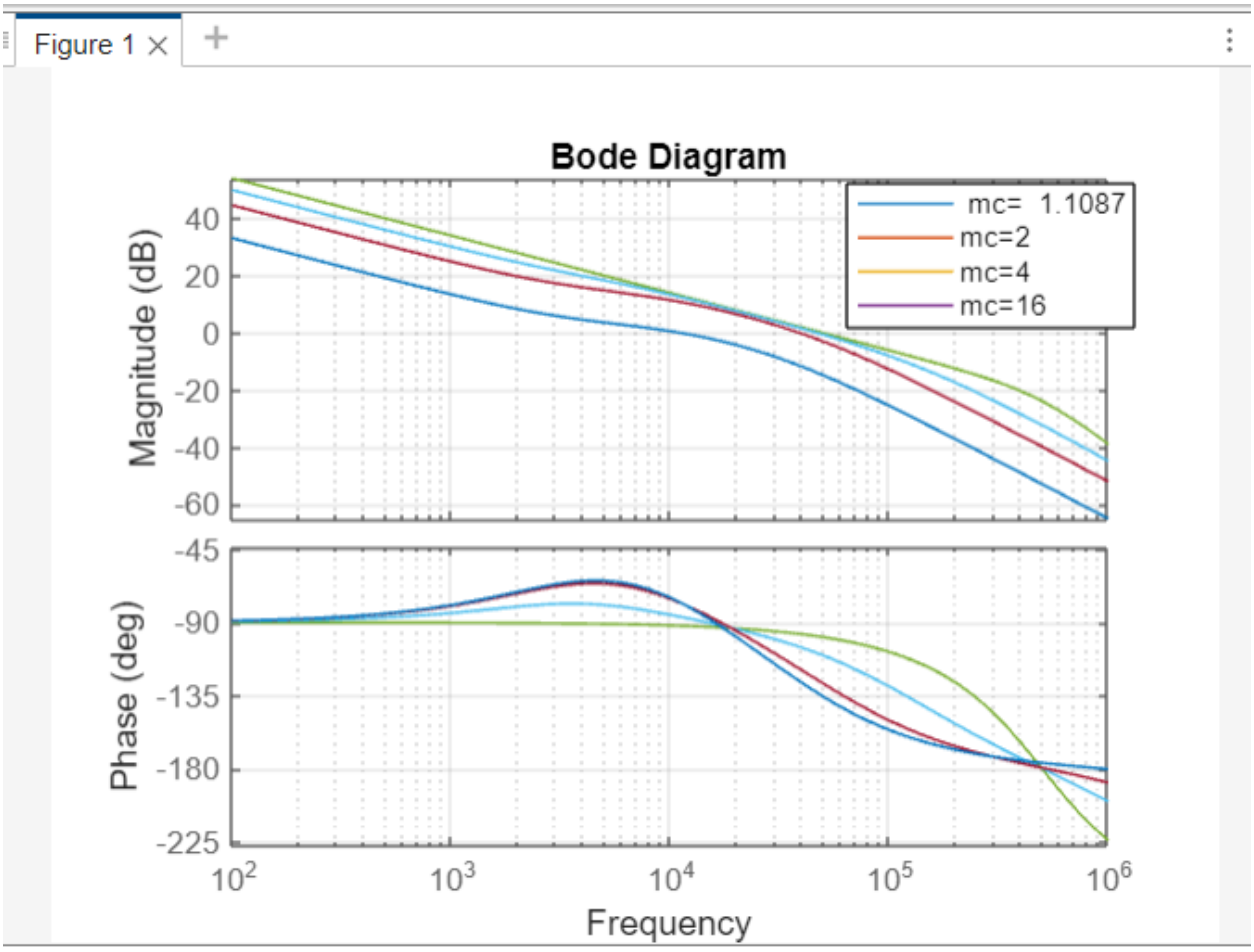

Bode Diagram
Magnitude (dB)
60
40
20
0
-20
-40
Phase (deg)
-90
-135
-180
-225
10^2
10^3
10^4
10^5
10^6
Frequency (Hz)



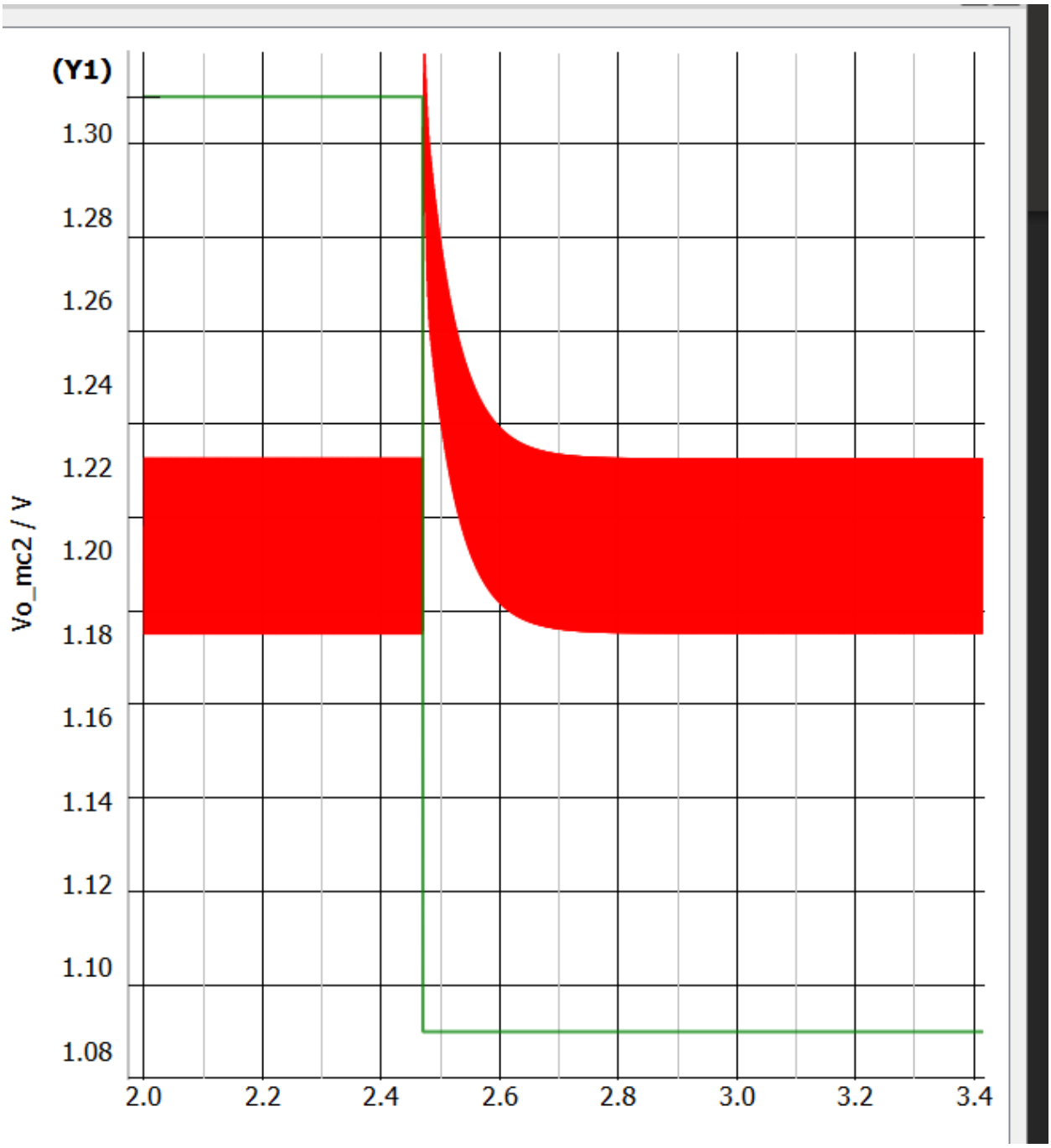
Compensator response

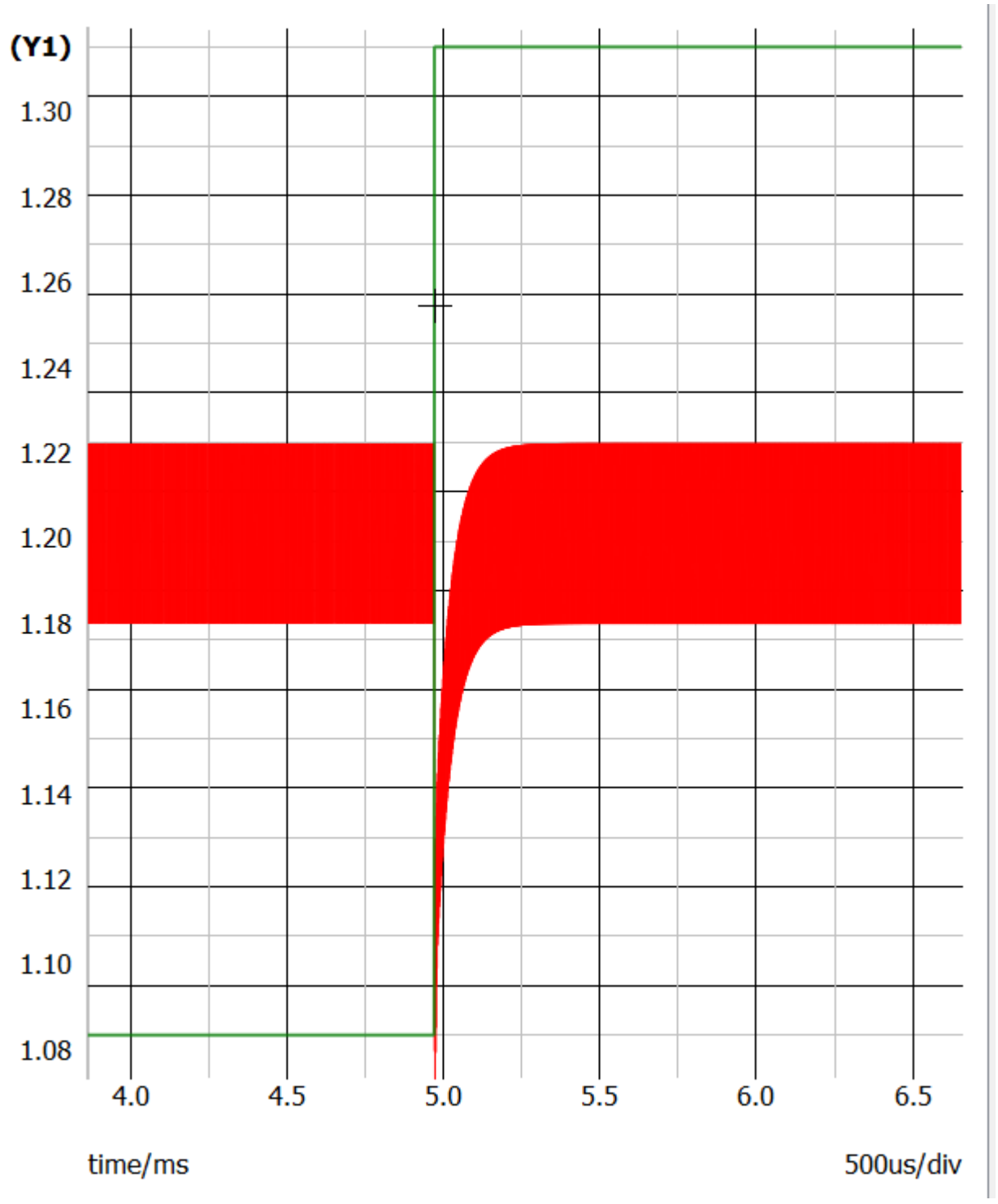
3. Comparison of the loop gain T_2 and load transient responses (with load transient specified previously) impacted by the external ramp S_e and the compensator A(s). (20%)

(3.1) With all the other parameters the same as your solution for question 2, Change S_e so that $m_c=(1+s_e/s_n)$ equals 2, 4, 16 respectively. Compare the loop gain T_2 and load transient response for the three cases and *comment the results.*

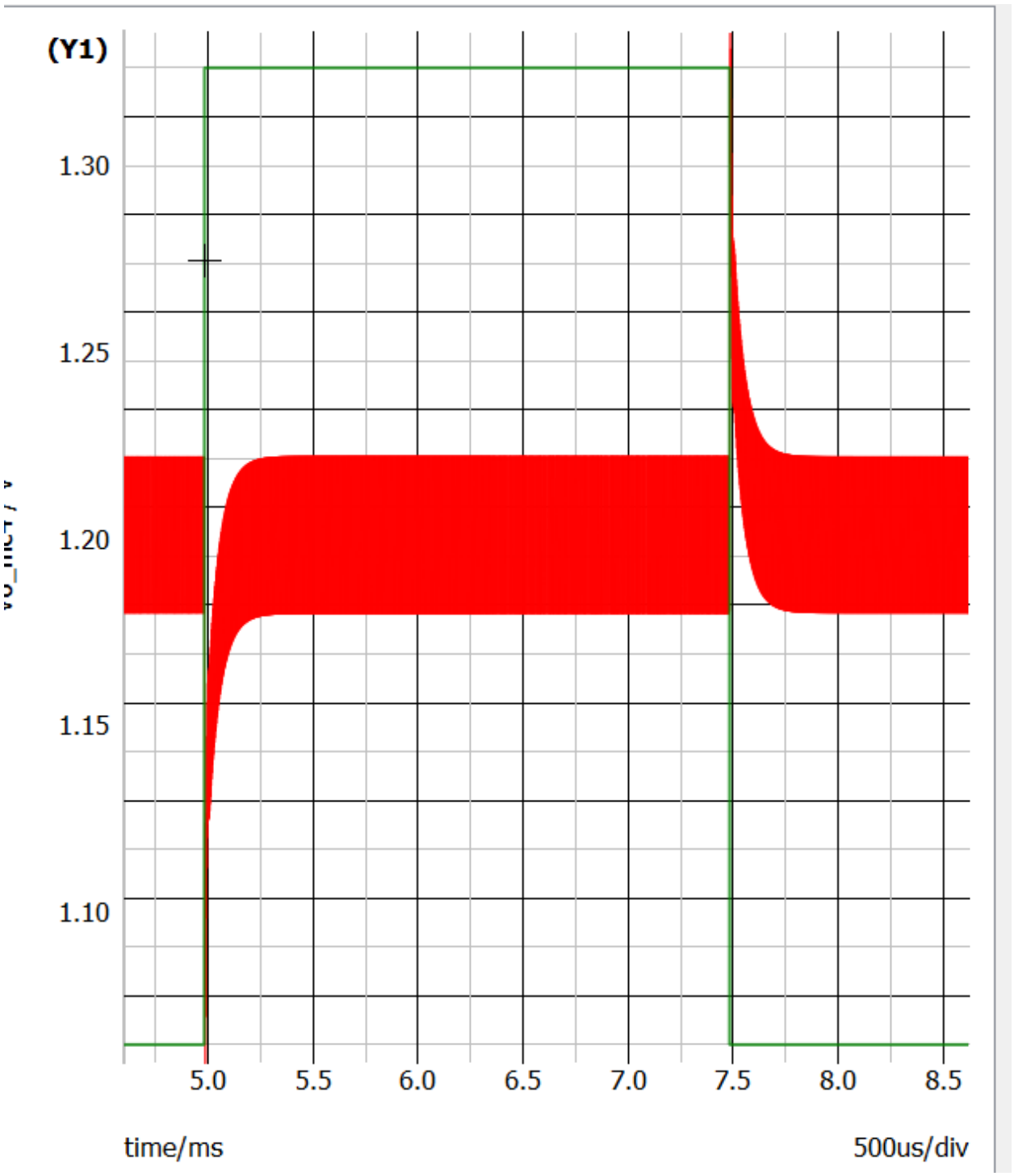


$$mc = 2$$

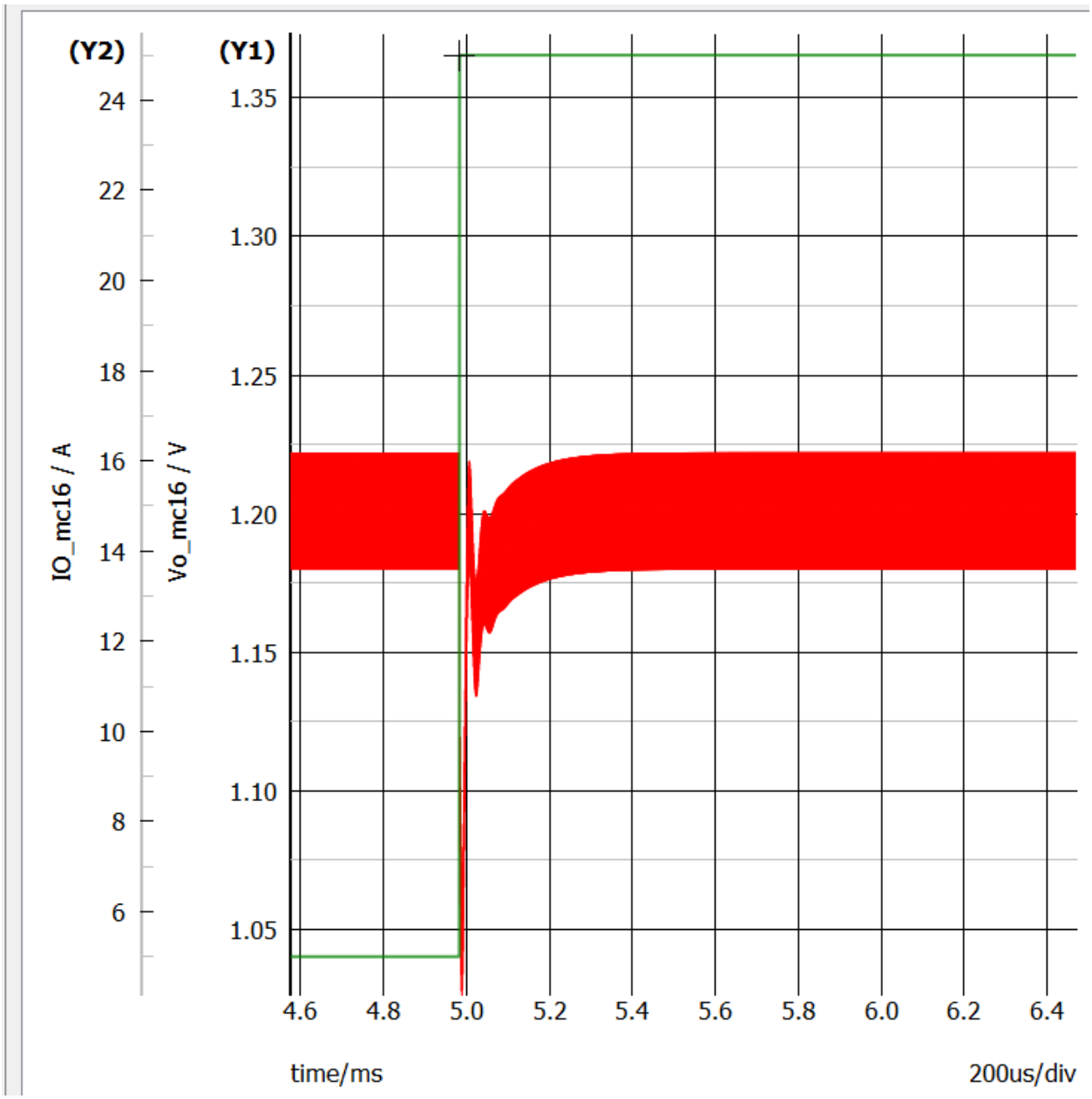

(Y1)
1.30
1.28
1.26
1.24
1.22
1.20
1.18
1.16
1.14
1.12
1.10
1.08
Vo_mc2 / V
2.0
2.2
2.4
2.6
2.8
3.0
3.2
3.4

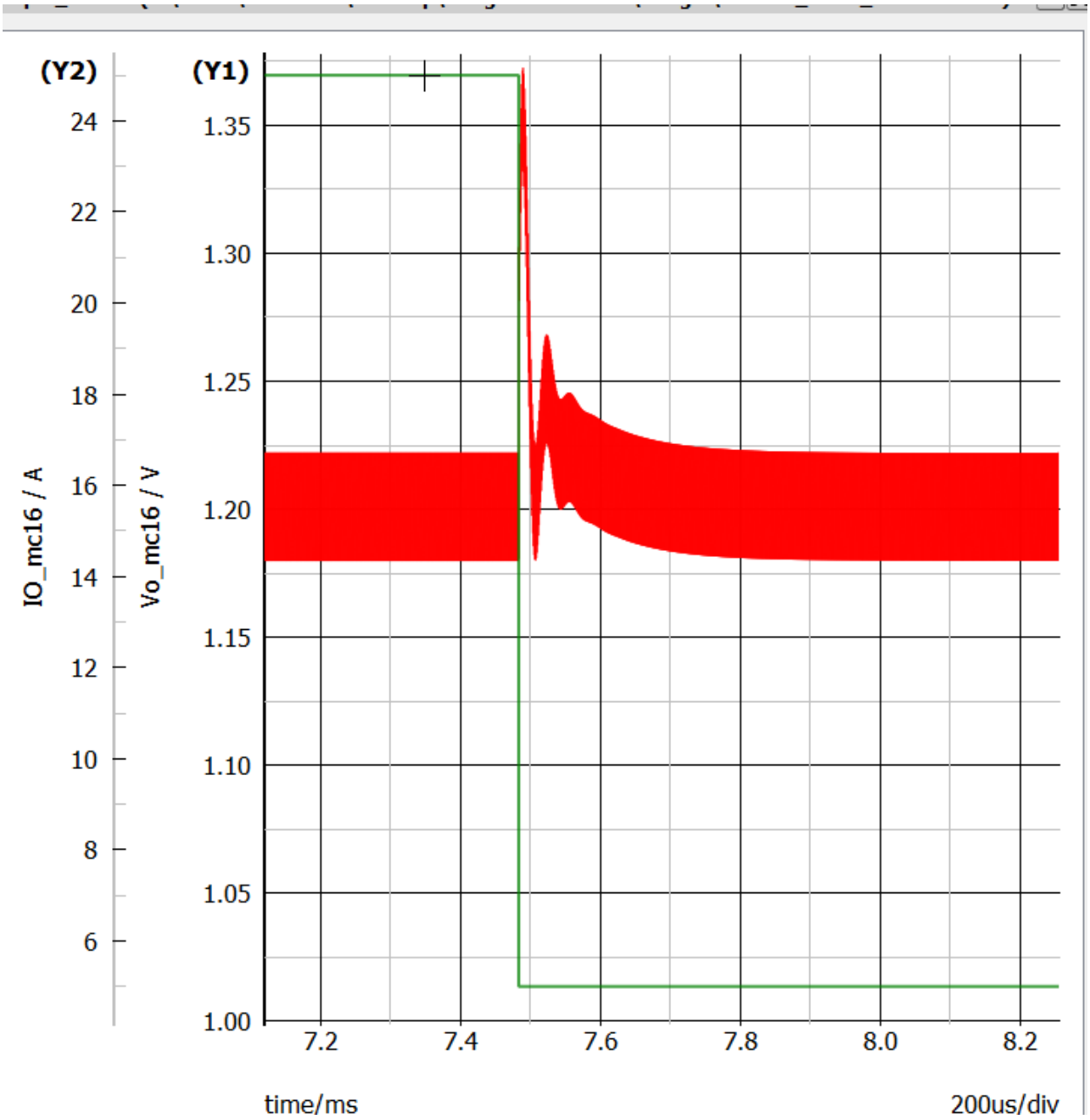

(Y1)
1.30
1.28
1.26
1.24
1.22
1.20
1.18
1.16
1.14
1.12
1.10
1.08
4.0
4.5
5.0
5.5
6.0
6.5
time/ms
500us/div

mc = 4



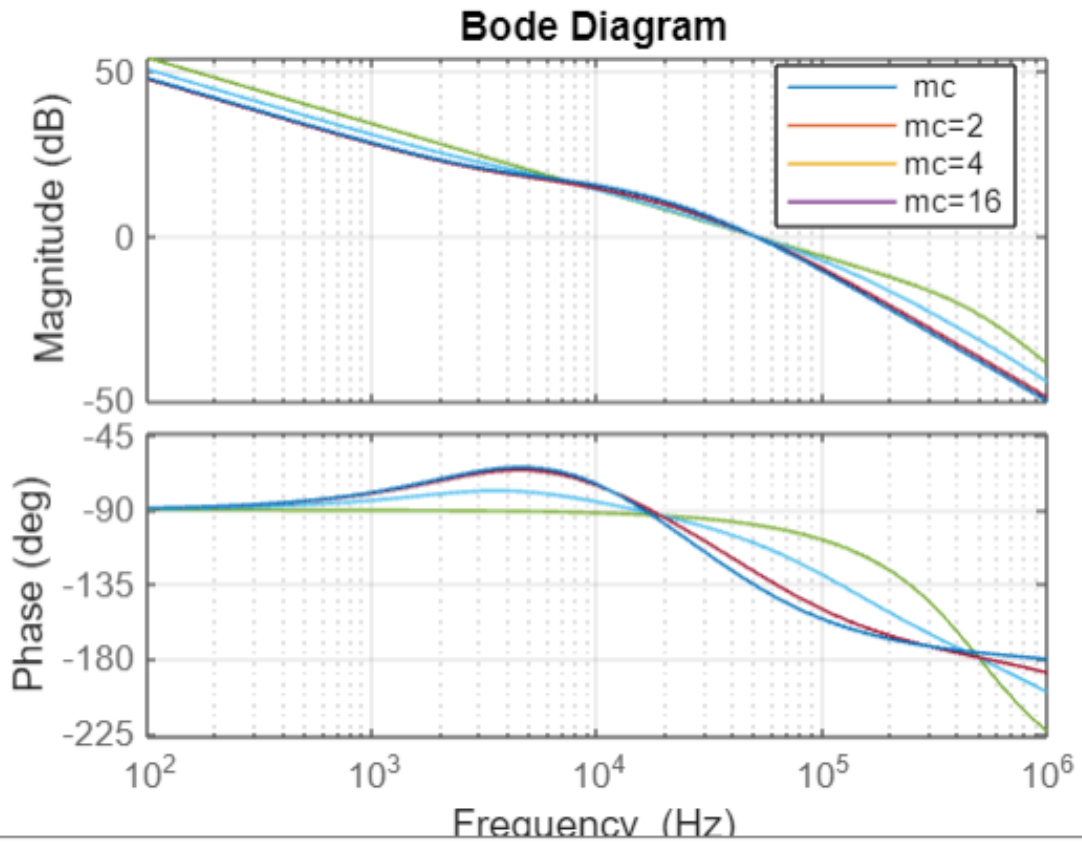
Mc = 16

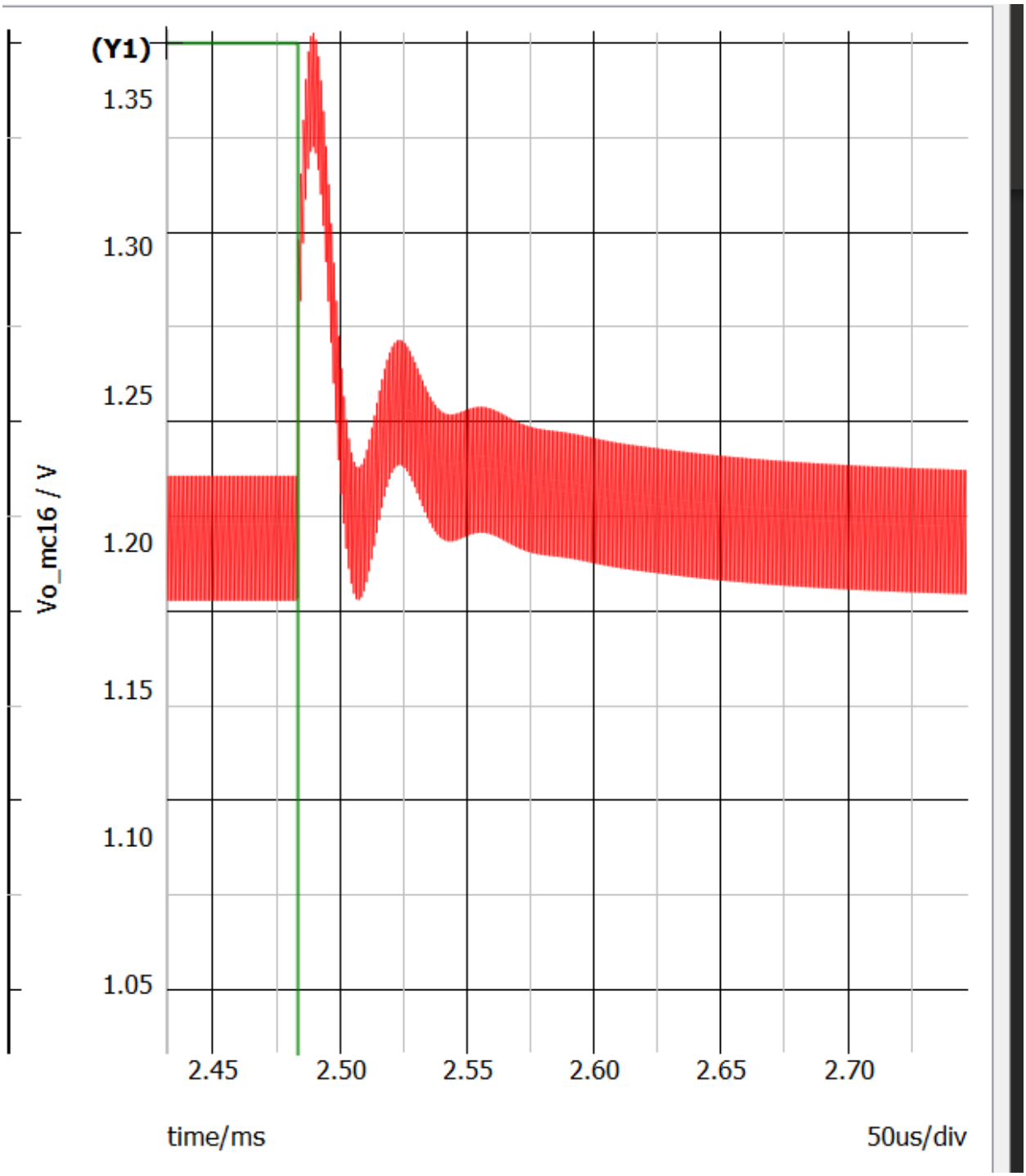

(Y2)
(Y1)
24
22
20
18
16
14
12
10
8
6
1.35
1.30
1.25
1.20
1.15
1.10
1.05
IO_mc16 / A
Vo_mc16 / V
4.6
4.8
5.0
5.2
5.4
5.6
5.8
6.0
6.2
6.4
time/ms
200us/div

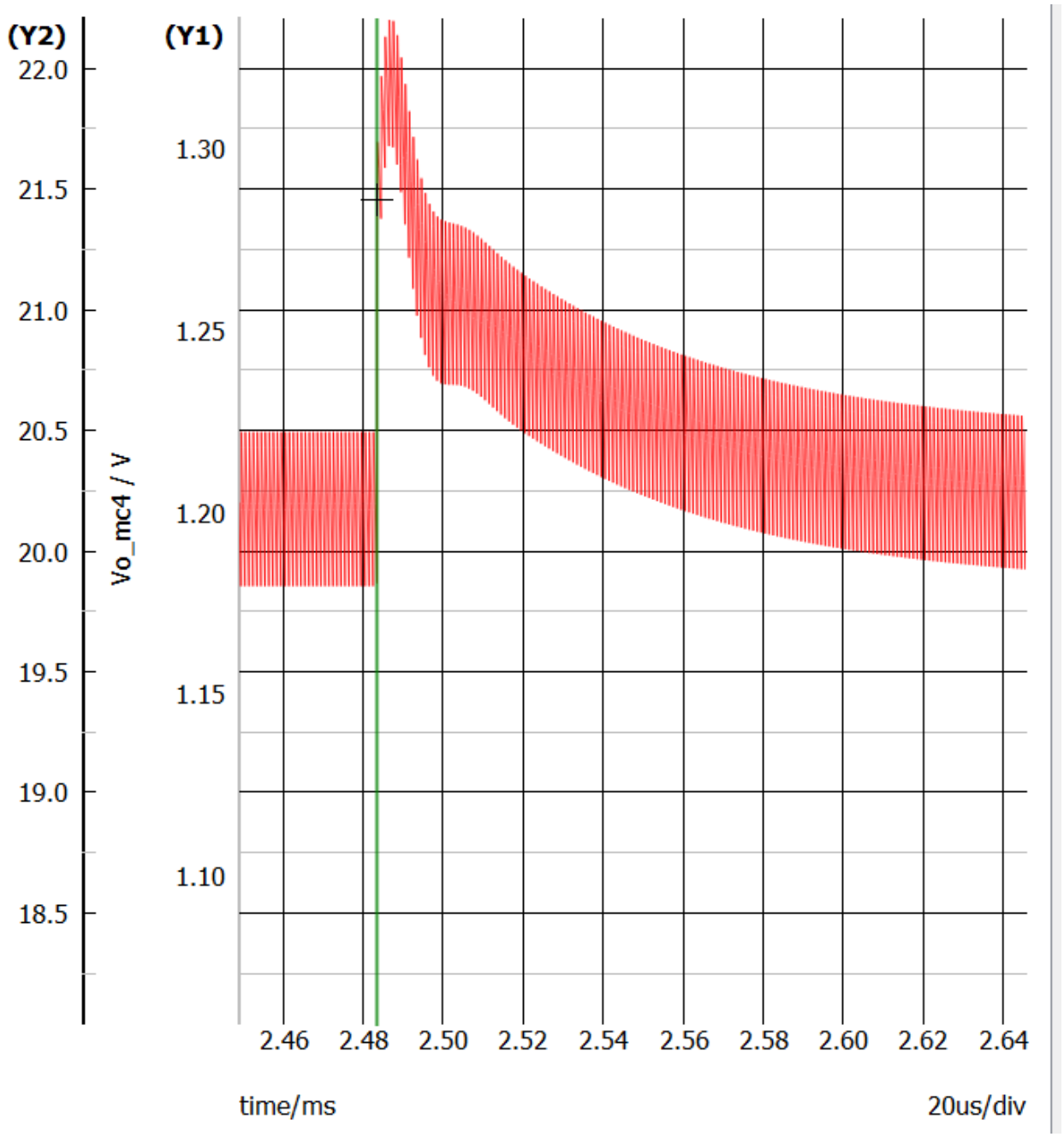


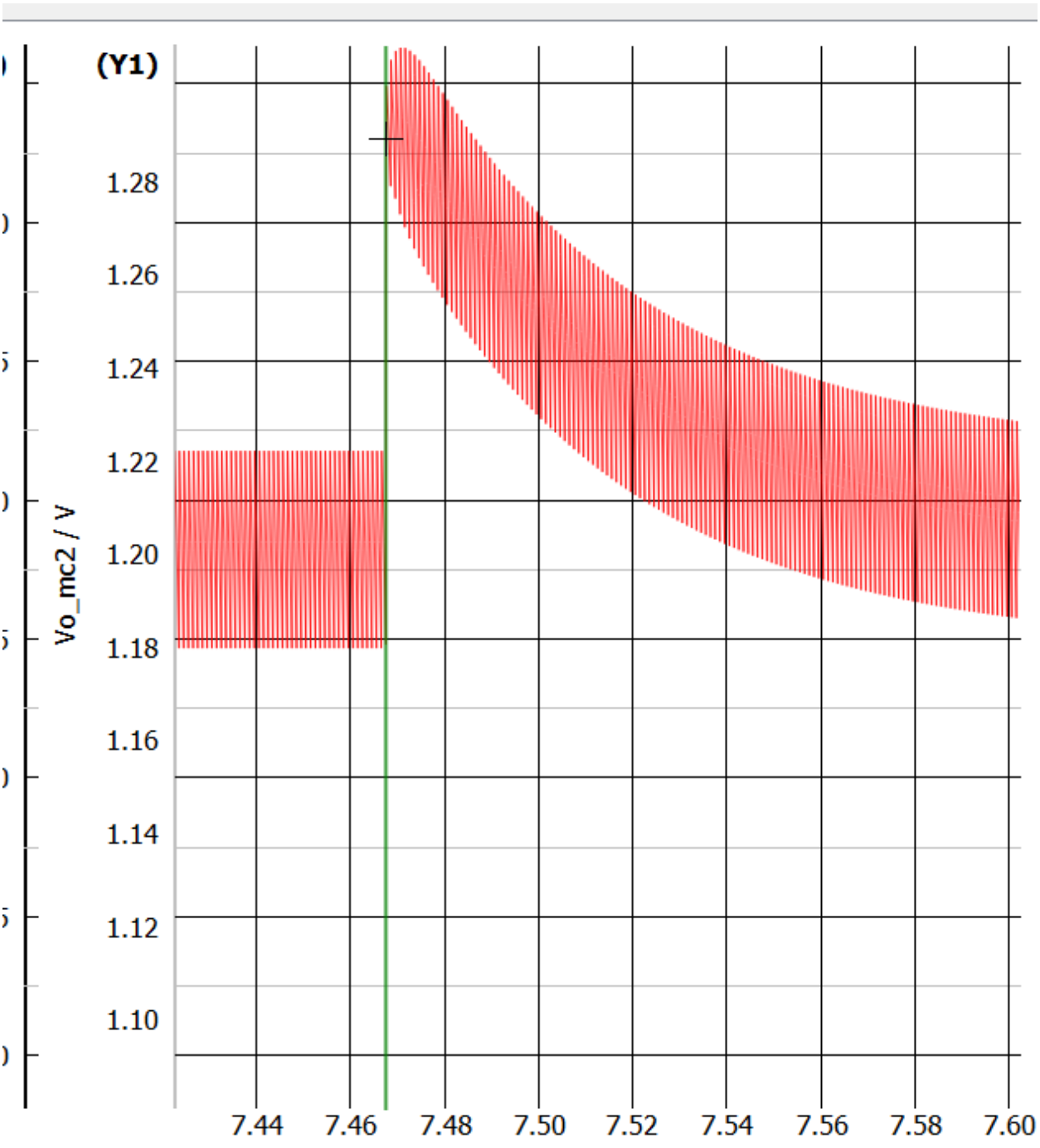
Comment: When mc increases, the settling time decreases because the low frequency pole of the power stage becomes faster, and overshoot decreases as the damping of the system increases

(3.2) Now change S_e so that $m_c=(1+s_e/s_n)$ equals 2, 4,16 respectively while keeping same bandwidth as in question 2 by adjusting only the gain of the compensator A(s). Compare the loop gain T_2 and load transient response for the three cases and *comment the results.*




(Y1)
1.35
1.30
1.25
1.20
1.15
1.10
1.05
Vo_mc16 / V
2.45
2.50
2.55
2.60
2.65
2.70
time/ms
50us/div


(Y2)
(Y1)
22.0
21.5
21.0
20.5
20.0
19.5
19.0
18.5
Vo_mc4 / V
1.30
1.25
1.20
1.15
1.10
2.46
2.48
2.50
2.52
2.54
2.56
2.58
2.60
2.62
2.64
time/ms
20us/div



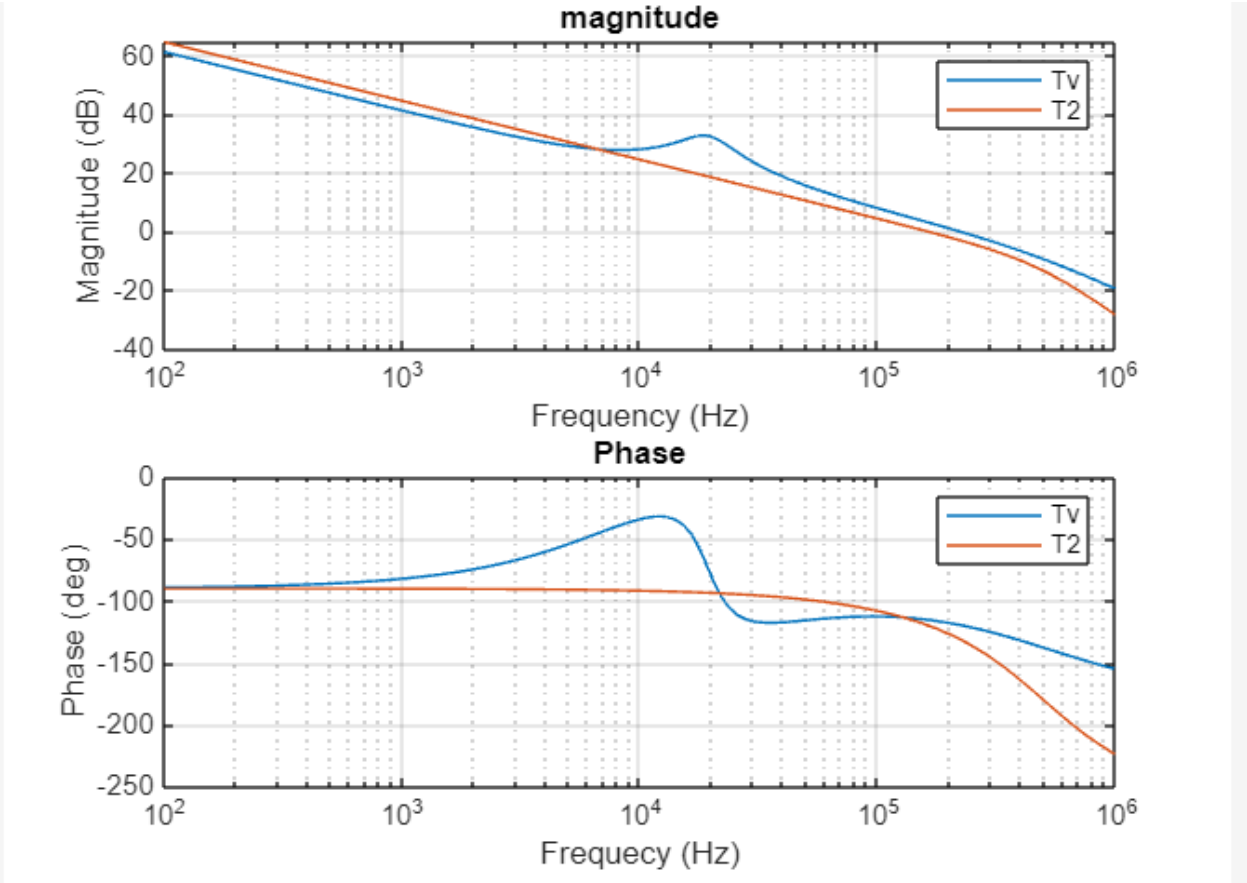
To have the same bandwidth, the gain of the compensator A(s) must increase to shift the crossover frequency a little bit to the right. And a higher mc value leads to lower phase margin.

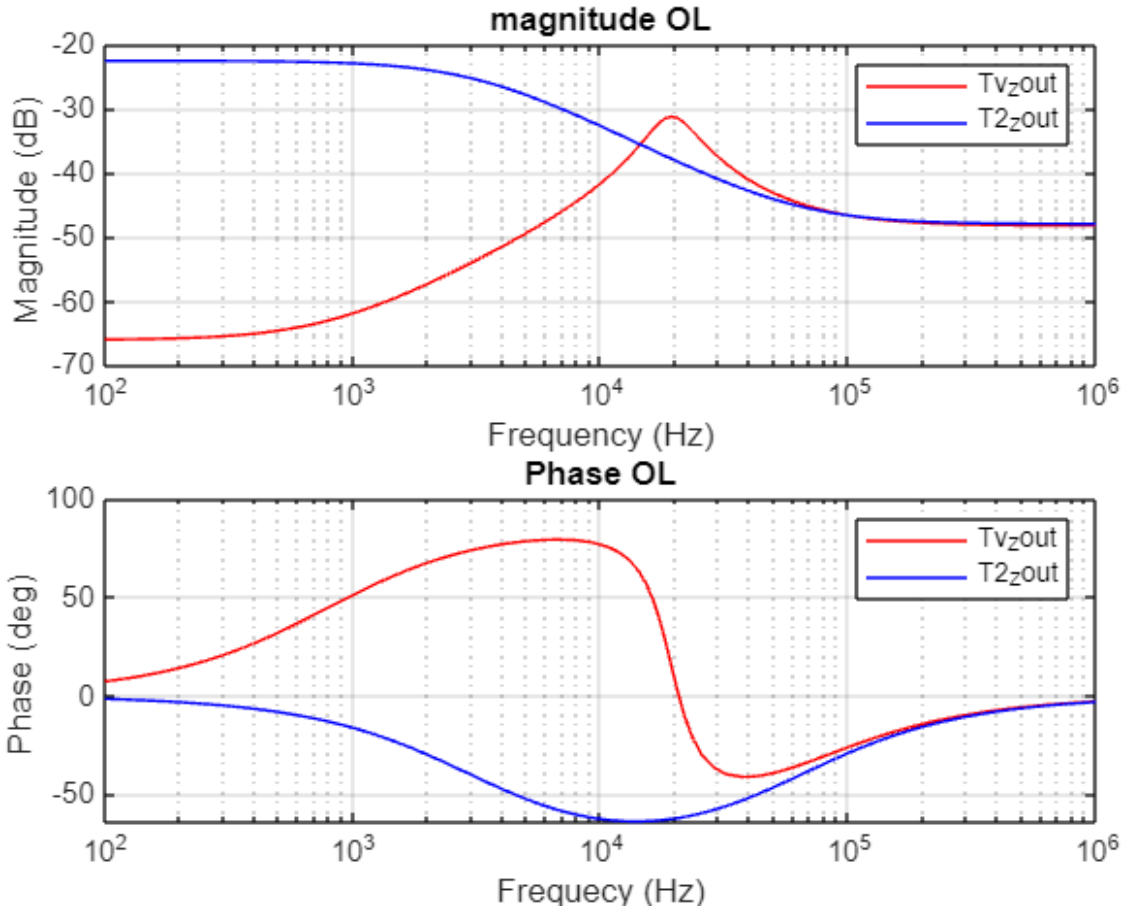
When mc increases, the settling time decreases because the low frequency pole of the power stage becomes faster and the gain of Zo decreases, and overshoot decreases and the damping of the system increases

4. Comparison of the loop gain T_2 and load transient responses (with load transient specified previously) between voltage mode and current mode control.

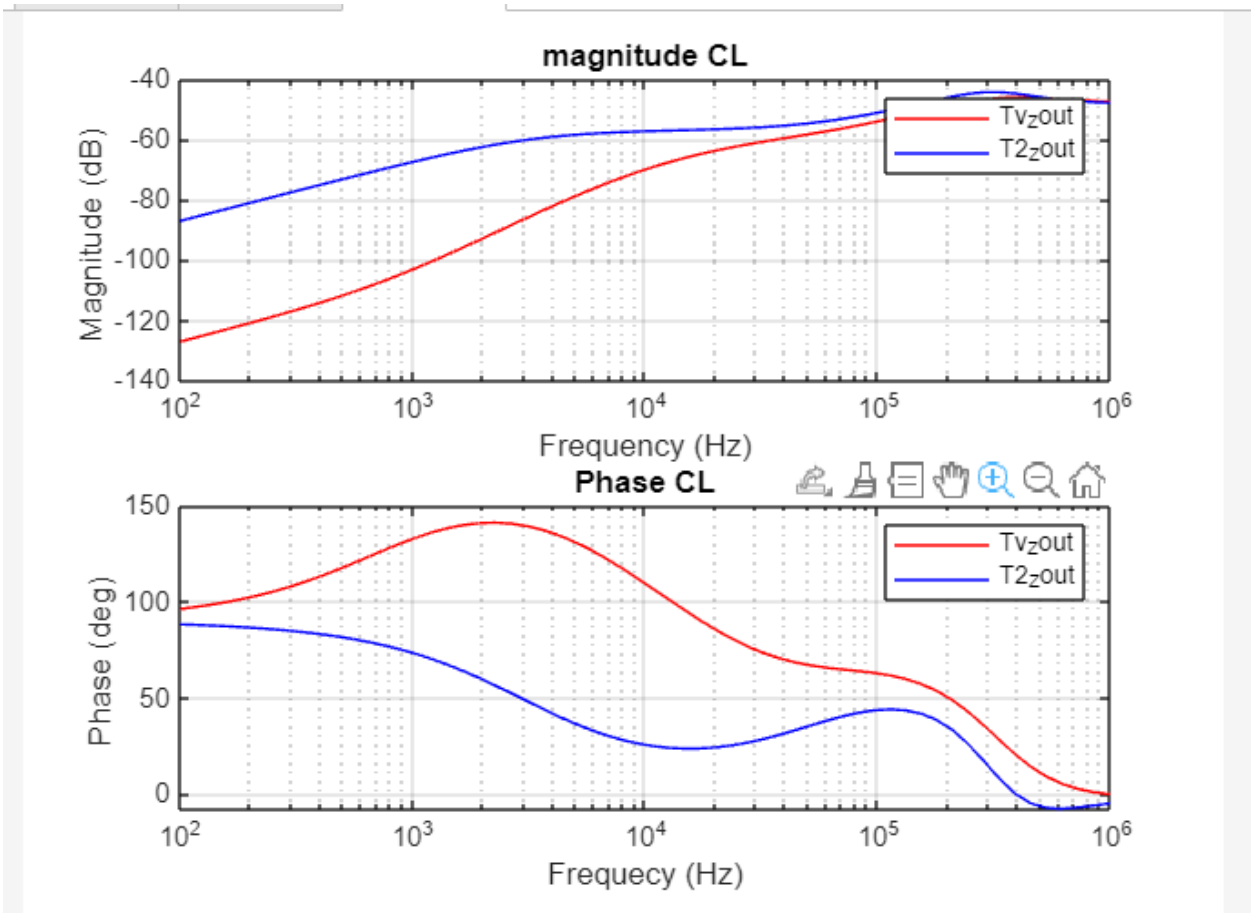
a. Same bandwidth design (50kHz): With the parameters specified in question 2 for current mode control and in question 3 (a) for voltage mode control in homework 3, make a comparison on the following aspects: (15%)

(1) Bode plots of the total loop gain (T_v in voltage mode control and T_2 in current mode control) in one graph, open loop output impedances Z_o in the second graph (With voltage loop open in voltage mode control; voltage loop open and current loop closed in current mode control), closed loop output impedances Z_{oc} in the third graph (With voltage loop closed in voltage mode control and all loops closed in current mode control).





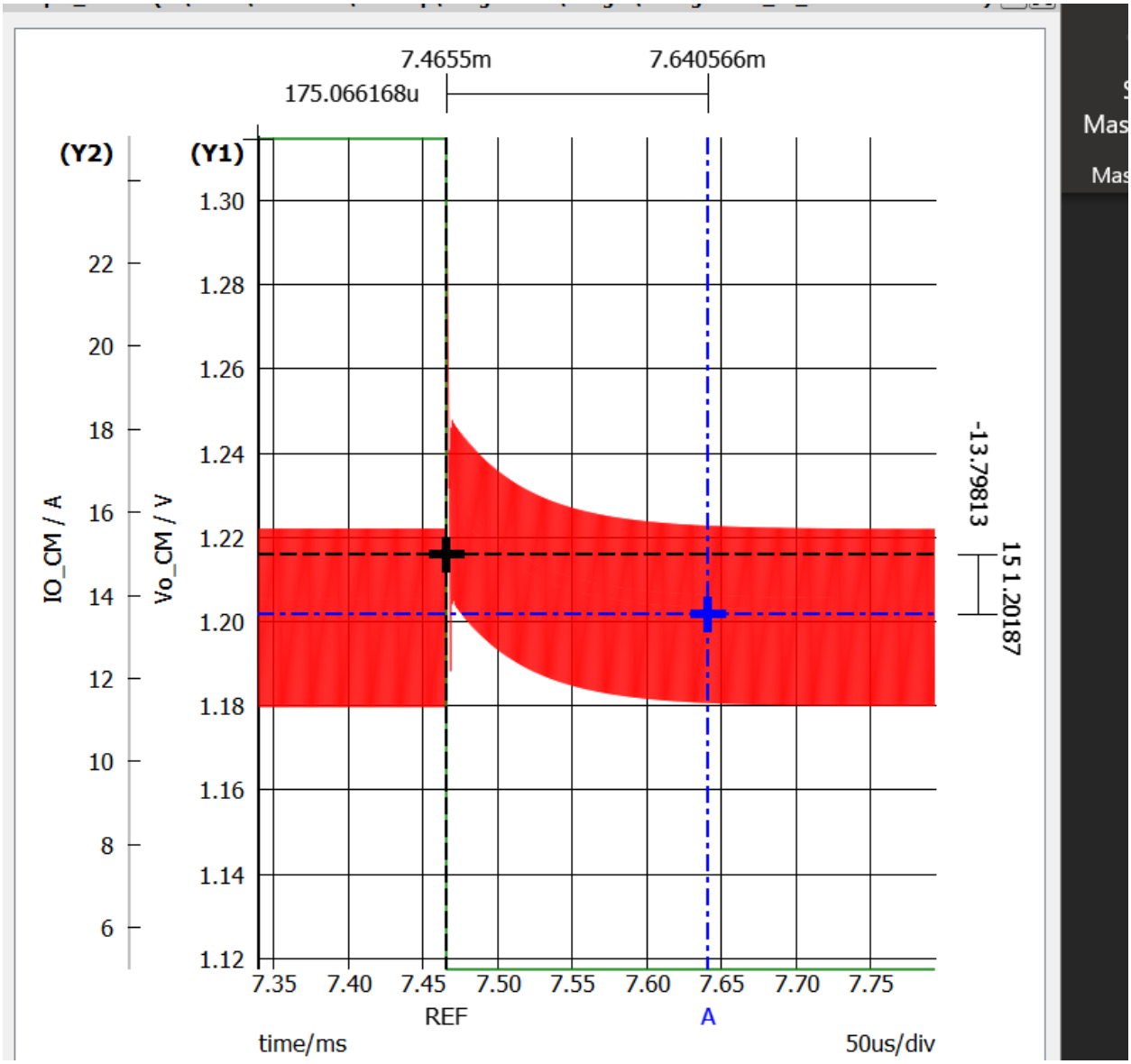
Open loop output impedances (With voltage loop open in voltage mode control; voltage loop open and current loop closed in current mode control)



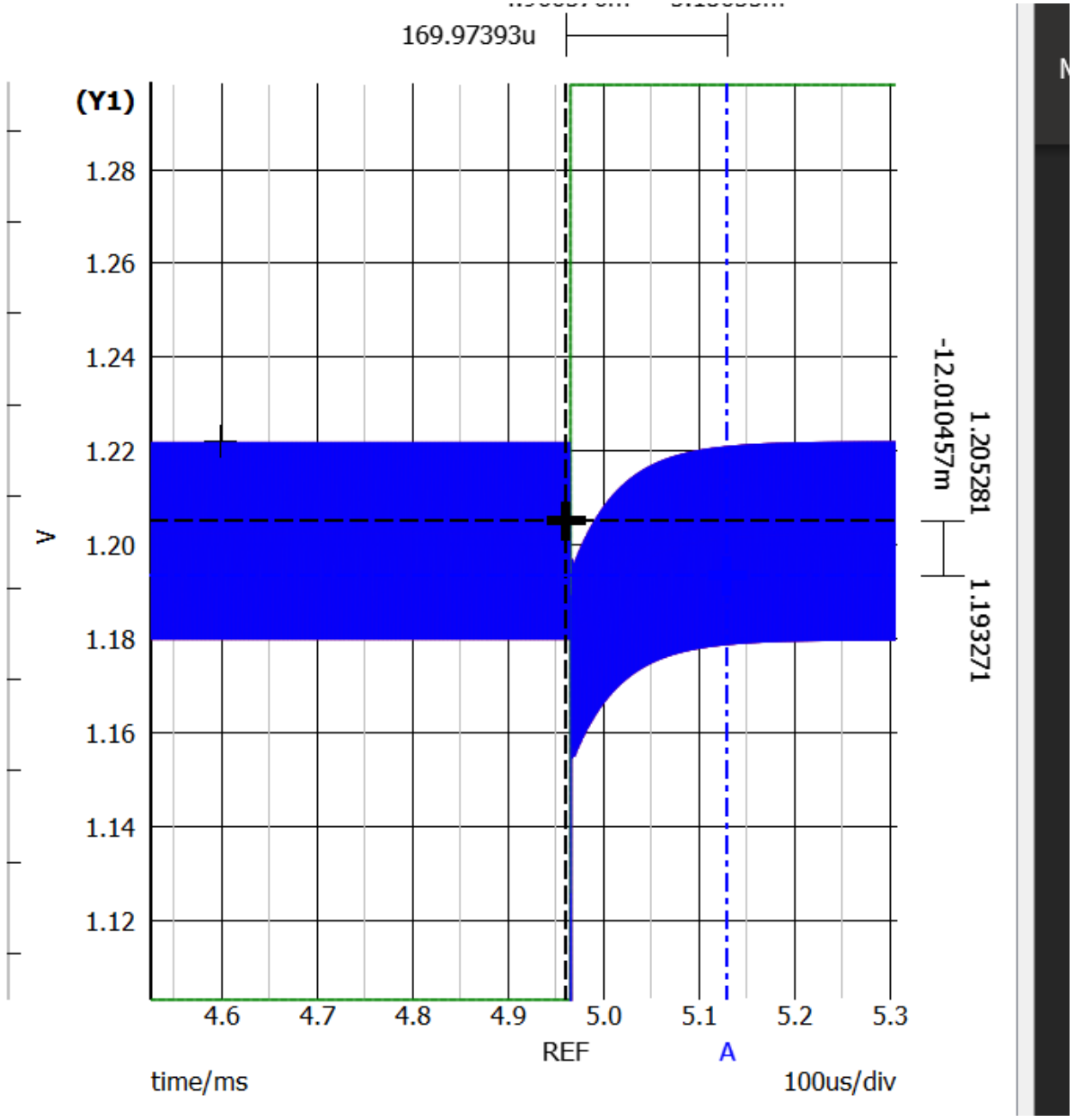
Closed loop output impedances Zoc in the third graph (With voltage loop closed in voltage mode control and all loops closed in current mode control).

b. Highest bandwidth design: please try to design the bandwidth of T_2 as high as possible in current mode control and design T_v as high as possible in voltage mode control in homework 3 (in both cases, please keep at least 60 degree phase margin). Make a comparison on the following aspects: (25%)
   (1) Bode plots of the total loop gain (T_v in voltage mode control and T_2 in current mode control) in one graph, closed loop output impedances Z_{oc} in the second graph (With voltage loop closed in voltage mode control and all loops closed in current mode control).
   (2) Compare the load transient response for these two controls in the third graph with the same load transient response (as specified previously). *Please comment the results.*

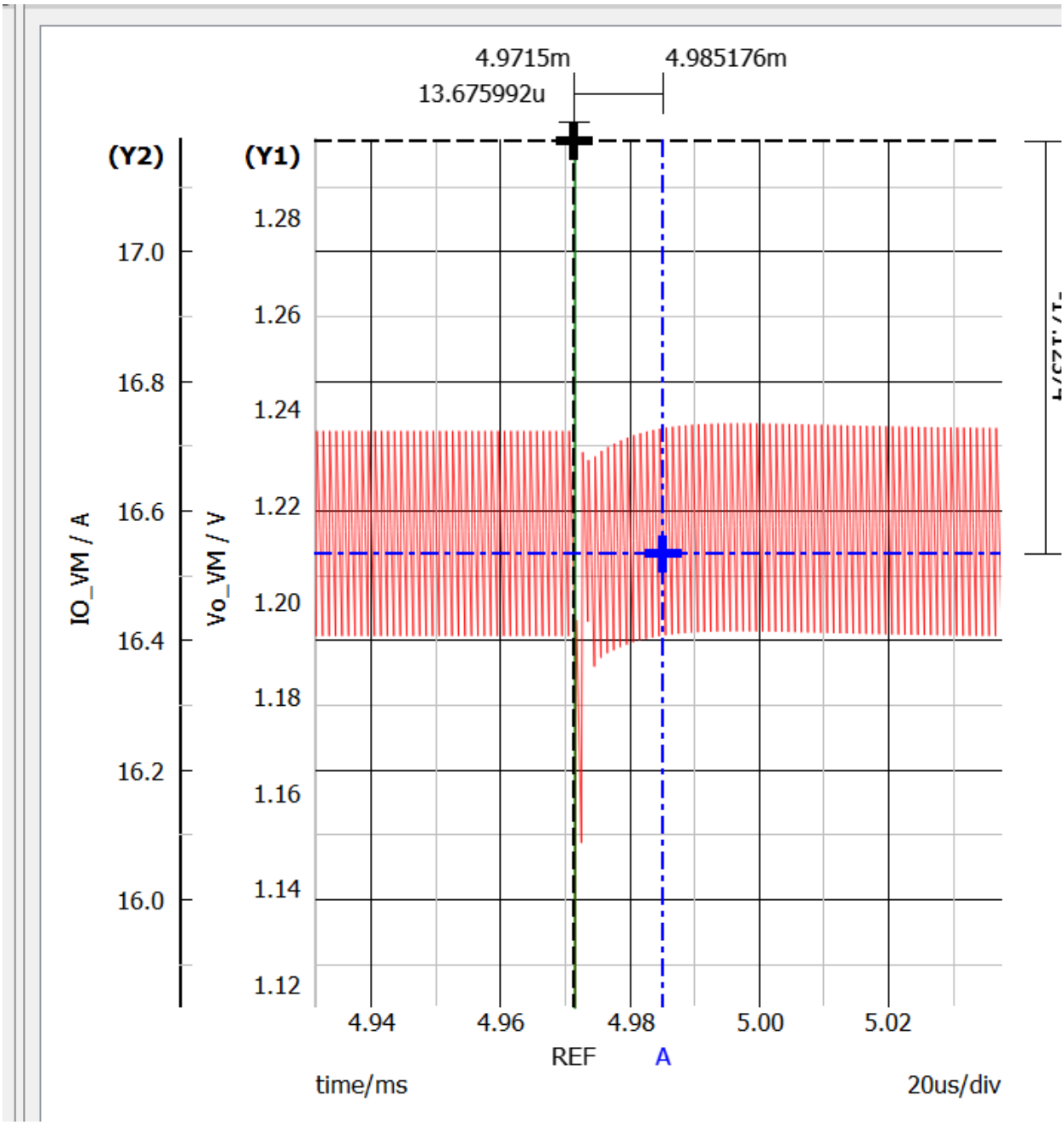
Current mode control overshoot 175 us



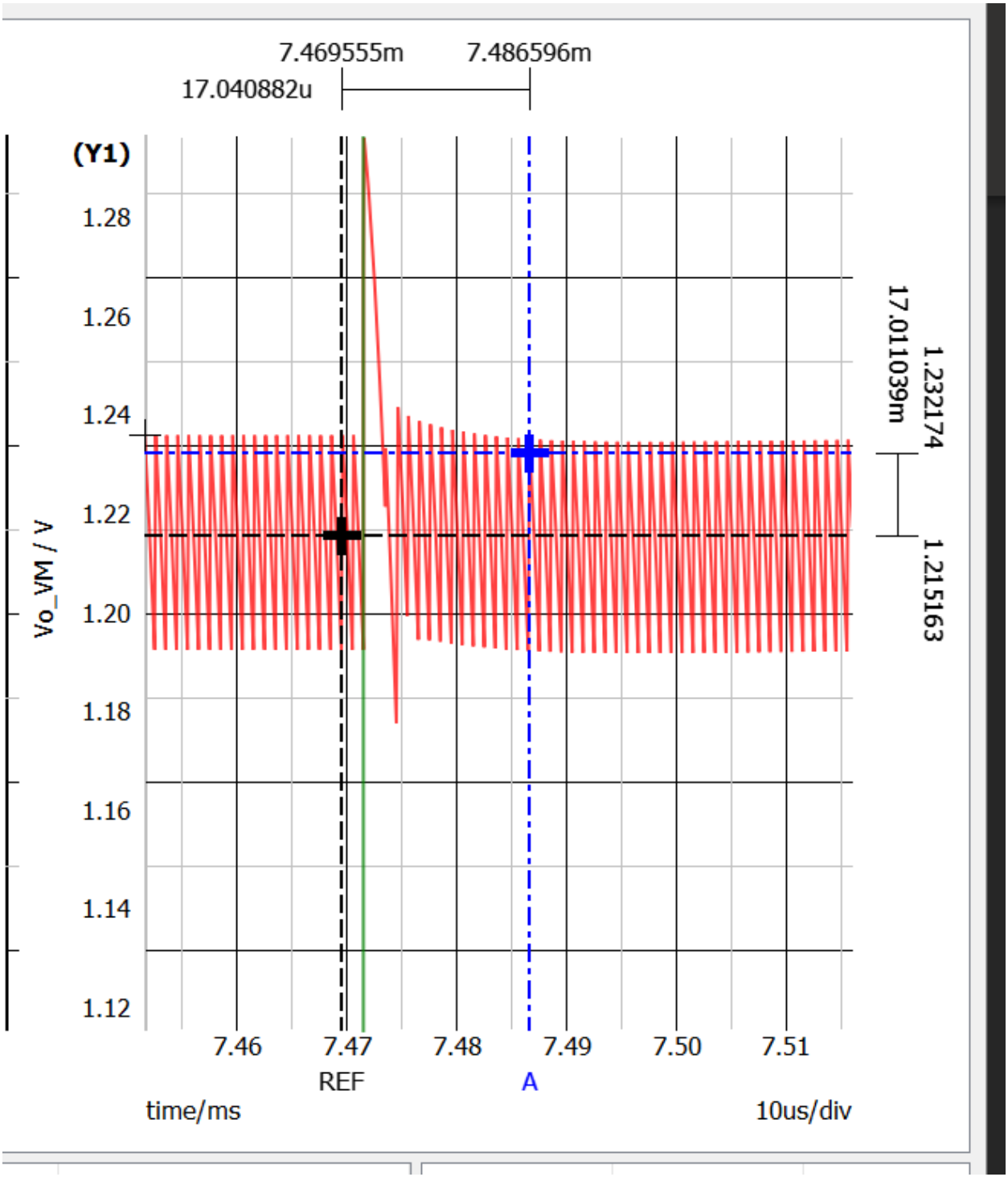
Undershoot of current mode control is (170 us)



Voltage mode control undershoot (13.6us)

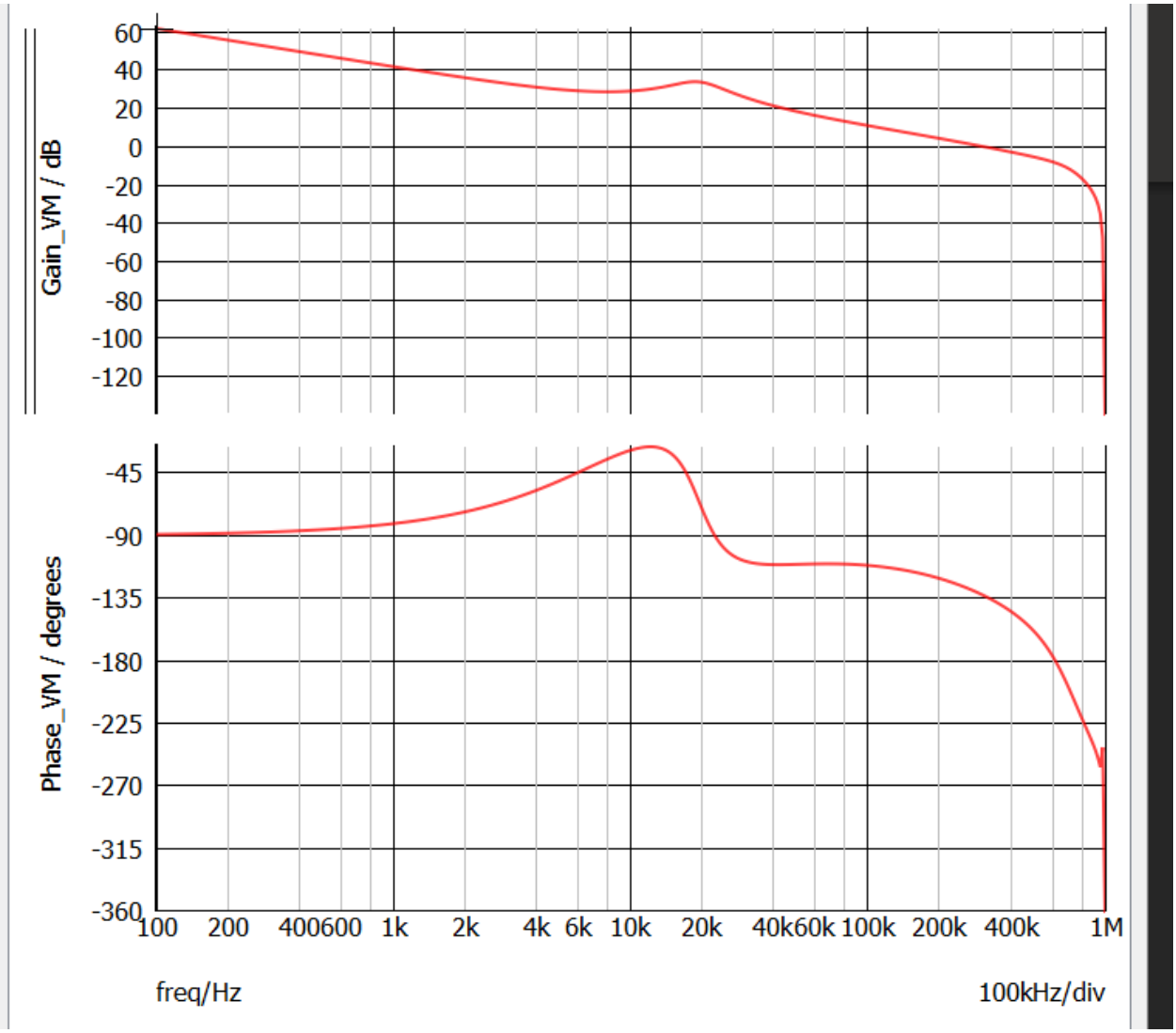


Voltage mode control overshoot is (17 us)

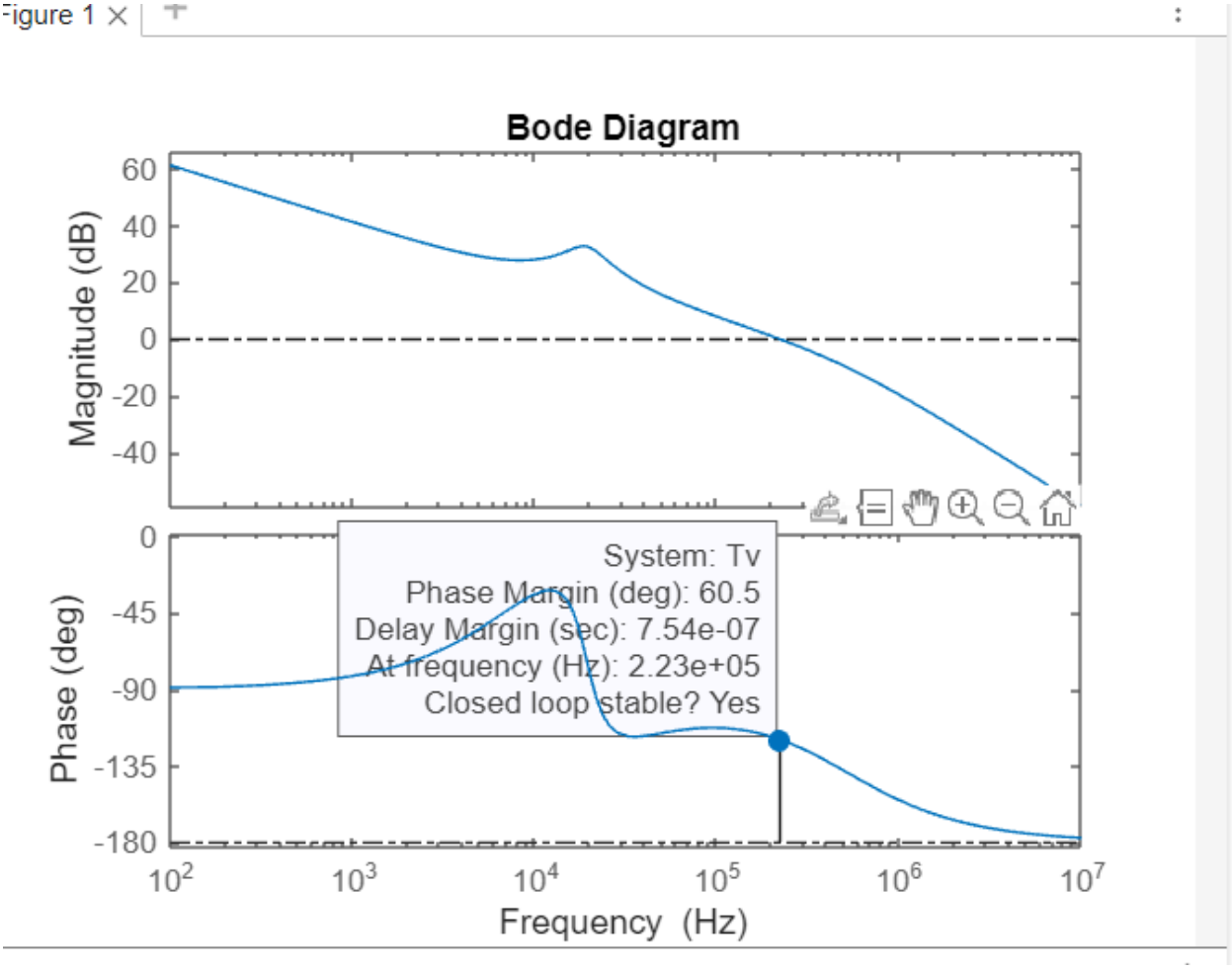


The settling time of the voltage control is lower than the current control because the mc slows the power stage pole and the overshoot is higher because the current control has high output impedance at low frequencies.

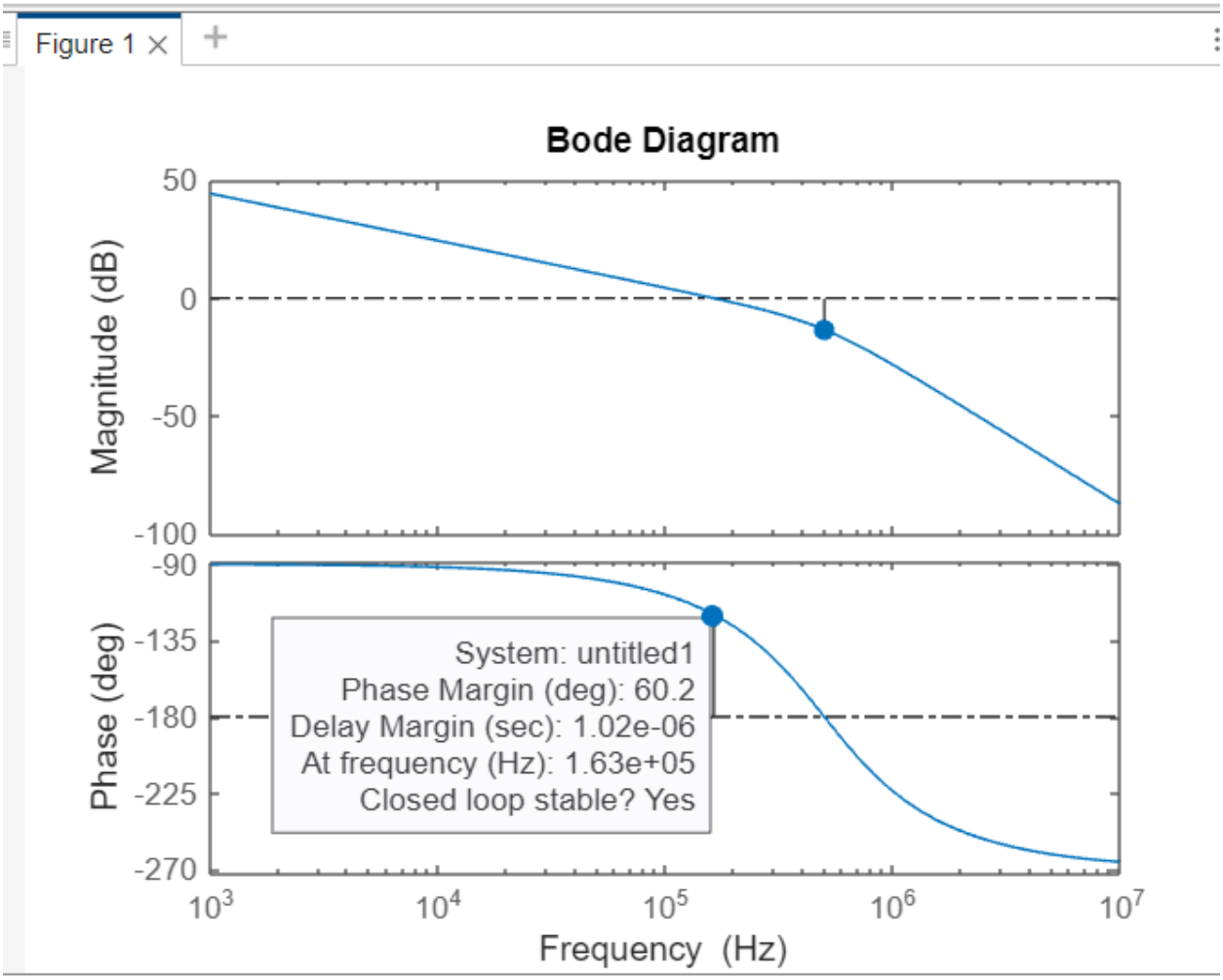
b. Highest bandwidth design: please try to design the bandwidth of T_2 as high as possible in current mode control and design T_v as high as possible in voltage mode control in homework 3 (in both cases, please keep at least 60 degree phase margin). Make a comparison on the following aspects: (25%)



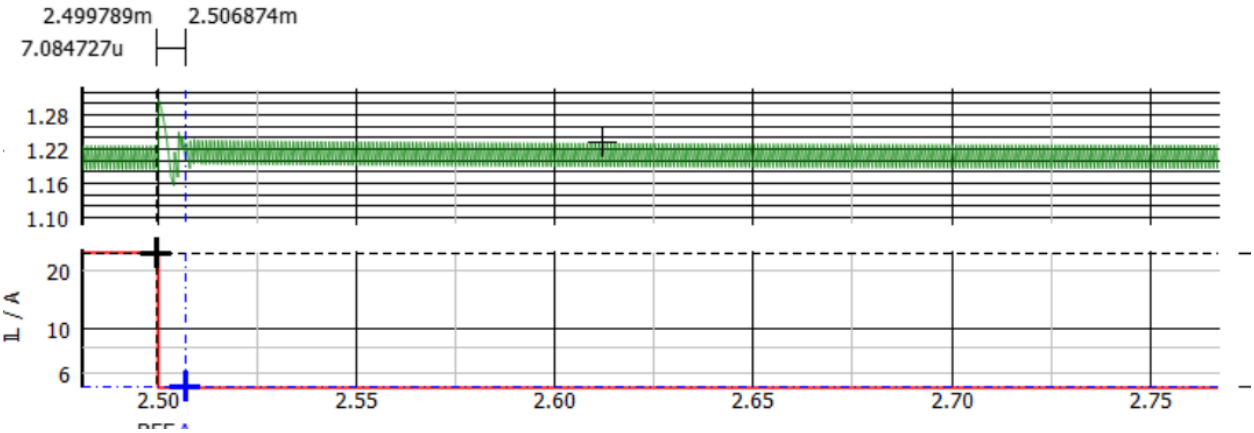
VOLTAGE MODE CONTROL

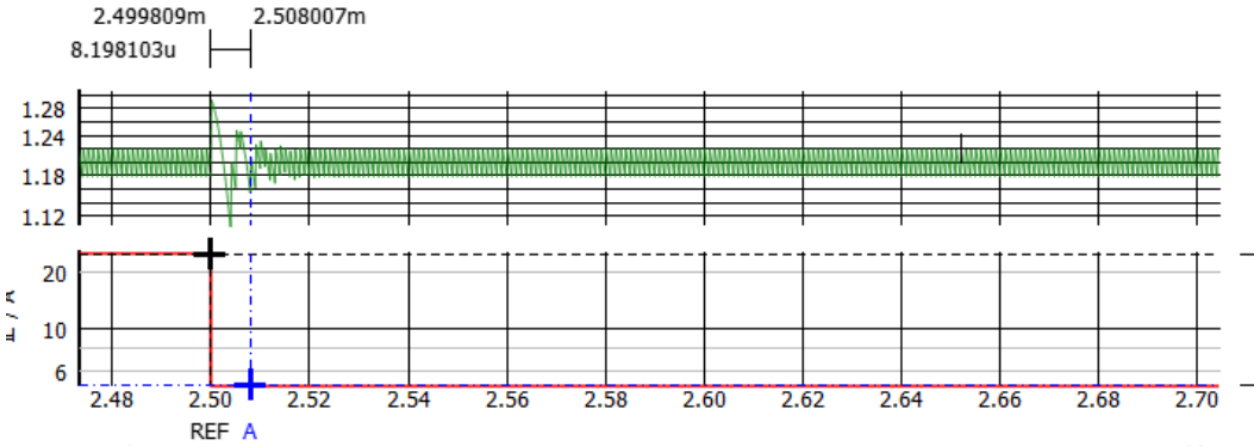


The highest bandwidth of VM control is 223 KHZ



Current mode control maximum BW is 163 KHZ





At highest bandwidth the current mode has lower settling time because the current mode has faster poles and higher phase margin, but the overshoot is higher because the current mode inherits high impedance which leads to high overshoot at transient.

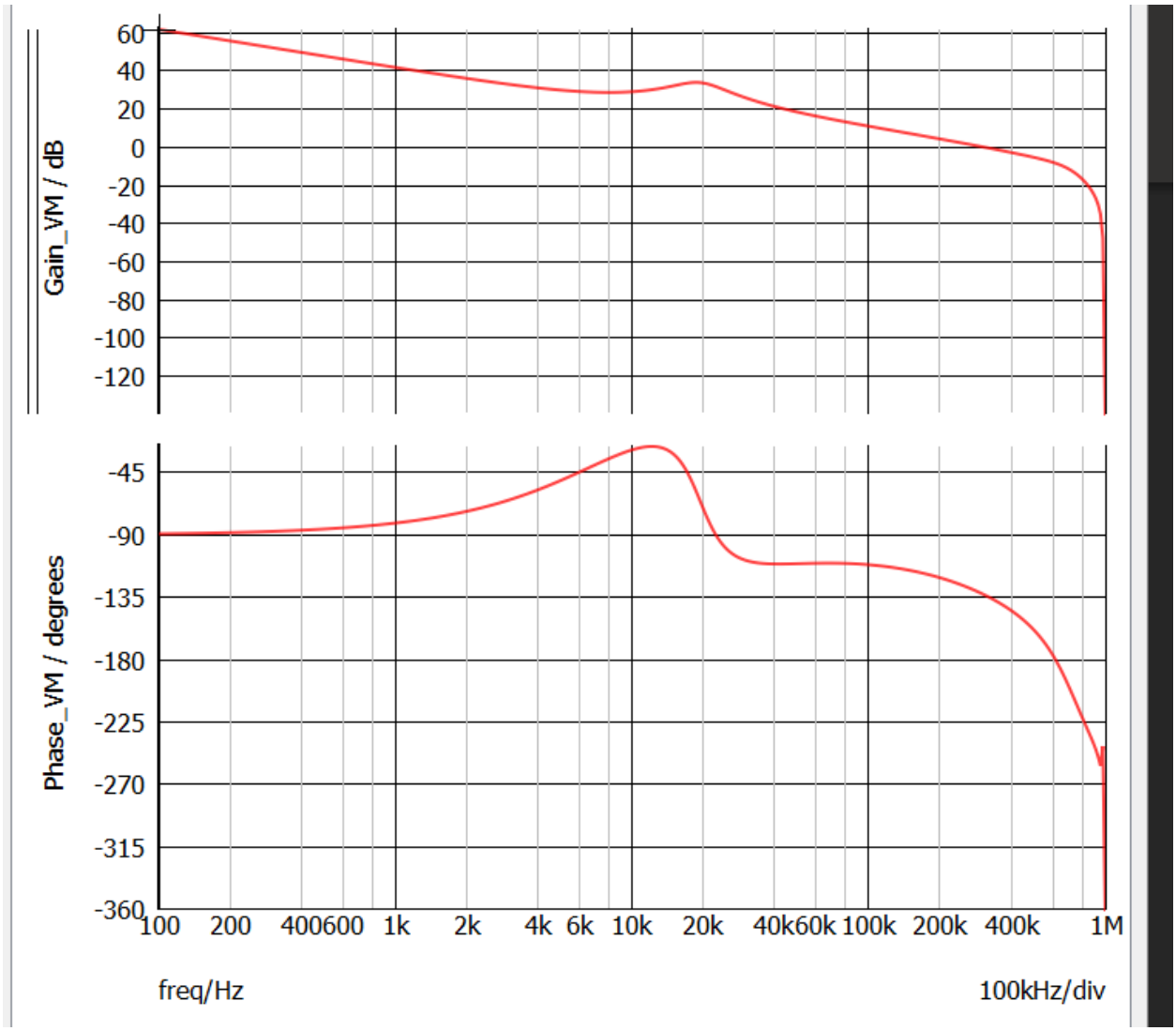
(3) Discussion 1: compare the bandwidth of T_v in voltage mode control and T_2 in current mode control, state your observation on which bandwidth is higher and explain the reason.

The current mode has lower bandwidth because the current loop has instability and to overcome this instability se is introduced to damp the current perturbation and that limits the maximum bandwidth.

higher and explain the reason.

(4) Discussion 2: compare the modeling result and simulation result of the loop gain T_v in voltage mode control, state your observation on whether they agree with each other and explain why. Compare the modeling result and simulation result of the loop gain T_2 in current mode control, state your observation on whether they agree with each other and explain why.

TV from simplis VS TV small signal model


Gain_VM / dB
60
40
20
0
-20
-40
-60
-80
-100
-120
Phase_VM / degrees
-45
-90
-135
-180
-225
-270
-315
-360
100
200
400600
1k
2k
4k
6k
10k
20k
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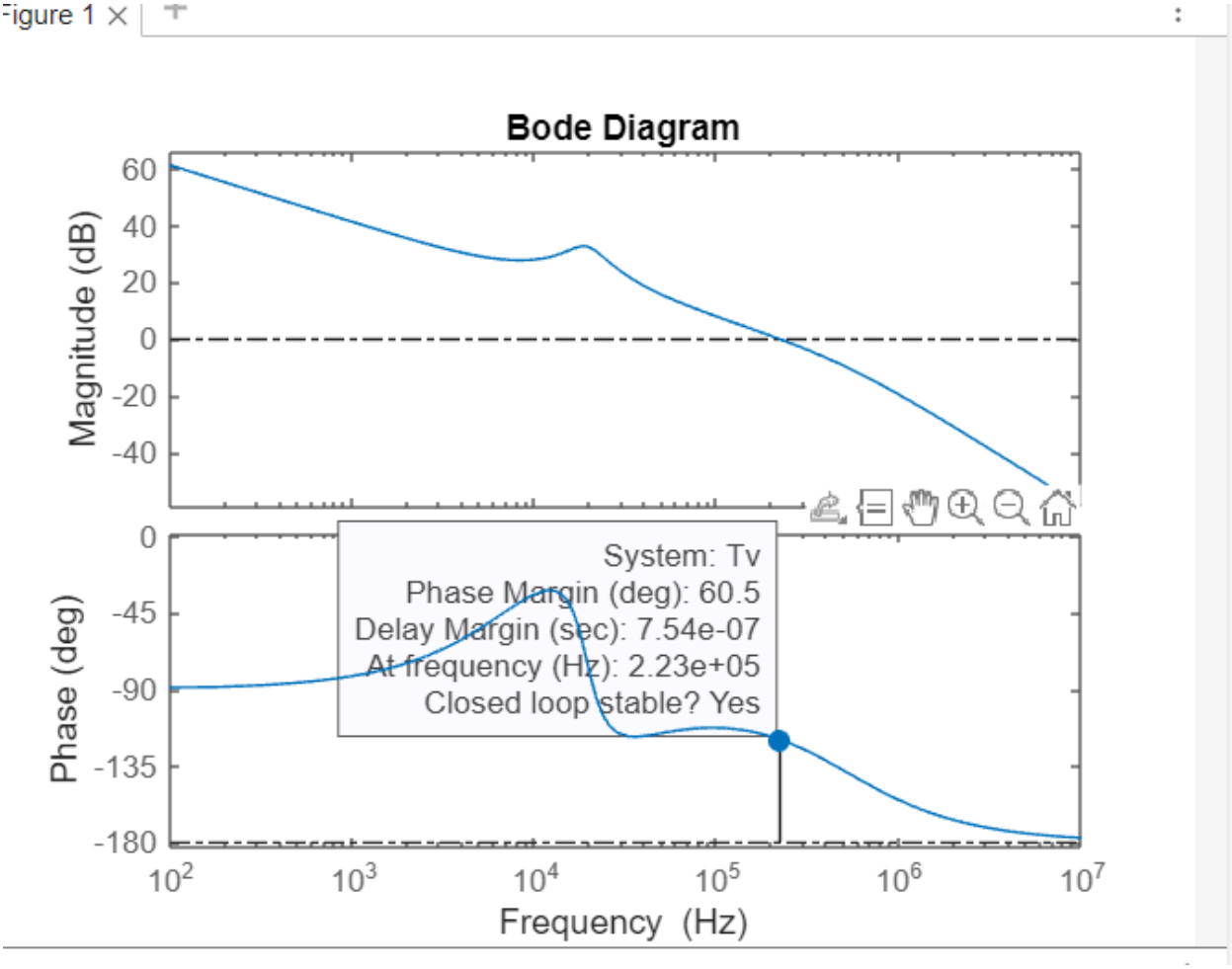
100k
200k
400k
1M
freq/Hz
100kHz/div



The simulation and model results nearly the same because the PWM power stage model truly represents the converter.

For CMC

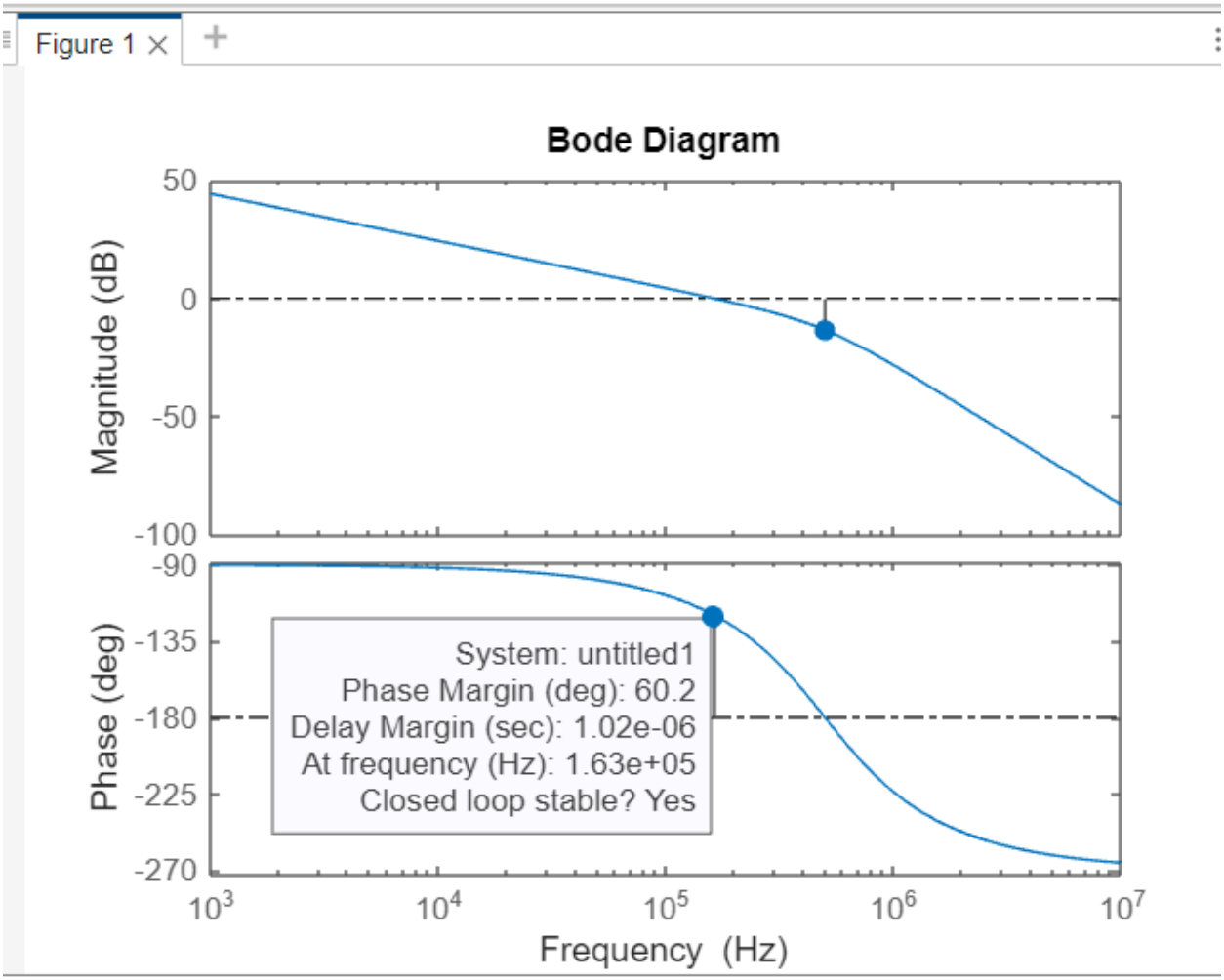
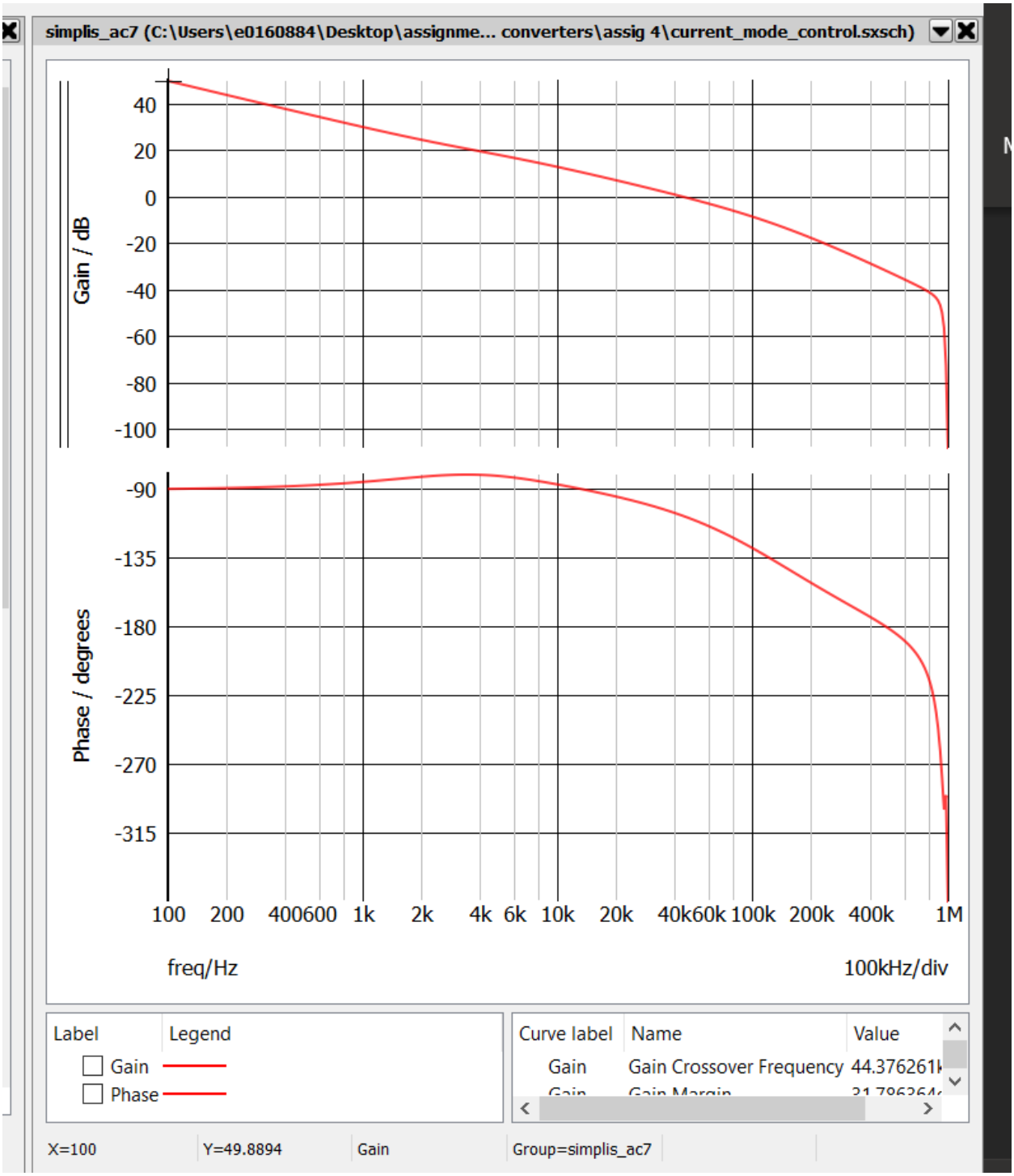
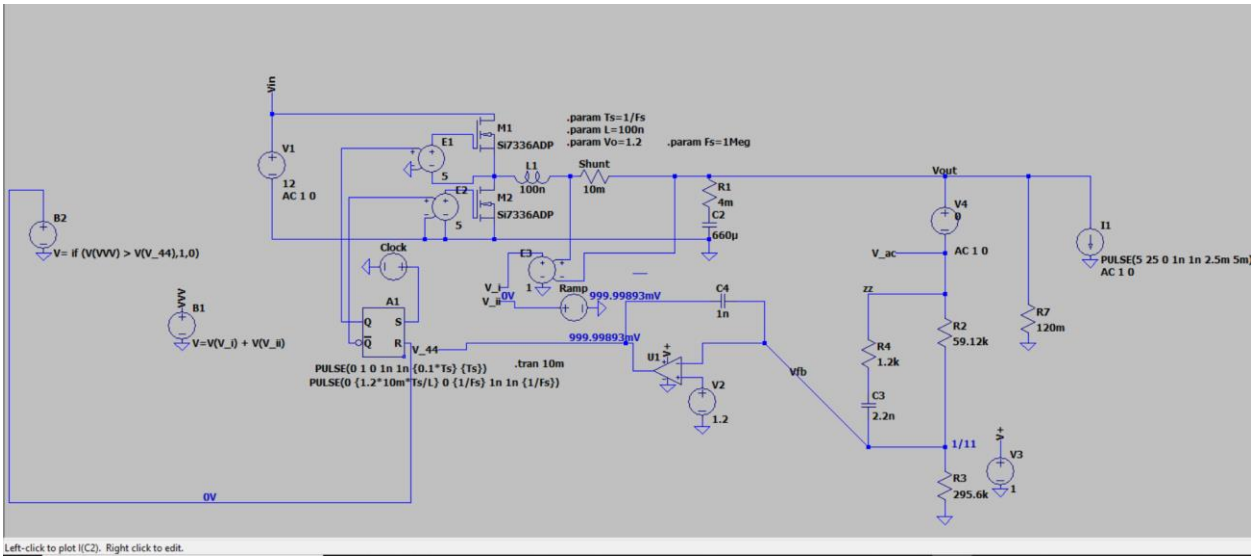


Figure 1
Bode Diagram
Magnitude (dB)
50
0
-50
-100
Phase (deg)
-90
-135
-180
-225
-270
System: untitled1
Phase Margin (deg): 60.2
Delay Margin (sec): 1.02e-06
At frequency (Hz): 1.63e+05
Closed loop stable? Yes
10^3
10^4
10^5
10^6
10^7
Frequency (Hz)

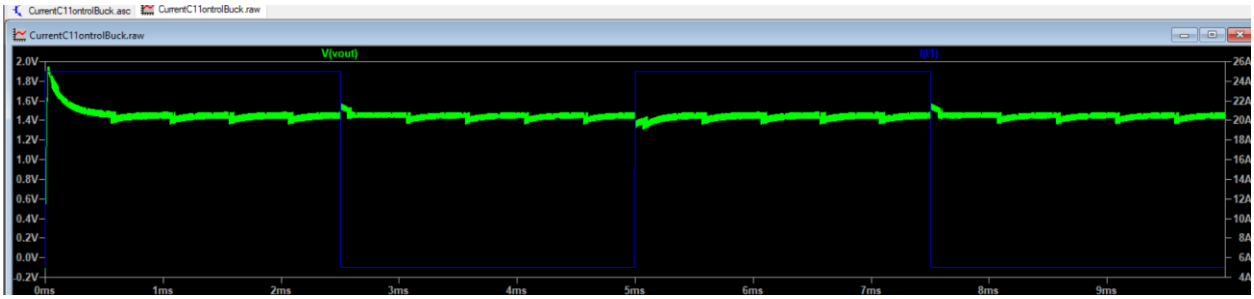


For mc values near the 1, the simulation and model results differs because the peak current mode models have many assumptions. The sampling effect introduces He(s) to have infinite zeros-poles is to be simplified as a 2nd order system. The current loop is much faster than the voltage loop and that introduces error when using PWM switch models.

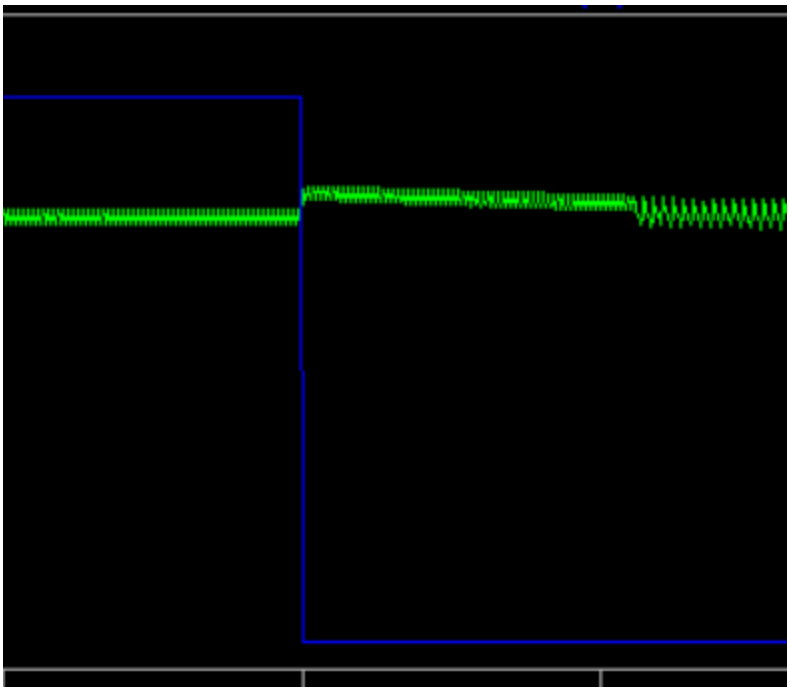
LTSPICE Validation:



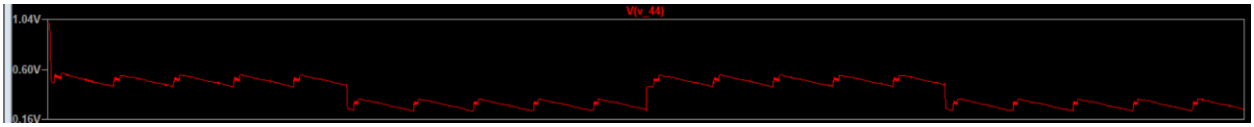
LTspice model



Output voltage



Out voltage Overshooting



Error signal