EEE 3101: Digital Logic and Circuits

Shift Register

Course Teacher: Nafiz Ahmed Chisty

Head, Department of EEE
Associate Professor, Department of EEE & CoE
Faculty of Engineering
Room# D0105, D Building
Email: chisty@aiub.edu
Website: http://engg.aiub.edu/faculties/nafiz
Website: www.nachisty.com

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Basic Shift Register Functions

A register is a digital circuit with two basic functions: **data storage and data movement**.

Shift registers consist of arrangements of flip-flops and are important in applications involving the storage and transfer of data in a digital system. Following figure illustrates the concept of storing a 1 or a 0 in a D flip-flop.
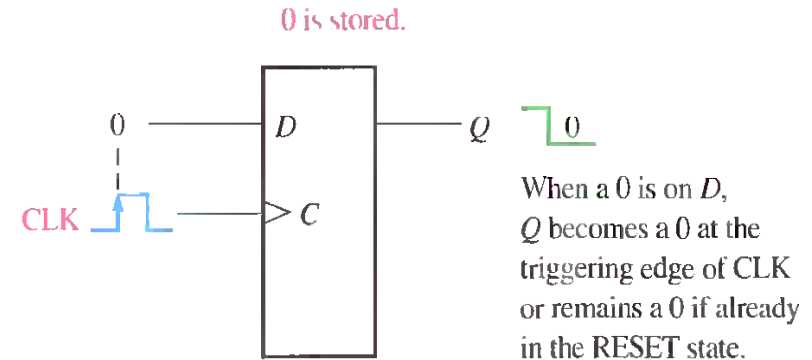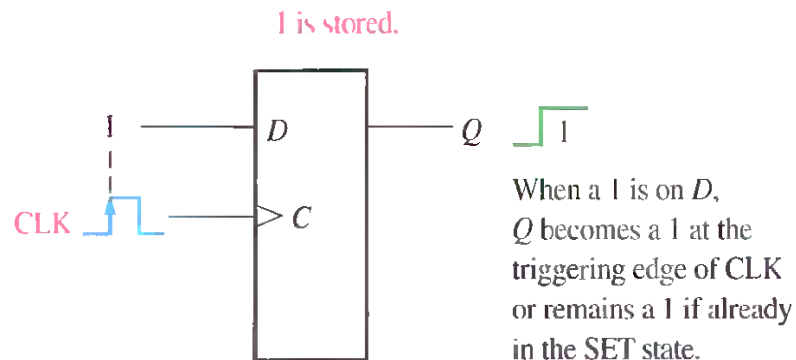
Each stage (flip-flop) in a shift register represents one bit of storage capacity; therefore, the number of stages in a register determines its storage capacity.
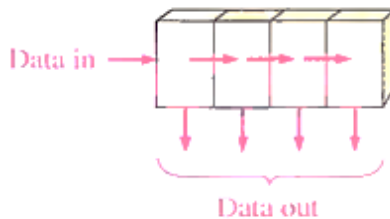
The shift capability of a register permits the movement of data from stage to stage within the register or into or out of the register upon application of clock pulses.

Based on the types of data movement, shift registers can be of 4 types:
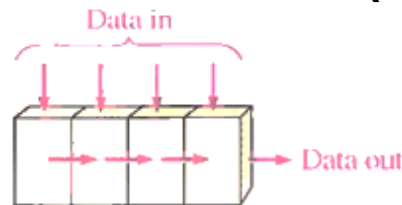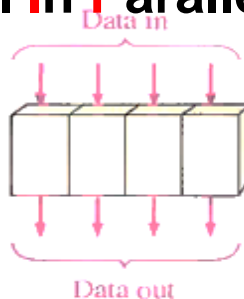
Serial In Serial Out (SISO)

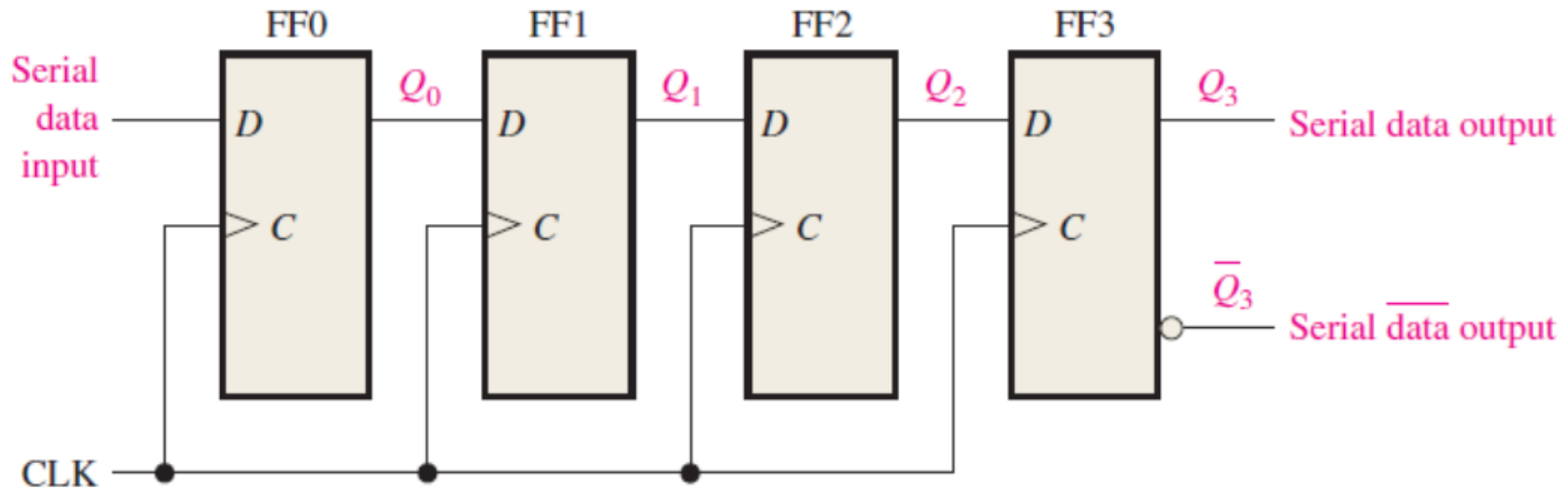## Serial In Parallel Out (SIPO)

Parallel In Serial Out (PISO)
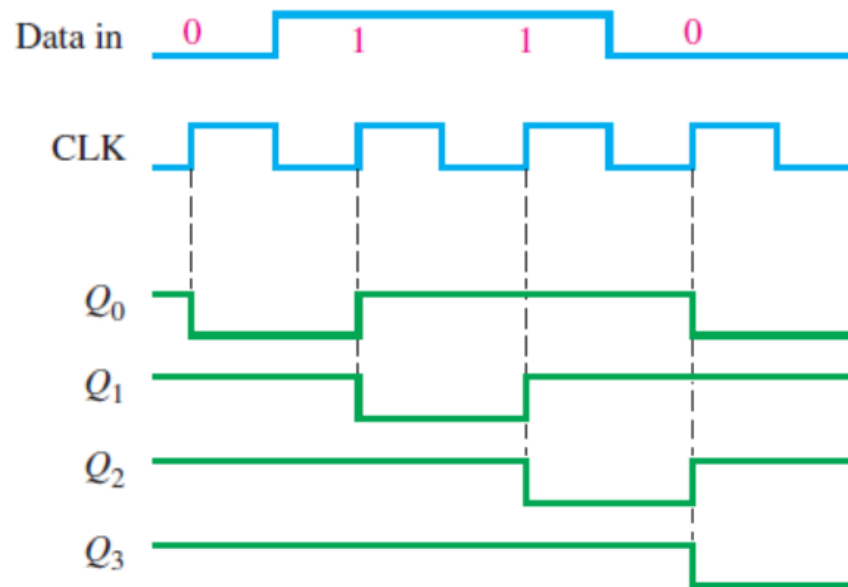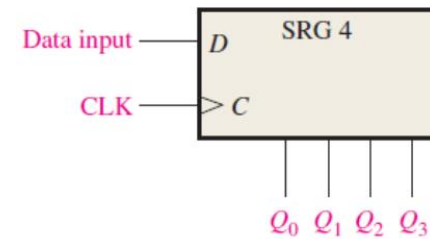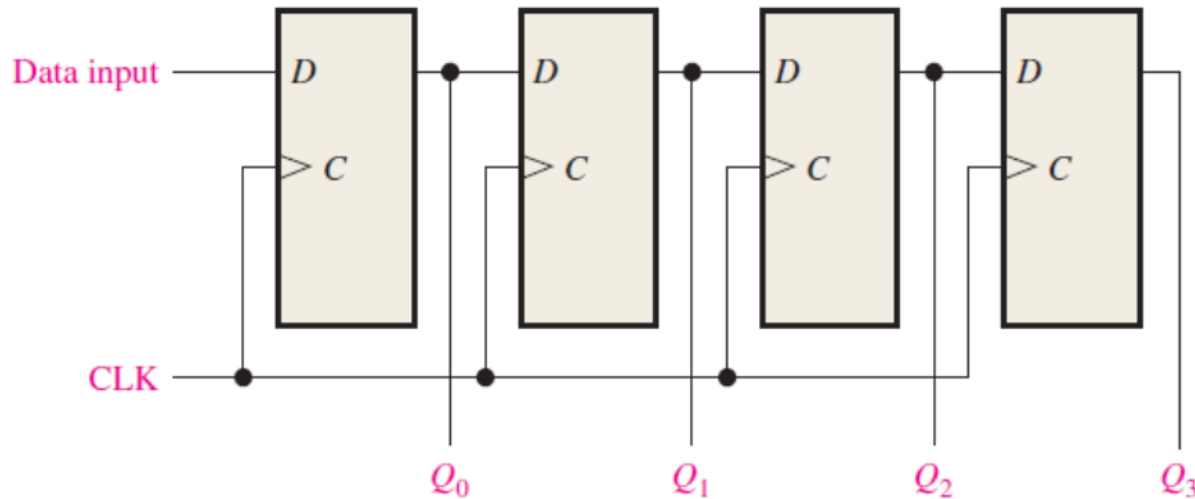

Parallel In Parallel Out (PIPO)

arrows indicate the direction of data movement

Serial IN/Serial OUT Shift Register

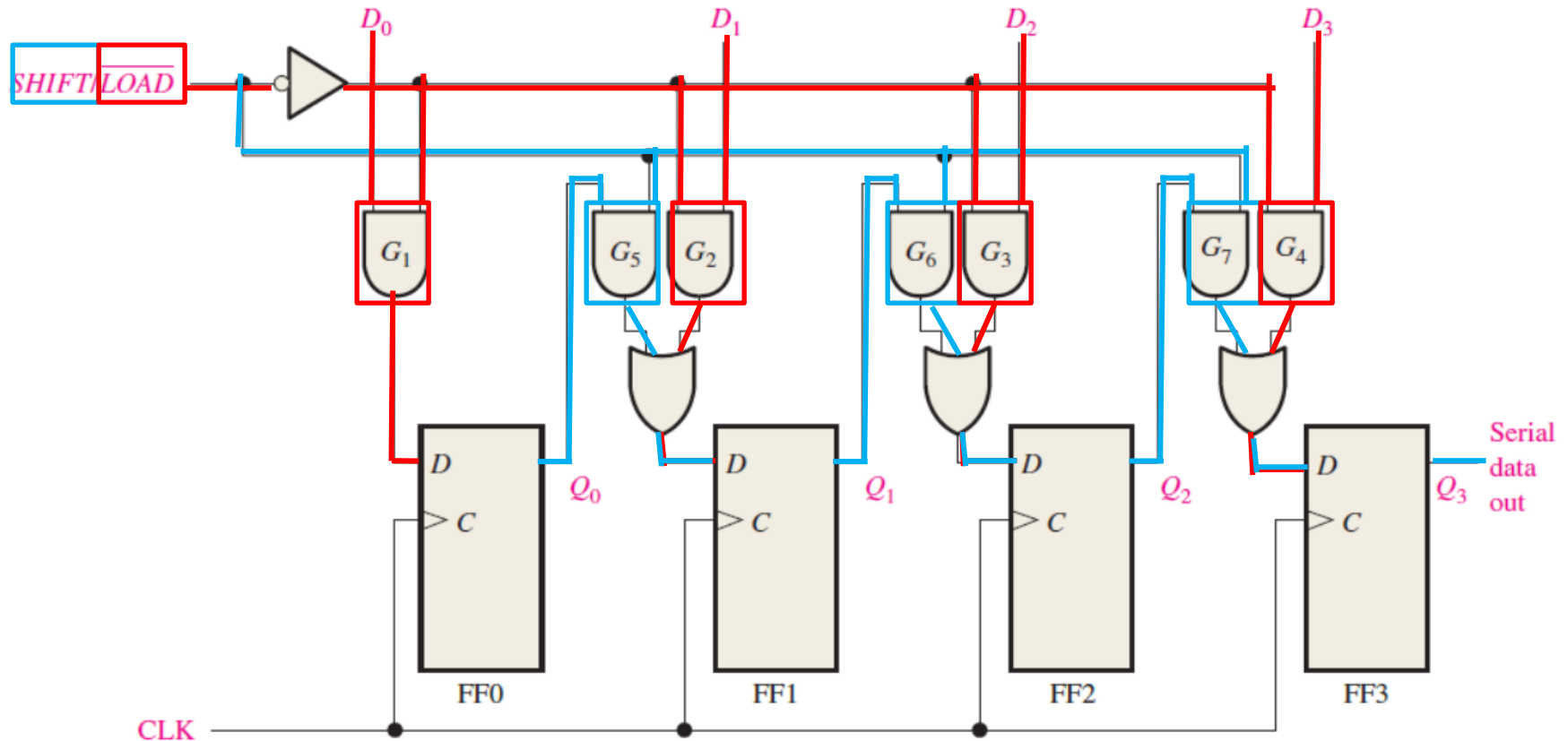The serial in/serial out shift register accepts data serially-that is, one bit at a time on a single line. It produces the stored information on its output also in serial form.

Serial IN/Serial OUT Shift Register
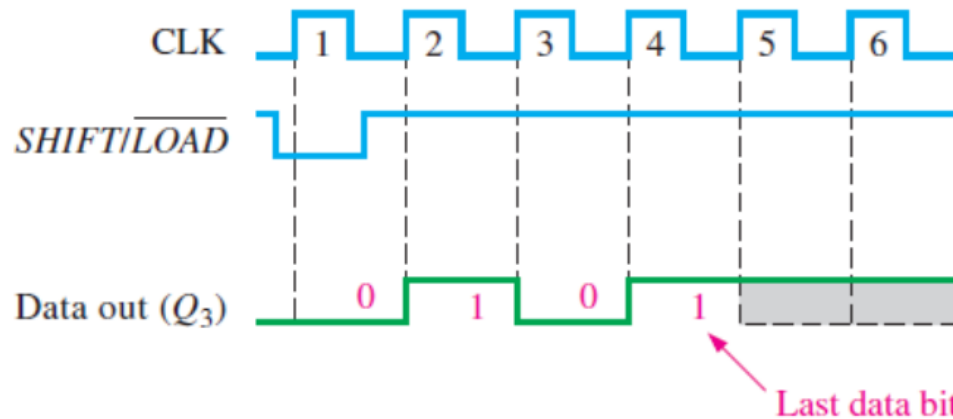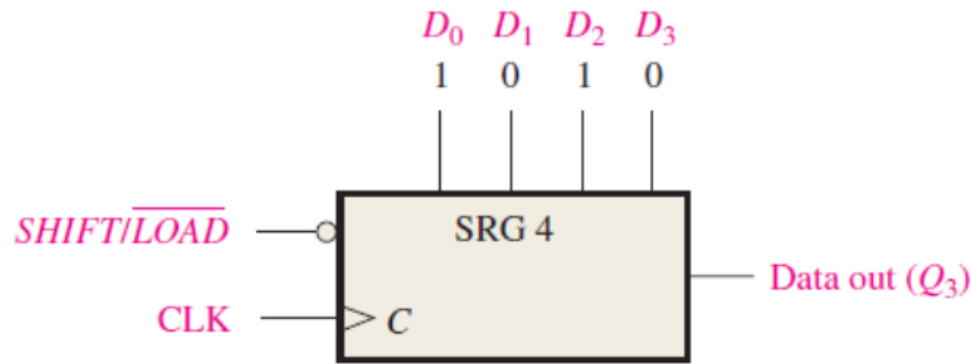
Serial IN/Parallel OUT Shift Register

Parallel IN/Serial OUT Shift Register

Shift/$\overline{\text{Load}}$ = 0, Load line gets activated.

Shift/$\overline{\text{Load}}$ = 1, Shift line gets activated.

Parallel IN/Serial OUT Shift Register

On clock pulse 1, the parallel data ($D_0 D_1 D_2 D_3 = 1010$) are loaded into the register, making Q_3 a 0. On clock pulse 2 the 1 from Q_2 is shifted onto Q_3; on clock pulse 3 the 0 is shifted onto Q_3; on clock pulse 4 the last data bit (1) is shifted onto Q_3; and on clock pulse 5, all data bits have been shifted out, and only 1s remain in the register (assuming the D input remains a 1).

Parallel IN/Parallel OUT Shift Register
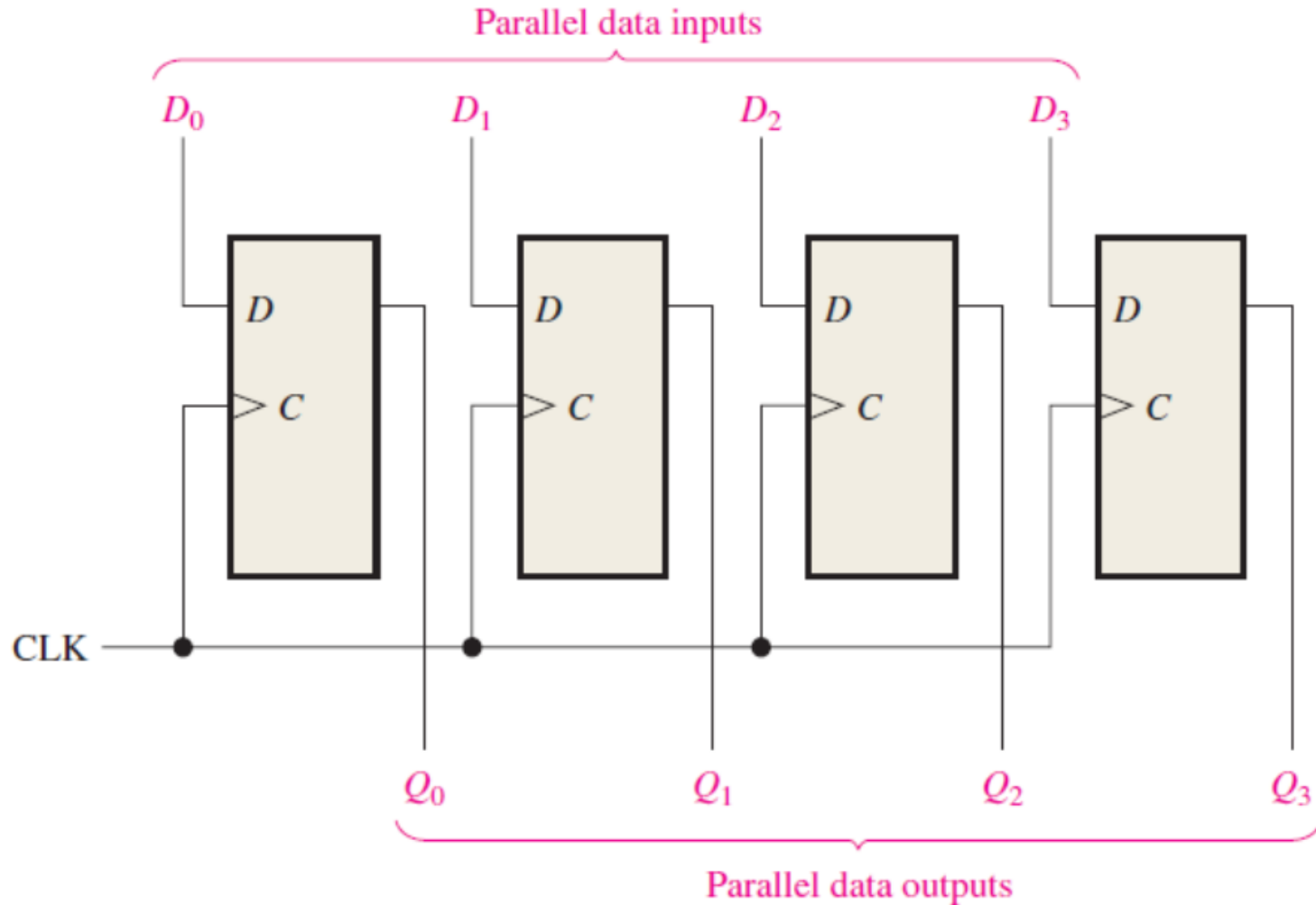
SISO Shift Registers

For Right Shift:

Data In | 0 | 1 | 2 | 3 | Output

For Left Shift:

Output | 0 | 1 | 2 | 3 | Data In
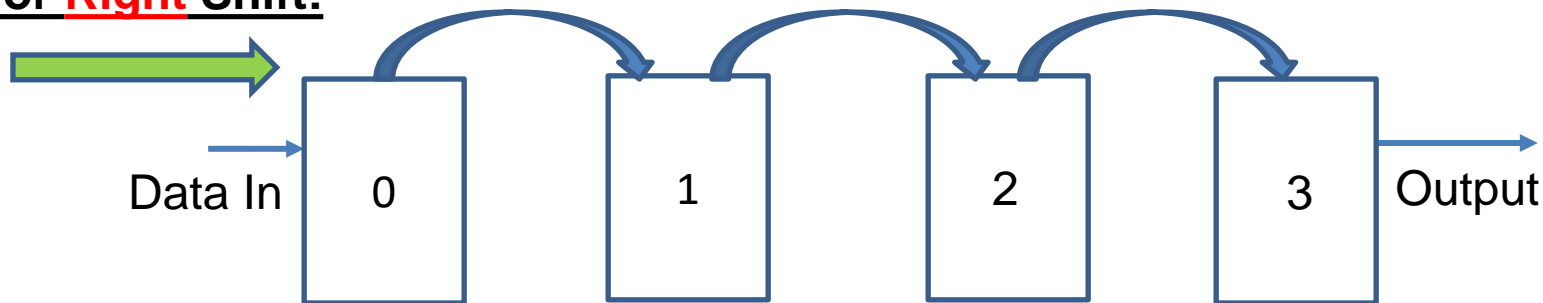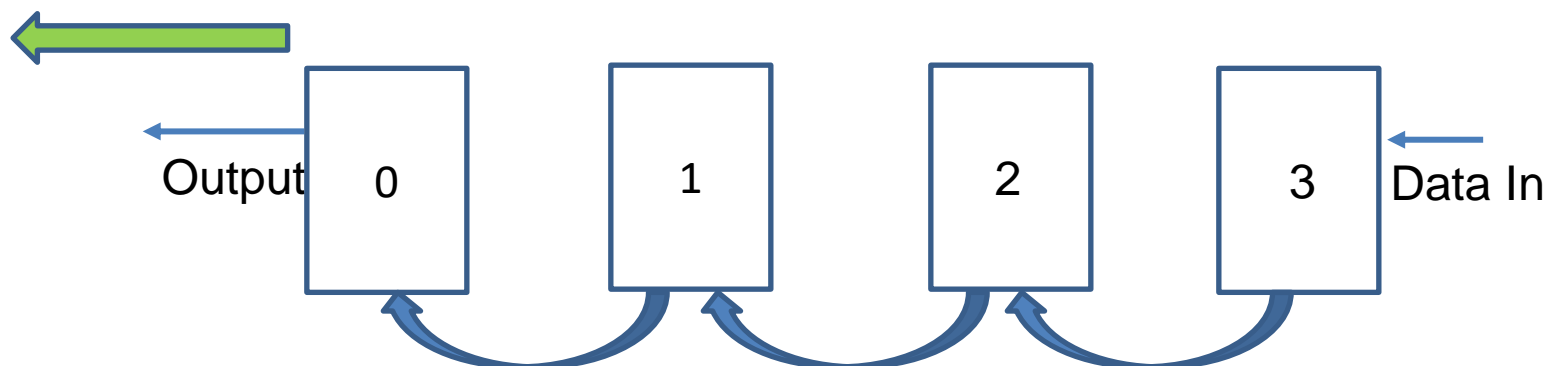
BIDIRECTIONAL SISO Shift Registers

Right Shift:

Left Shift:

Data In | 0 | 1 | 2 | 3 | Output

Output | | | | | Data In
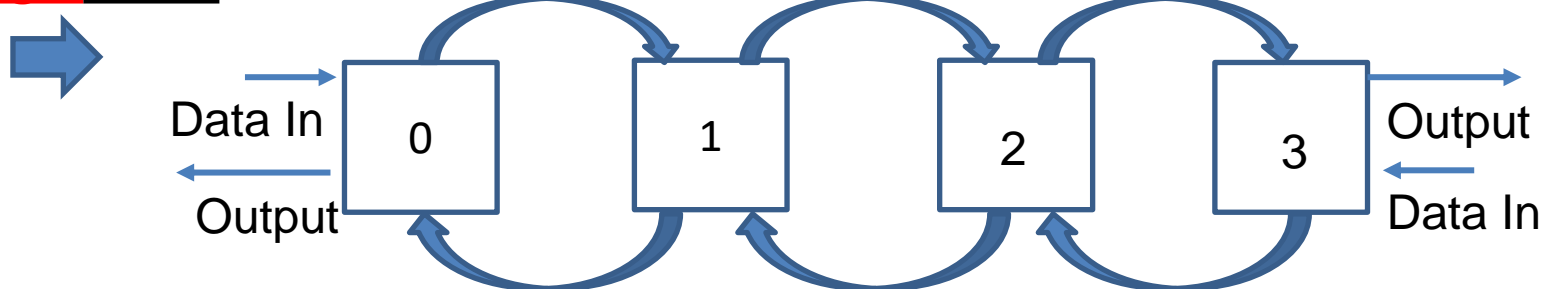
BIDIRECTIONAL Shift Registers
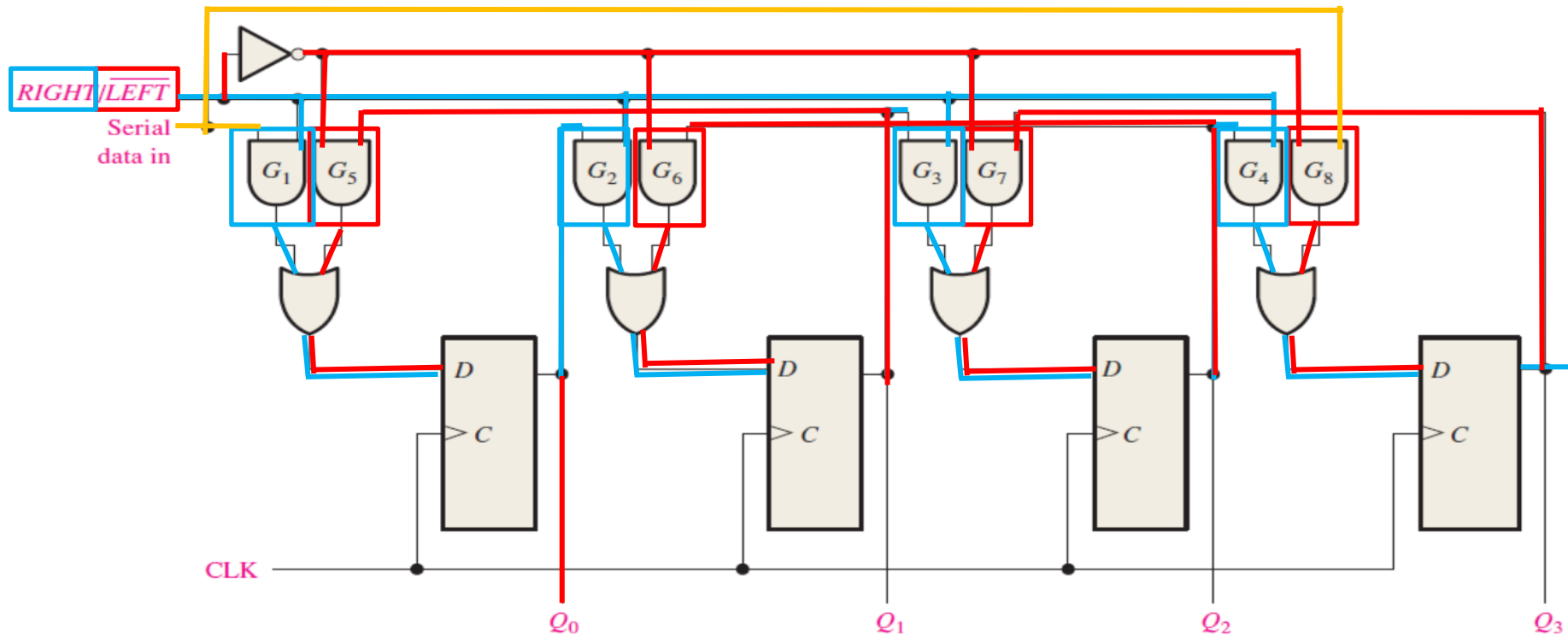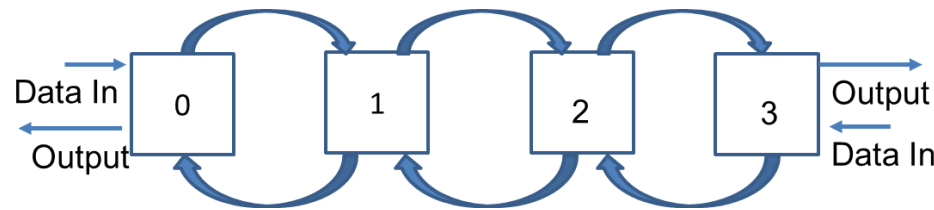
Right/$\overline{\text{Left}}$ = 0, Left line gets activated.

Right/$\overline{\text{Left}}$ = 1, Right line gets activated.

BIDIRECTIONAL Shift Registers

Data In → | 0 | 1 | 2 | 3 | → Output

Output ← | | | | | ← Data In
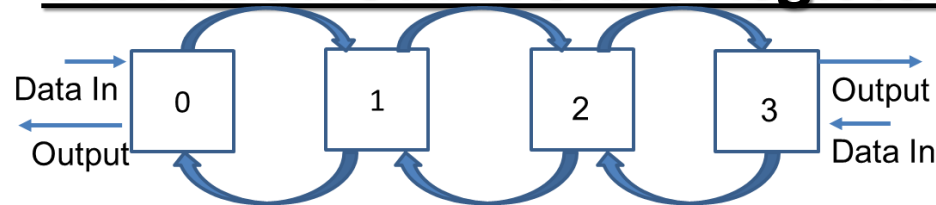
Determine the state of the shift register of Figure 9–19 after each clock pulse for the given $RIGHT/\overline{LEFT}$ control input waveform in Figure 9–20(a). Assume that $Q_0 = 1$, $Q_1 = 1$. $Q_2 = 0$. and $Q_3 = 1$ and that the serial data-input line is LOW.

BIDIRECTIONAL SISO Shift Registers

Optional
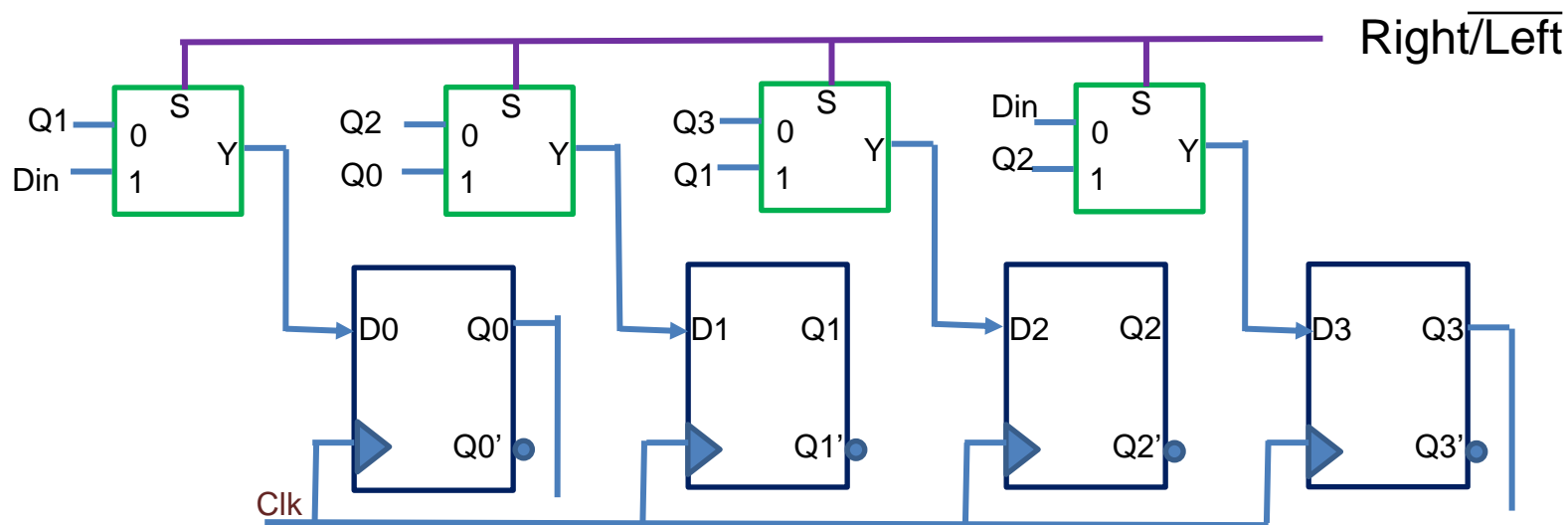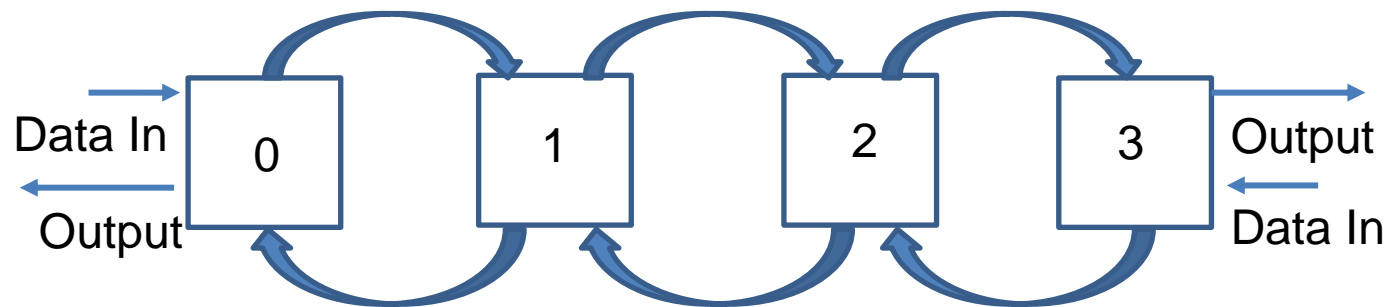
$Right/\overline{Left}$ = 0, Leftwards movement gets activated.

$Right/\overline{Left}$ = 1, Rightwards movement gets activated.

Shift Register Counters

A shift register counter is basically a shift register with the serial output connected back to the serial input to produce special sequence. These devices are often classified as counters because they exhibit a specified sequence of states.

The Johnson Counter

In a Johnson counter, the complement of the output of the last flip-flop is connected back to the D input of the first flip-flop. This feedback arrangement produces a characteristic sequence of states. Note that a 4-bit sequence has a total of 8 states and a 5-bit sequence has a total of 10 states. In general, a **Johnson counter will produce a modulus of 2n**, where n is the number of stages in the counter.

Four Bit Johnson Counter:

Four-bit Johnson sequence.

CLOCK PULSE	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
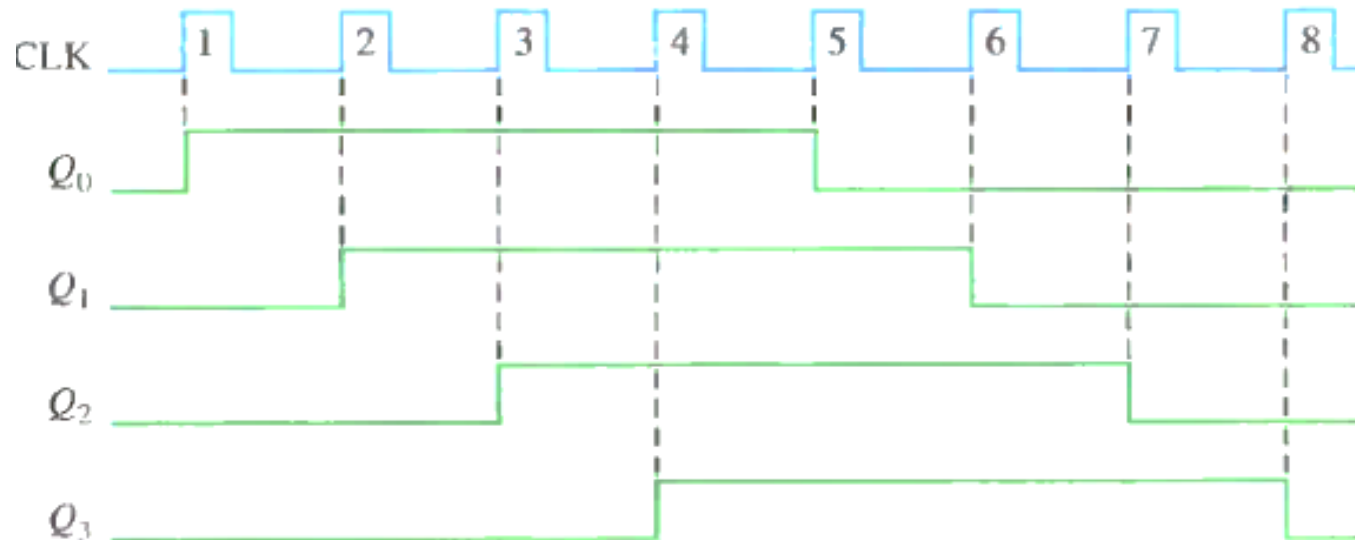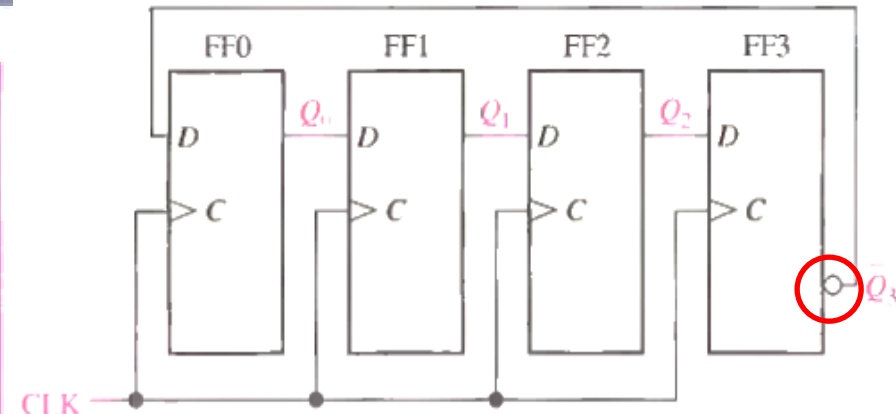
Five Bit Johnson Counter:

Five-bit Johnson sequence.

CLOCK PULSE	Q_0	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

Five-bit Johnson counter.
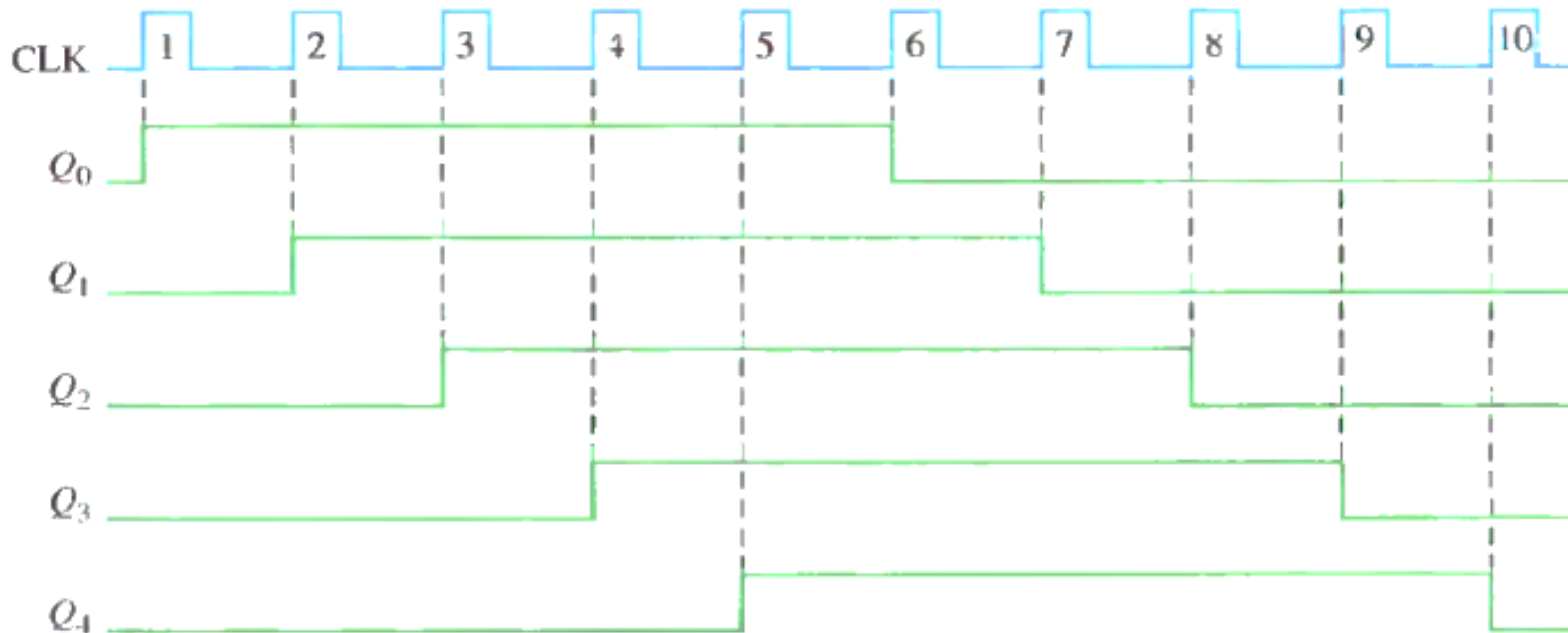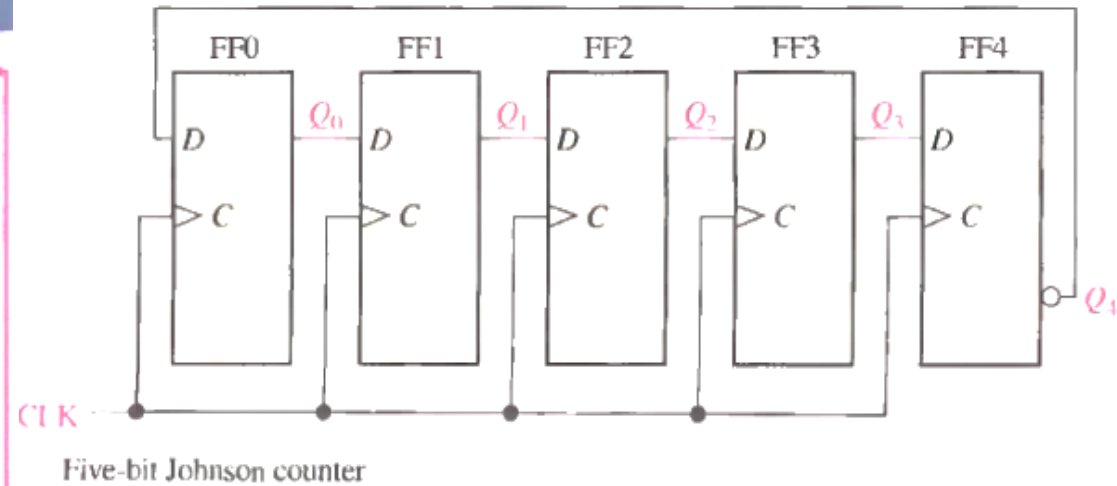
The Ring Counter

The Ring Counter utilizes one flip-flop for each state in its sequence. It has the advantage that decoding gates are not required. In the case of a 10 bit ring counter, there is an unique output for each decimal digit.
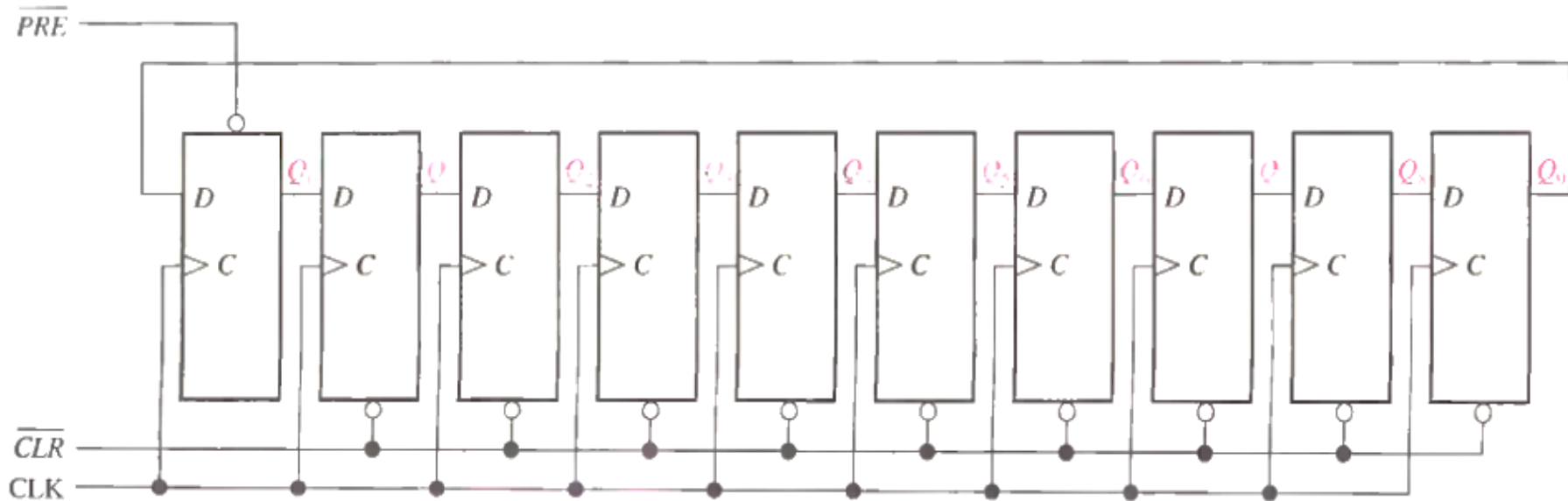
10 Bit Ring Counter Sequence

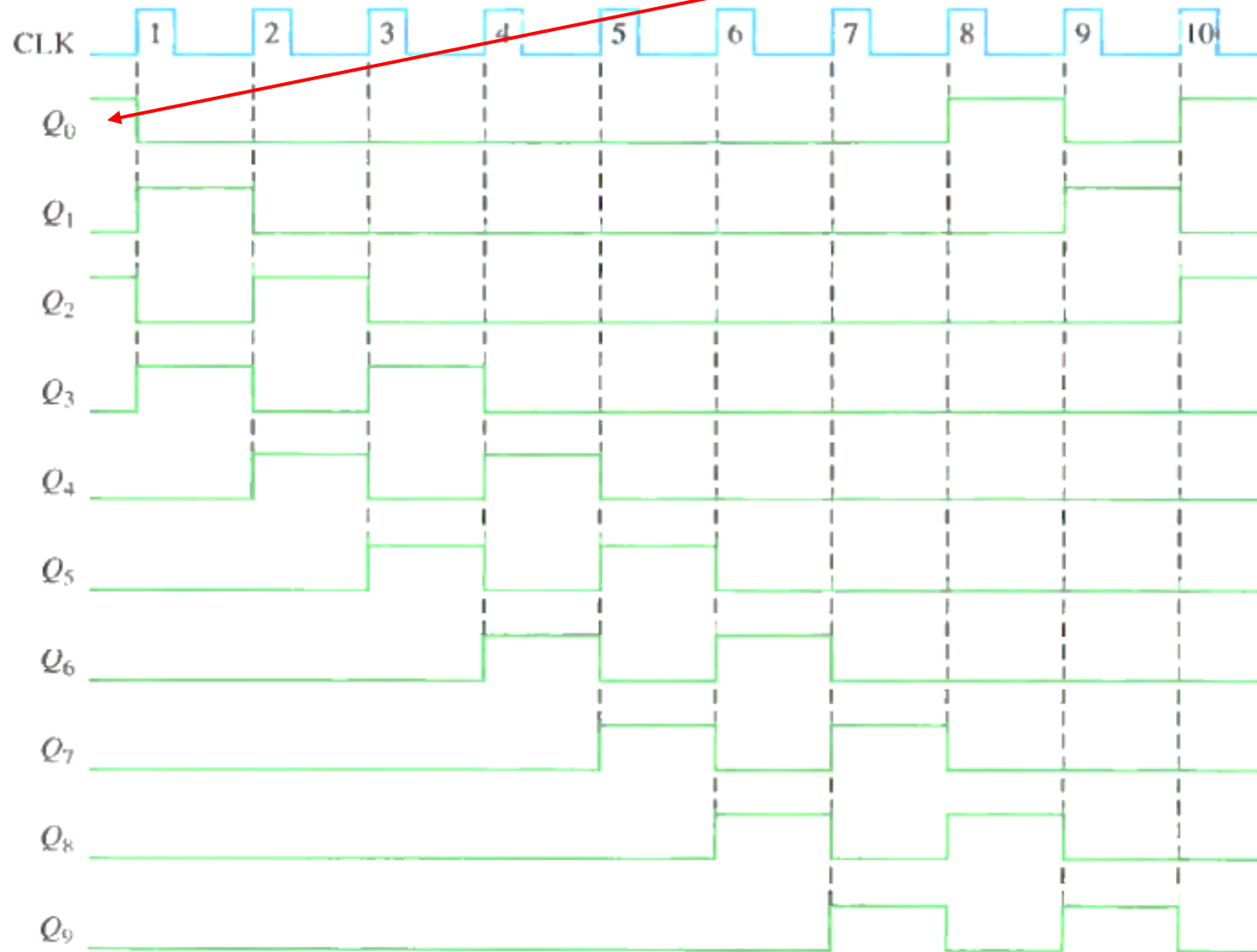| CLOCK PULSE	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0
3	0	0	0	1	0	0	0	0	0	0
4	0	0	0	0	1	0	0	0	0	0
5	0	0	0	0	0	1	0	0	0	0
6	0	0	0	0	0	0	1	0	0	0
7	0	0	0	0	0	0	0	1	0	0
8	0	0	0	0	0	0	0	0	1	0
9	0	0	0	0	0	0	0	0	0	1

If a 10 Bit Ring counter has an initial state of 1010000000, determine the waveform for each of the Q outputs

Reference:

[1] Thomas L. Floyd, "Digital Fundamentals" 11th edition, Prentice Hall.
[2] M. Morris Mano, "Digital Logic & Computer Design" Prentice Hall.
[3] Mixed contents from Vahid And Howard.

Thanks