EEE 3101: Digital Logic and Circuits

Digital Signal Processing

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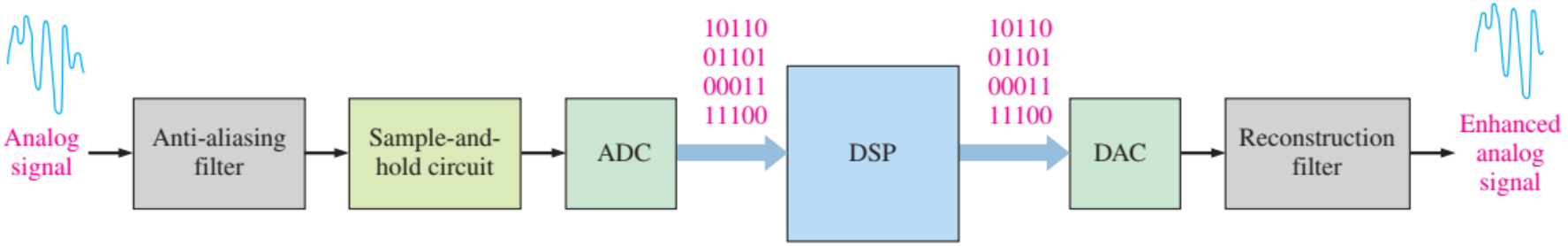
Introduction

- Digital Signal Processing coverts signals that naturally occur in analog form, such as sound, video and information from sensors, etc. to digital form and uses digital techniques to enhance and modify analog signal data for various applications.



- First the analog signal is passed through the Anti-aliasing filter (low pass filter) to eliminate harmonic frequencies above a certain specified frequency determined by the Nyquist frequency.
- Then the sampling and hold circuit performs two operation, the first of which is sampling. Sampling is the process of taking a sufficient number of discrete values at points on a waveform that will define the shape of the waveform.
- An analog signal can constitute signals of various frequencies. **Sampling Theorem** states that, in order to represent an analog signal, the sampling frequency , $\mathbf{f_{sample}}$, must be at least twice the highest frequency component $\mathbf{f_{a(max)}}$ of the analog signal. The frequency $\mathbf{f_{a(max)}}$ is known as the **Nyquist frequency** and is expressed in

$$\mathbf{f\_sample \geq 2f_{a(max)}}$$

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Sampling and Filtering

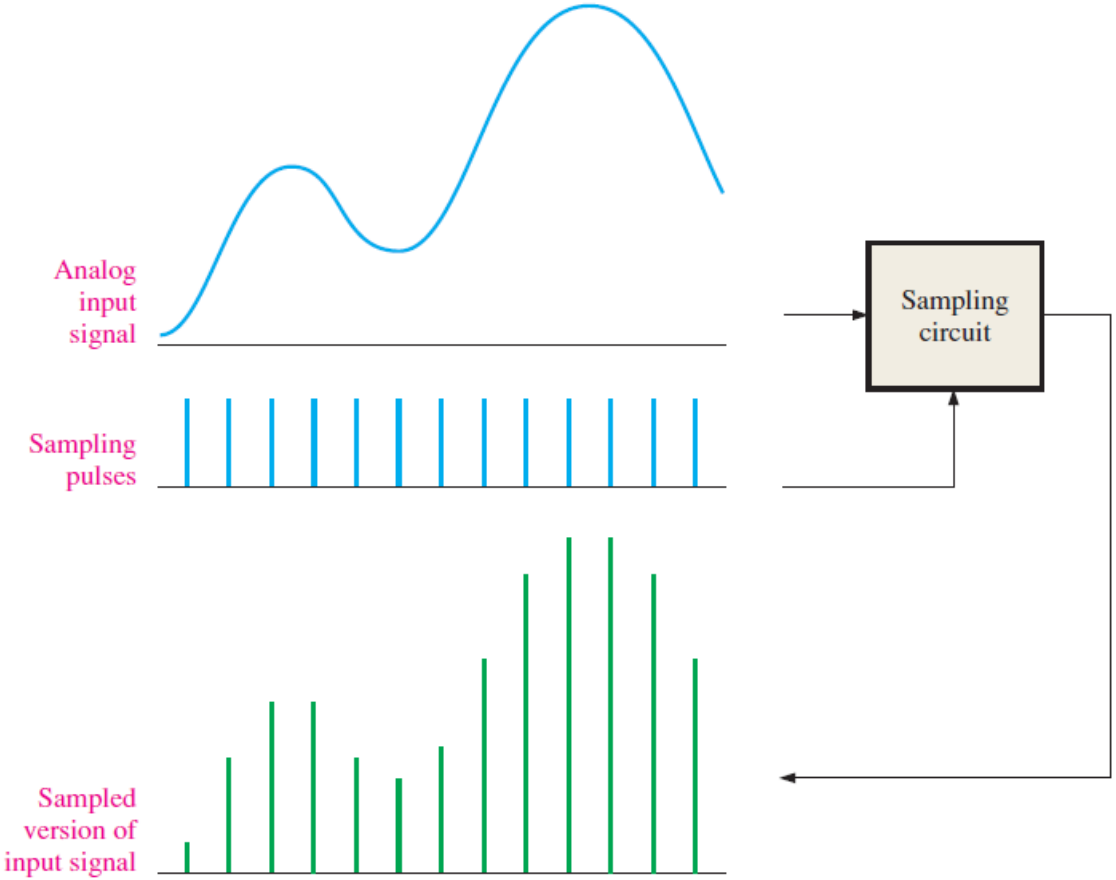

Illustration of sampling process

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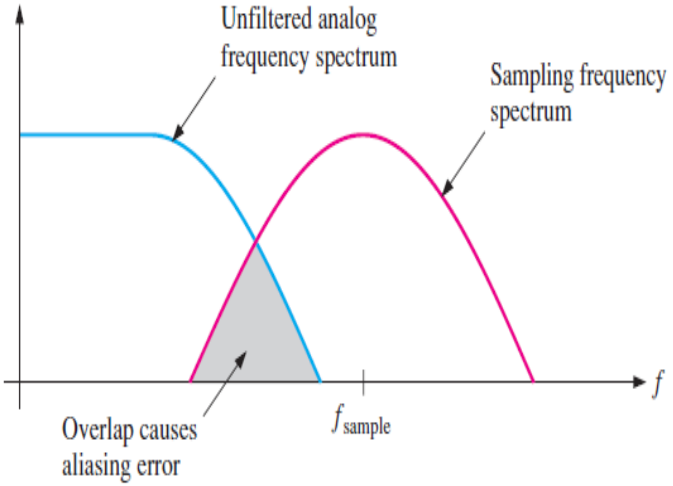
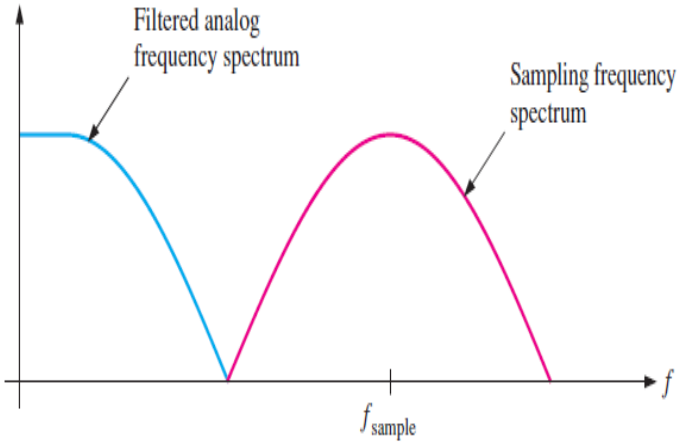
Sampling and Filtering

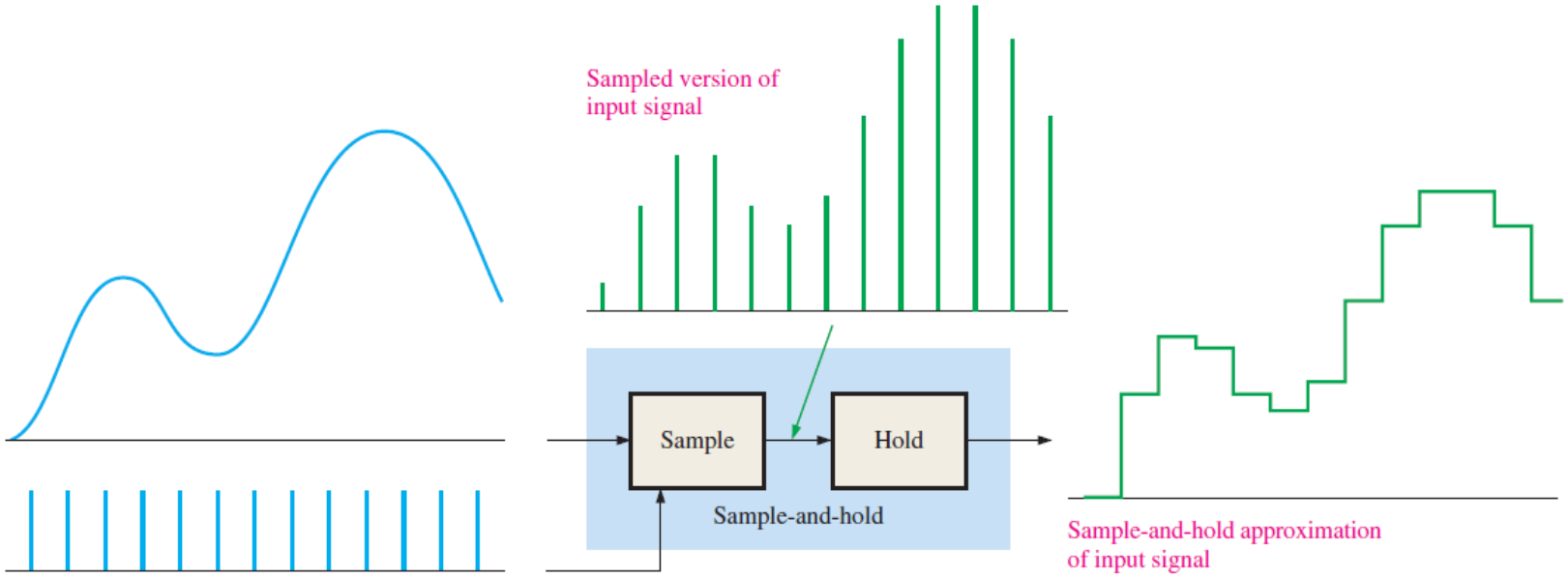
- The reason we need a low pass filter, is to remove all frequency components (harmonics) of the analog signal that exceed the Nyquist frequency.
- If there are any frequency component in the analog signal that exceed the Nyquist frequency, an unwanted condition know as aliasing will occur. An alias is a signal produced when the sampling frequency is not at least twice the signal frequency.
- An alias signal has a frequency that is less than the highest frequency in the analog signal being sampled and therefor falls within the spectrum or frequency band of the input analog signal causing distortion. Such a signal is actually "posing" as the part of the analog signal when its isn't, thus the term alias.





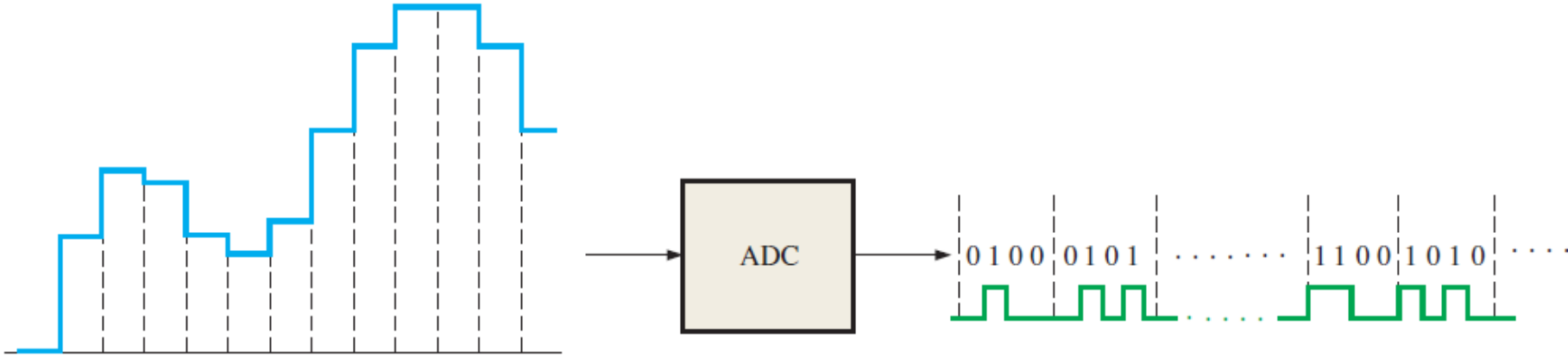
Hold Operation

- The holding operation is part of the sample and hold block shown in figure. After filtering and sampling, the sampled level must be held constant until the next sample occurs.
- This is necessary for the ADC to have time to process the sampled value. This sample and hold operation results in a "stairstep" wave form that approximate the analog input waveform.



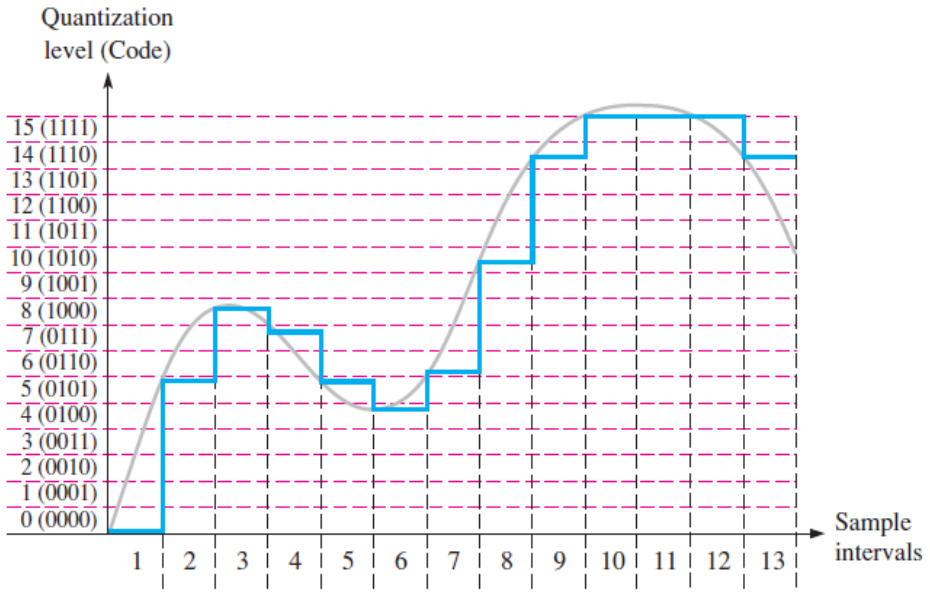
Analog to Digital Conversion

- Analog to digital conversion is the process of converting the output of the sample and hold circuit to a series of binary codes that represent the amplitude of the input at each of the sample times.
- The sample and hold process keeps the amplitude of the analog input signal constant between sample pulses.
- Therefore, the analog to digital conversion can be done using a constant value rather than having the analog signal change during conversion interval, which is the time between the sample pulses.



Quantization

- The process of converting an analog value to a code is called quantization.
- During quantization process, the ADC converts each sampled value of analog signal to a binary code.
- The more bits that are used to represent a sampled value, the more accurate is the representation.



Sample Interval	Quantization Level	Code
1	0	0000
2	5	0101
3	8	1000
4	7	0111
5	5	0101
6	4	0100
7	6	0110
8	10	1010
9	14	1110
10	15	1111
11	15	1111
12	15	1111
13	14	1110

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Quantization

For n-bit quantization:

- No. of quantization steps: $\mathbf{2^n}$
- Full-Scale Input Voltage Range, FSR: $\mathbf{V_{i(max)} - V_{i(min)}}$
- Resolution (Step-Size): $\frac{\mathbf{FSR}}{\mathbf{2^n}}$
- Digital Code, D: $\frac{\mathbf{Input\ Voltage - V_{i(min)}}}{\mathbf{Resolution}}$

Example Problem: An 8-bit ADC is capable of accepting an input voltage of range 0 to 10V. Find:

a) The Resolution
b) Digital output code for an input 5.2V.

Flash Analog to Digital Converter

- The flash method utilizes comparators that compare reference voltages with analog input voltages.
- When the input voltage exceeds the reference voltage for a given comparator, a HIGH is generated.
- A 3-bit converter uses seven comparator circuits; a comparator is not needed for all 0's condition. In general $2^n - 1$ comparators are required for conversion to an n-bit binary code.
- The number of bits used in an ADC is its resolution.
- The large number of comparators necessary for a reasonable-sized binary number is one of the disadvantage of the flash ADC.
- Its chief advantage is that it provides a fast conversion time because of a high throughput, measured in samples per second (sps)

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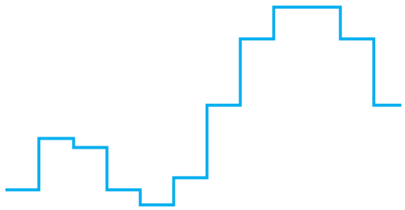
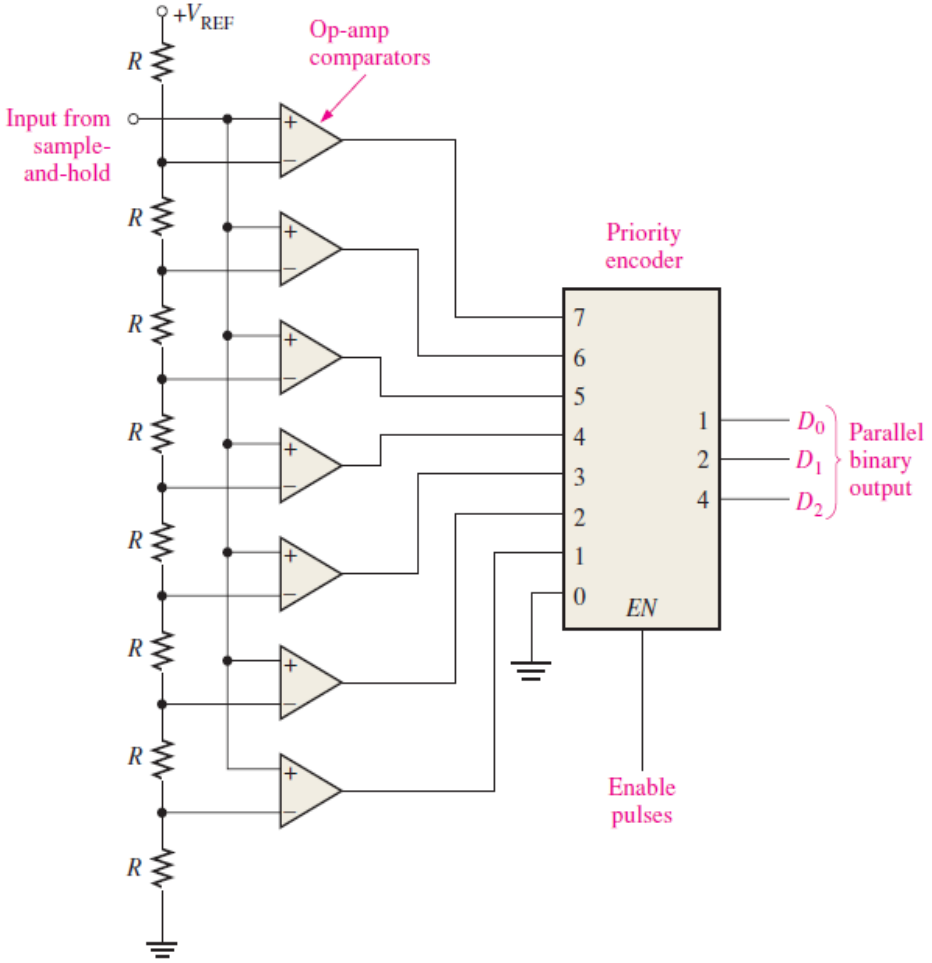
Flash Analog to Digital Converter





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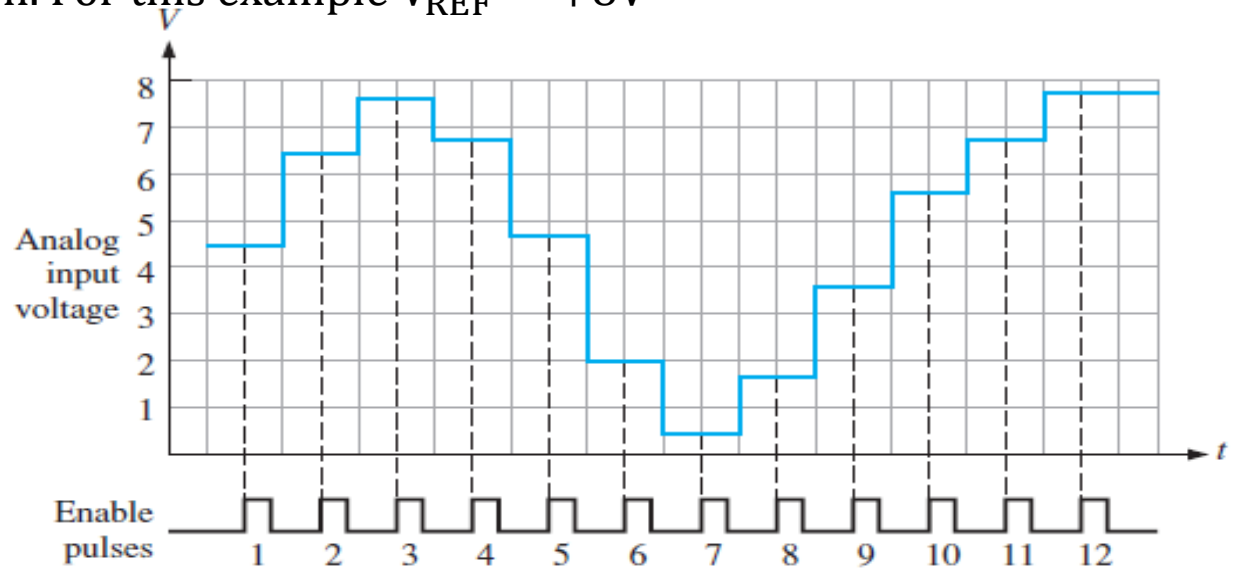
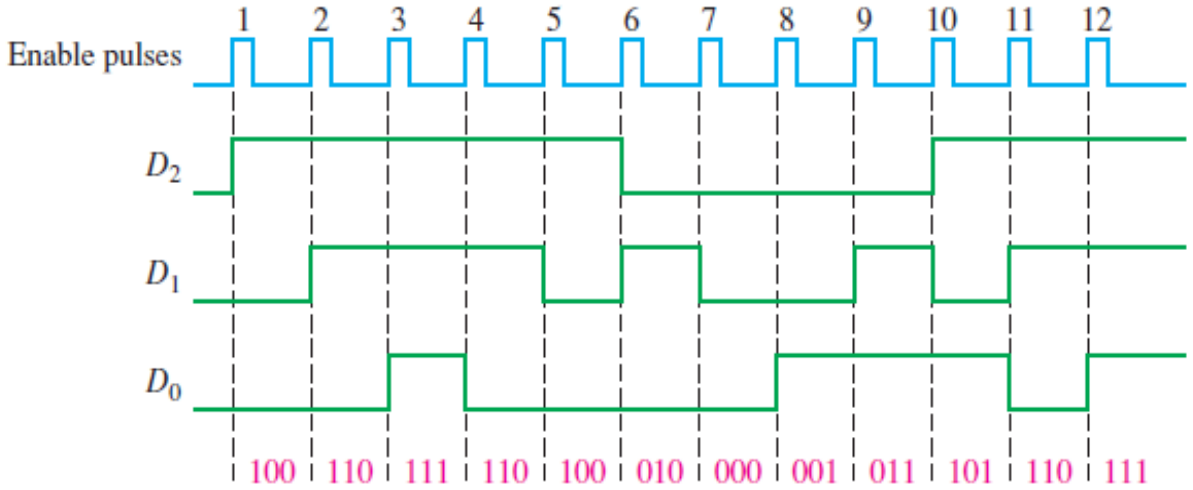
Flash Analog to Digital Converter

Determine the binary code output of a 3-bit ADC for the input signal and encoder enable pulses shown. For this example $V_{REF} = +8V$

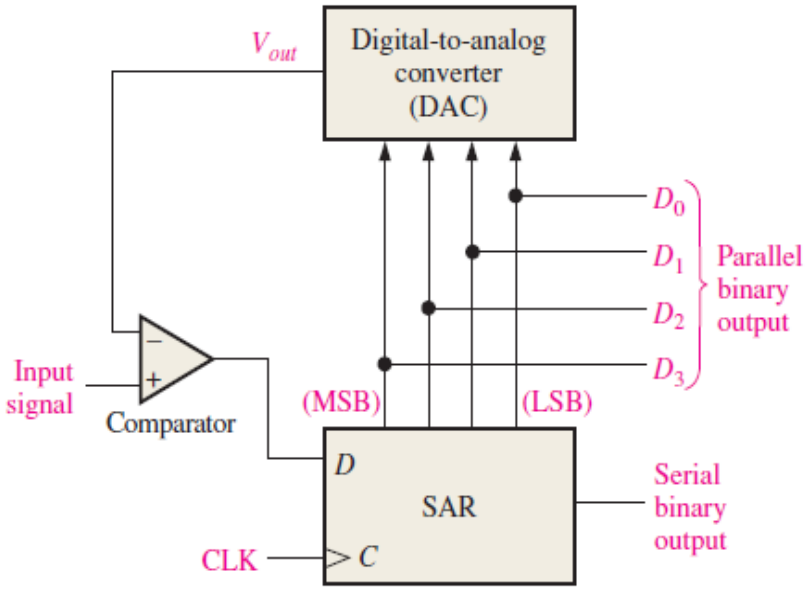


SOLUTION



Successive-Approximation Analog to Digital Converter

- Successive-Approximation is the most widely used ADC method.
- It is faster than a dual-slope converter.
- However, it is slower than a Flash ADC.
- It has a fixed conversion time for any value of analog input.
- An n-bit converter takes n cycles or steps to converts any analog input.



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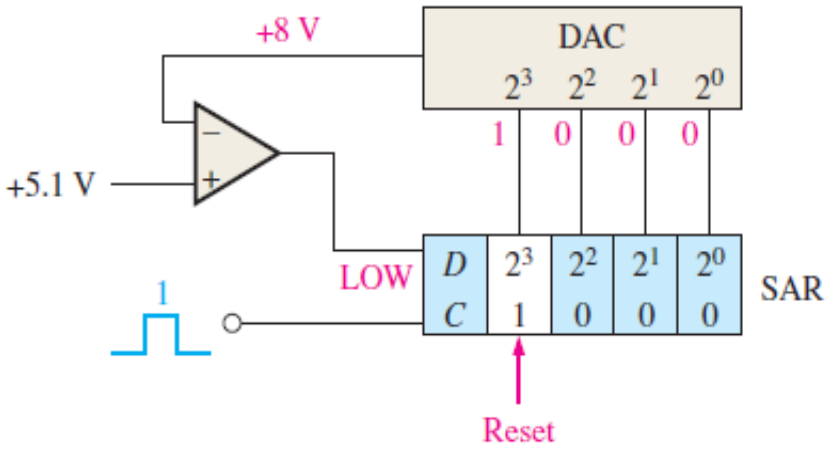
Successive-Approximation Analog to Digital Converter

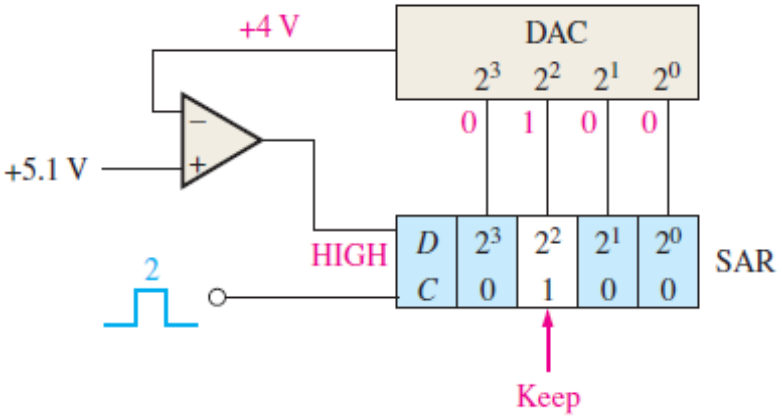
- The DAC outputs 8V for 2^3 bit, 4V for 2^2 bit, 2V for 2^1 bit and 1V for 2^0 bit.
- Now as an example we try to convert an input voltage of 5.1V

At the first pulse, the MSB is turned HIGH. As 8V is greater than 5.1V, it is therefore reset.

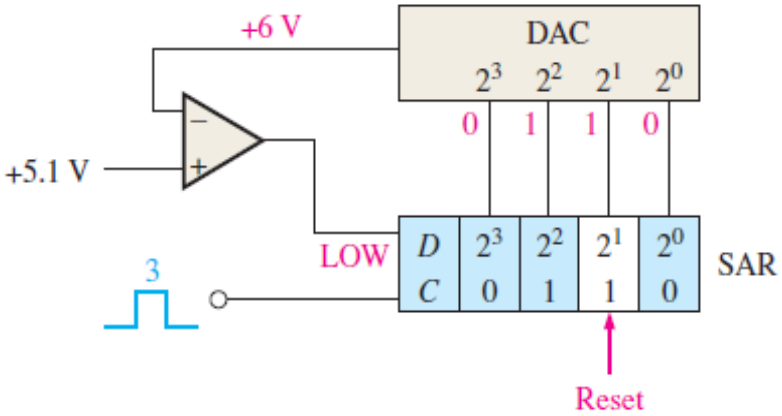


Successive-Approximation Analog to Digital Converter

Then the next bit is turned HIGH. The corresponding output is 4V. As it is less than 5.1V, the bit is kept as HIGH.

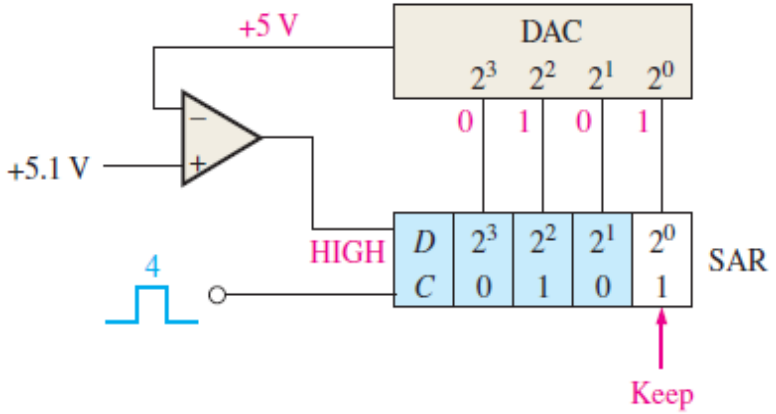


Then the next bit is turned HIGH, the corresponding output now is 6V. As 6V is greater than 5.1V, the bit is RESET.



Successive-Approximation Analog to Digital Converter

Now, finally the last bit is turned HIGH. The corresponding output is 5V. As this is less than the input 5.1V, the last bit is retained as 1.



So after 4 cycles all the bit has been tried. Therefore, the digital code corresponding to 5.1V is 0101, which is 5V. If the no. of bit is increased the resolution of ADC will increase and thus will produce a more accurate approximation.

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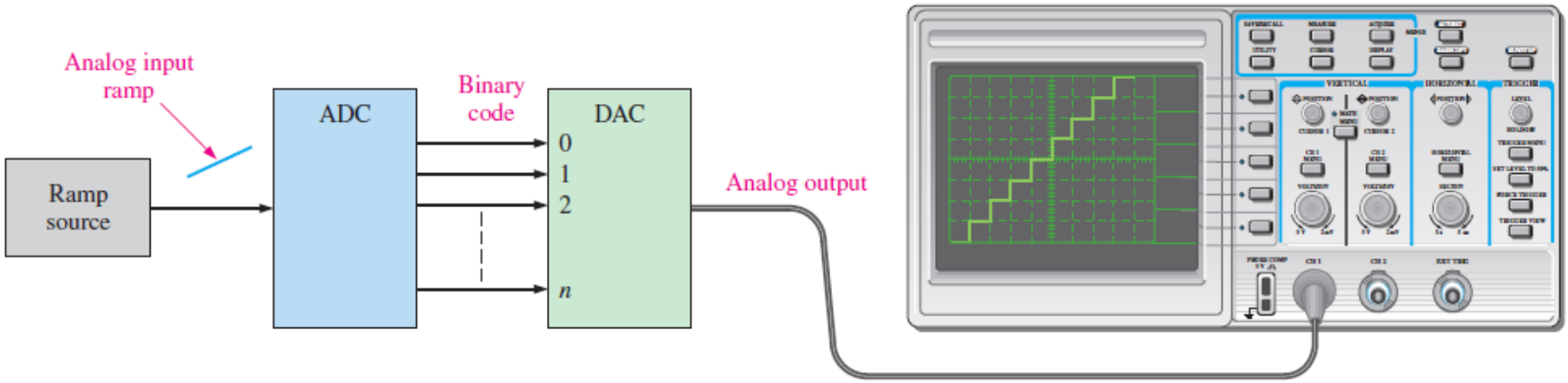
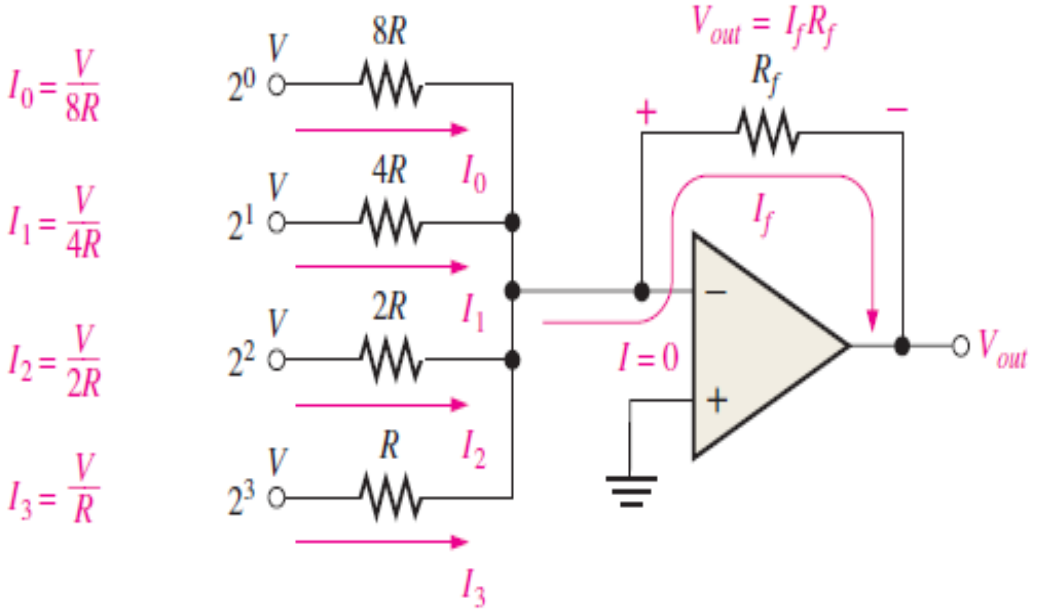
Introduction

- Digital to analog conversion is an important part of digital signal processing.
- Once the digital signal has been processed, it is further needed to be converted back to the analog form.
- A Digital to Analog Converter (DAC) is an electronic device, often an integrated circuit, which converts a digital signal to its corresponding analog signal.
- Two types of DAC will be studied:
  - Binary Weighted DAC
  - R-2R Ladder DAC



Binary Weighted DAC

- The figure shows a 4-bit DAC.
- The resistors have a specific value depending on the binary weights.
- The resistor corresponding to MSB have the lowest value
- The resistor corresponding to LSB have the highest value.
- The output depends on the presence or absence of current in the branches.



$$\mathbf{I_f = I_0 + I_1 + I_2 + I_3}$$

$$\frac{\mathbf{V_0}}{\mathbf{R_f}} = \frac{\mathbf{V}}{\mathbf{8R}} + \frac{\mathbf{V}}{\mathbf{4R}} + \frac{\mathbf{V}}{\mathbf{2R}} + \frac{\mathbf{V}}{\mathbf{R}}$$

$$\textbf{Now if } \mathbf{R_f = R}$$

$$\mathbf{V_0} = \frac{\mathbf{V}}{\mathbf{8}} + \frac{\mathbf{V}}{\mathbf{4}} + \frac{\mathbf{V}}{\mathbf{2}} + \frac{\mathbf{V}}{\mathbf{1}}$$

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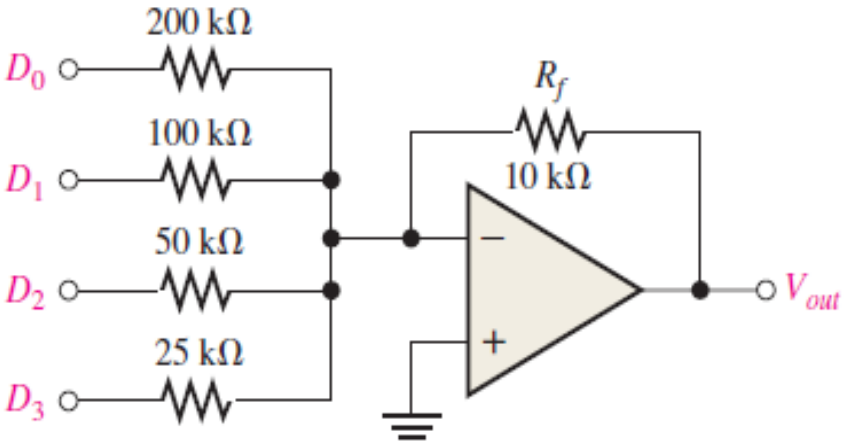
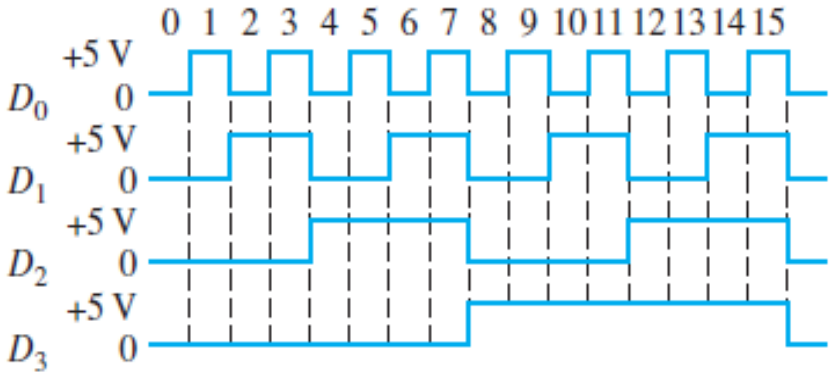
Binary Weighted DAC

Determine the output of the DAC if the waveform representing a sequence of 4-bit numbers are applied to the inputs. Input D_0 is the least significant bit(LSB)





Binary Weighted DAC

- First we need to determine the current for each of the weighted inputs.

$$I_0 = \frac{5V}{200k} = 0.0025mA$$
$$I_1 = \frac{5V}{100k} = 0.05mA$$
$$I_2 = \frac{5V}{50K} = 0.1mA$$
$$I_3 = \frac{5V}{25K} = 0.2mA$$

- Now we will calculate the output contribution for each of the weighted inputs. Since no current goes through the inverting input, the current only flows through the feedback path.

$$V_{O(D0)} = (10k)(-0.025mA) = -.25V$$
$$V_{O(D1)} = (10k)(-0.05mA) = -0.5V$$
$$V_{O(D2)} = (10k)(-0.1mA) = -1V$$
$$V_{O(D3)} = (10k)(-0.2mA) = -2V$$

From Figure 12–27(b), the first binary input code is 0000, which produces an output voltage of 0 V. The next input code is 0001, which produces an output voltage of −0.25 V. The next code is 0010, which produces an output voltage of −0.5 V. The next code is 0011, which produces an output voltage of −0.25 V + −0.5 V = −0.75 V. Each successive binary code increases the output voltage by −0.25 V, so for this particular straight binary sequence on the inputs, the output is a stairstep waveform going from 0 V to −3.75 V in −0.25 V steps. This is shown in Figure 12–28.

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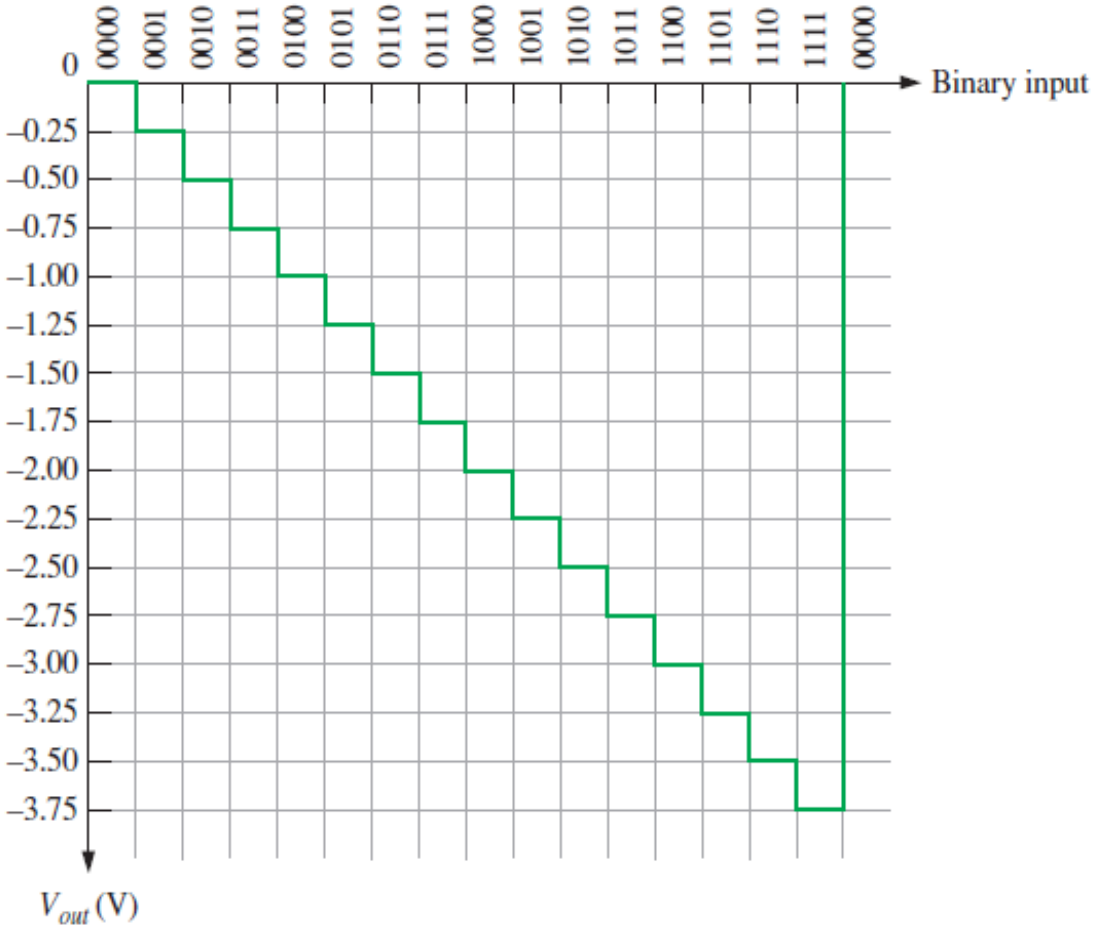
Binary Weighted DAC



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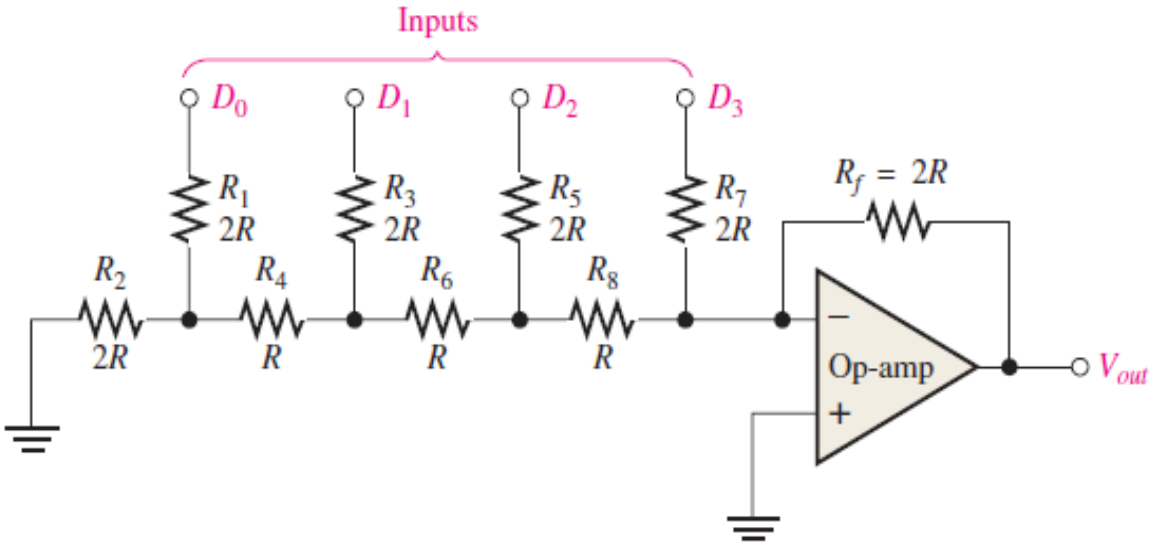
R-2R Ladder DAC

- Though binary-weighted DAC is simple to understand, construction of it is hectic.
- For binary-weighted DAC we need exact multiples of the resistors (R, 2R, 4R, 8R, 16R).
- For DAC of higher bits, the construction becomes practically infeasible.
- However, R-2R DAC solves this problem.
- The construction only require resistors of value R and 2R



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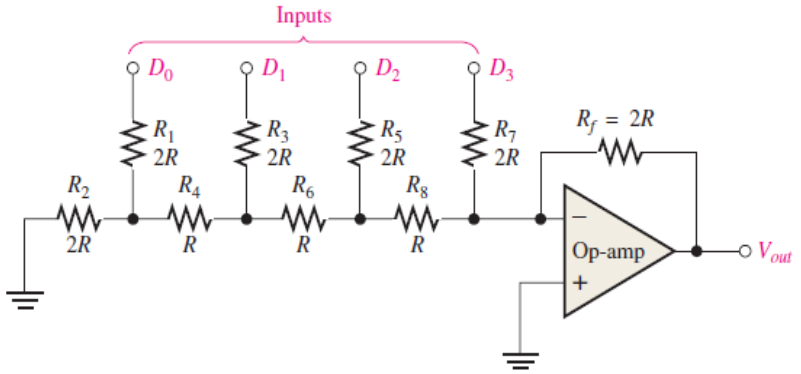
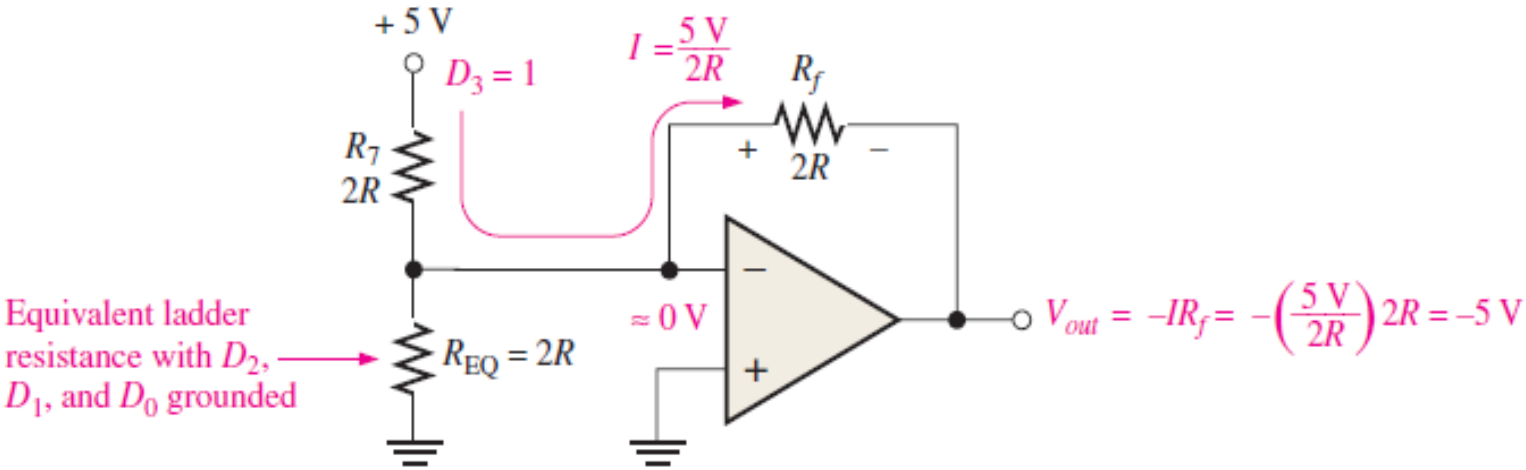
R-2R Ladder DAC

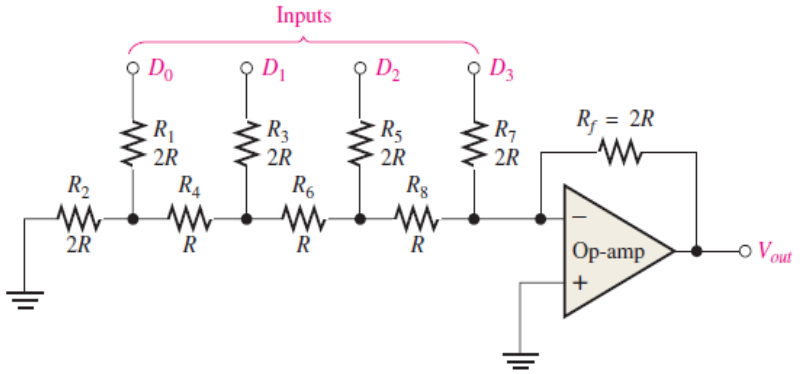
Contribution of D_3.

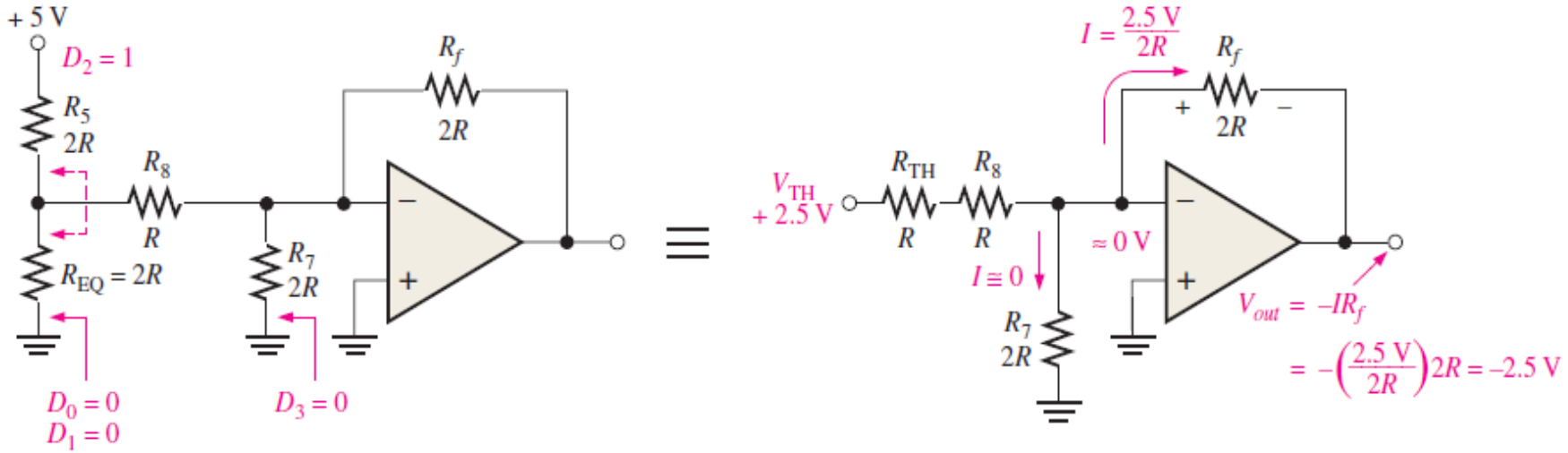




R-2R Ladder DAC

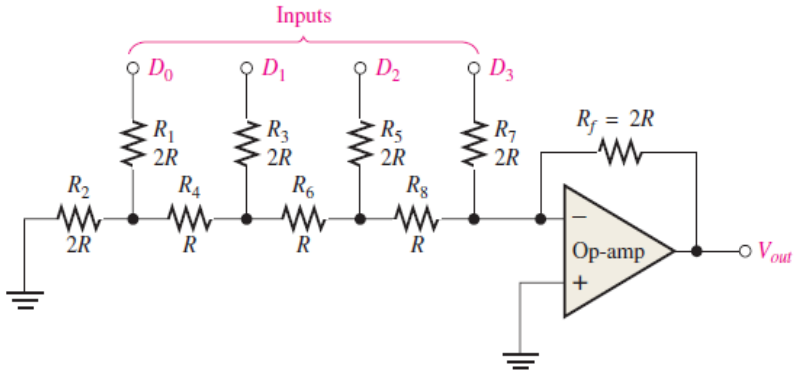
Contribution of D_2.

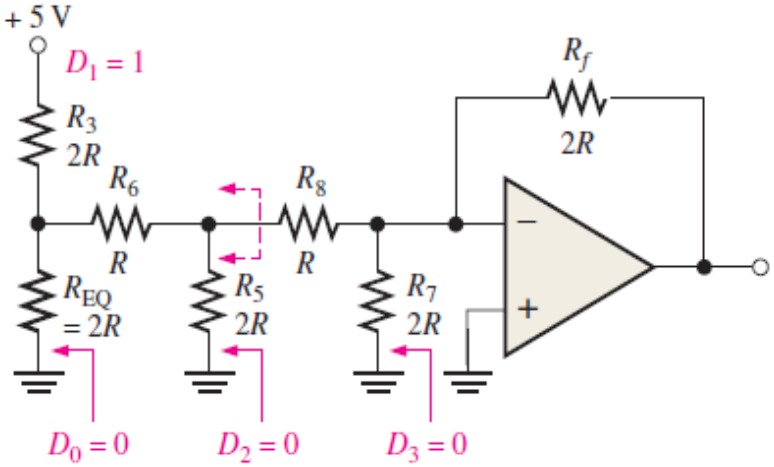




R-2R Ladder DAC

Contribution of D_1.





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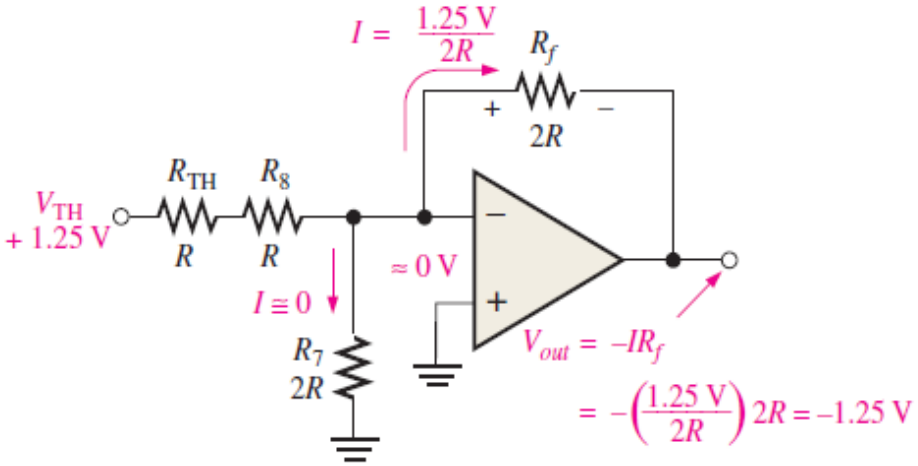
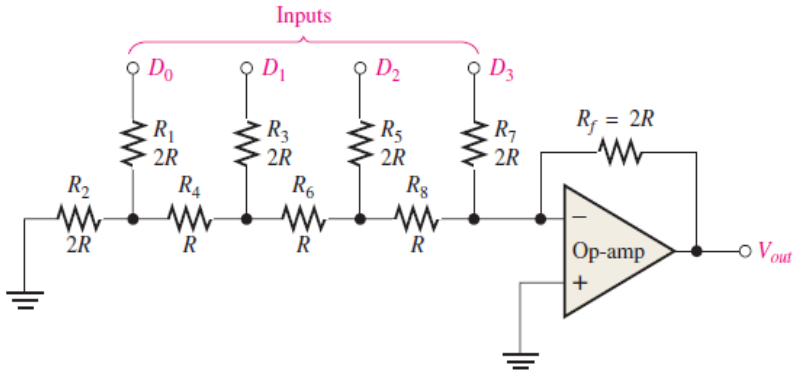
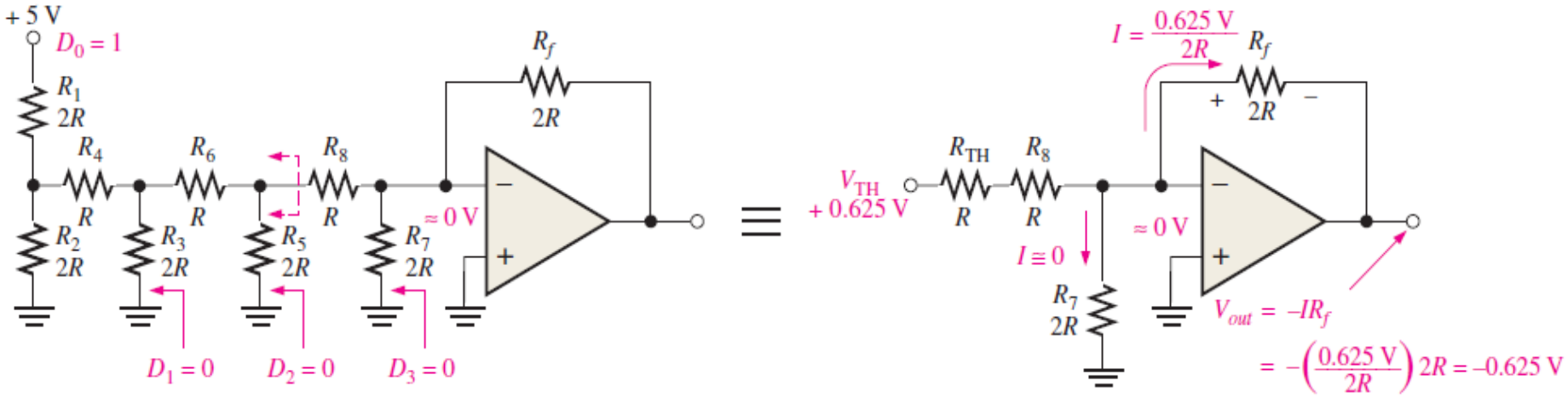


R-2R Ladder DAC

Contribution of D_0.





DAC

Resolution of a n-bit DAC:

$$\frac{1}{2^n - 1}$$

Determine the resolution expressed as a percentage of the following:

a) An 8-bit DAC
b) A 12-bit DAC

Solution:

a) Resolution for 8-bit converter,

$$\frac{1}{2^8 - 1} \times 100 = \frac{1}{255} \times 100 = 0.392\%$$

b) Resolution for 12-bit converter,

$$\frac{1}{2^{12} - 1} \times 100 = \frac{1}{4095} \times 100 = 0.0244\%$$

The Reconstruction Filter

The output of the DAC is a “stairstep” approximation of the original analog signal after it has been processed by the digital signal processor (DSP), which is a special type of microprocessor that processes data in real time. The purpose of the low-pass reconstruction filter (sometimes called a postfilter) is to smooth out the DAC output by eliminating the higher frequency content that results from the fast transitions of the “stairsteps,” as roughly illustrated in the figure below.

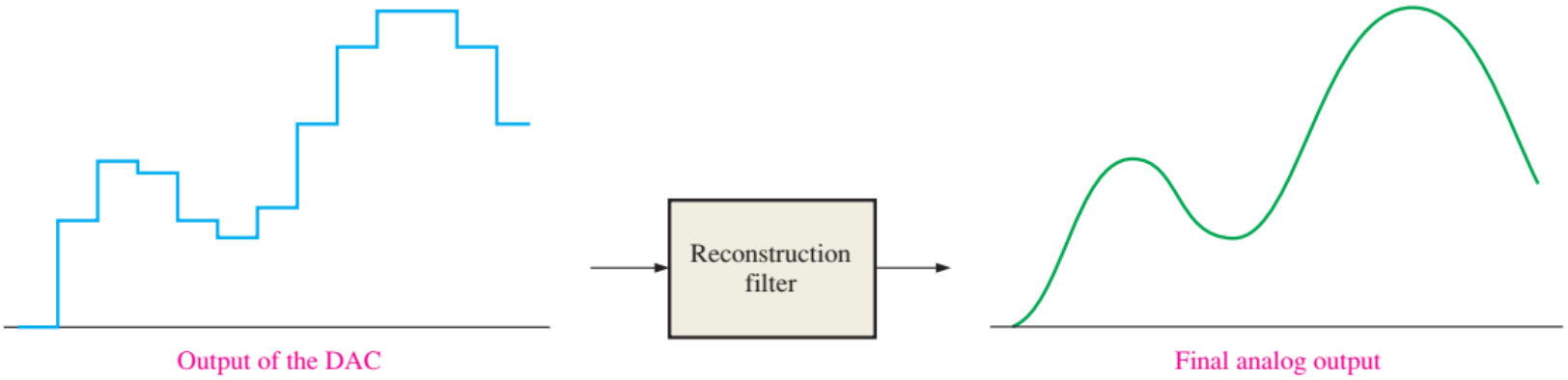


FIGURE : The reconstruction filter smooths the output of the DAC.

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Reference:

[1] Thomas L. Floyd, "Digital Fundamentals" 11th edition, Prentice Hall.
[2] M. Morris Mano, "Digital Logic & Computer Design" Prentice Hall.
[3] Mixed contents from Vahid And Howard.

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Thanks