
American International University - Bangladesh
Welcome to the first class of
EEE 3101: Digital Logic and Circuits
AIUB
EEE
FACULTY OF ENGINEERING

EEE 3101: Digital Logic and Circuits

Course Teacher: Nafiz Ahmed Chisty

Associate Professor, Department of EEE & CoE
Head (UG), Department of EEE
Faculty of Engineering
Room# D0105, D Building
Email: chisty@aiub.edu
Website: http://engg.aiub.edu/
Website: www.nachisty.com

Teaching and Consulting Schedule

Nafiz A. Chisty| Head (UG), Dept of EEE; Associate Professor, Dept. of EEE & CoE

AMERICAN INTERNATIONAL UNIVERSITY-BANGLADESH (AIUB)
Ka 66/a, Kuratuli Road, Kuril, Dhaka-1229, Bangladesh

TEACHER'S SCHEDULE FORM

Fall Semester, 2021-2022

Day	Sunday	Monday	Tuesday	Wednesday	Thursday
Starting Time	10:30	10:30	10:30	10:30	10:30
Ending Time	18:30	18:30	18:30	18:30	18:30
10:30-11:00	Consulting & Office Hours	Consulting & Office Hours	Consulting & Office Hours	Consulting & Office Hours	Consulting & Office Hours
11:00-12:30		Digital Logic and Circuits Section: D Room# 1116		Digital Logic and Circuits Section: D Room# 1116	
12:30-14:00	Digital Logic and Circuits Section: I Room# 1118	Digital Logic and Circuits Section: C Room# 1117	Digital Logic and Circuits Section: I Room# 1118	Digital Logic and Circuits Section: C Room# 1117	
14:00-15:30	Digital Logic and Circuits Section: B Room# 1119	Consulting & Office Hours	Digital Logic and Circuits Section: B Room# 1119	Consulting & Office Hours	
15:30-18:30	Consulting & Office Hours		Consulting & Office Hours		

Teacher's Name: Nafiz Ahmed Chisty

Designation: Associate Professor, Dept. of EEE & CoE
Head In-Charge (UG), Dept. of EEE

E-mail: chisty@aiub.edu

Consulting Hours:

Sunday	Monday	Tuesday	Wednesday	Thursday
10:30 - 12:30 15:30 - 18:30	10:30 - 11:00 14:00 - 18:30	10:30 - 12:30 15:30 - 18:30	10:30 - 11:00 14:00 - 18:30	10:30 - 18:30

Nafiz A. Chisty| Head (UG), Dept of EEE; Associate Professor, Dept. of EEE & CoE

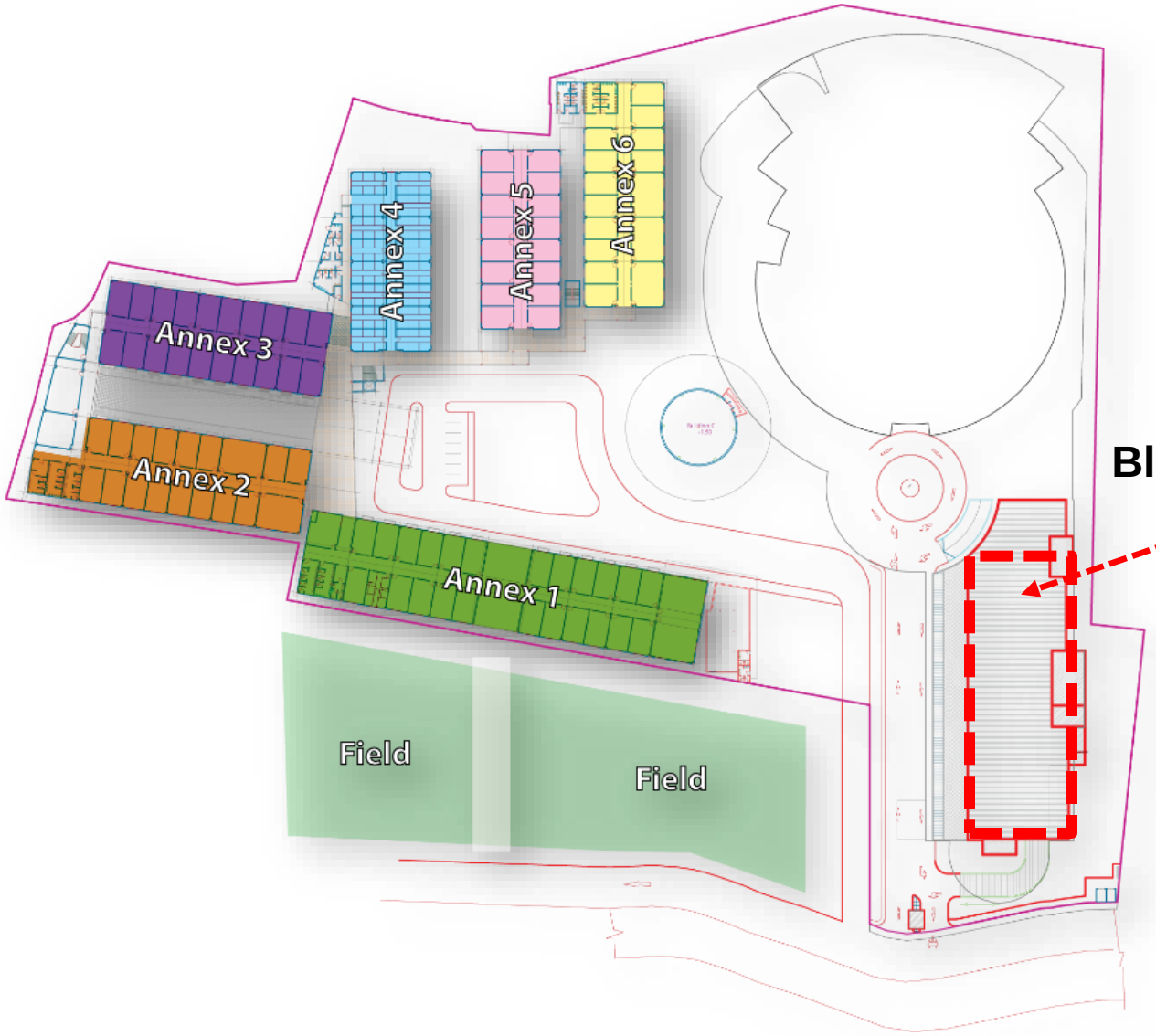
Academic Calendar

Fall 2021-2022

2021		
Sep	9 (Thursday)	New Teachers' orientation
	12	First Day of Classes (Regular and Masters' Freshman Classes)
	16	General Meeting
	16 & 19	Adding/ Dropping
	26	Automatic conversion of UW, I, blank grades of Summer 2020-21 Semester to F
Oct	16 – 21	Mid Semester Laboratory Assessment (Regular and Masters' Freshman Courses)
	23 – 28	Mid Semester Assessment (Regular and Masters' Freshman Courses)
Nov	4	Submission of mid semester grades (Regular and Masters' Freshman Classes)
	21 - 25	TPE
	25	Mid semester Grades Locked
	21 - 25	Pre-registration for Spring 2021-22
	27 – Dec 9	Final Laboratory Assessment
Dec	4 - 18	Final Assessment
	26	Submission of Final Grades
	Dec 19 – Jan 15, 2022	Semester break Release of grades Final Registration for Spring 2021-22
	Jan 8, 2022	Final Grades Locked
Jan	Jan 27, 2022	Automatic conversion of UW, I grades of this semester to F

Nafiz A. Chisty| Head (UG), Dept of EEE; Associate Professor, Dept. of EEE & CoE

Office



Bldg D, Ground Floor

AMERICAN INTERNATIONAL UNIVERSITY - BANGLADESH (AIUB)

Mission:

American International University-Bangladesh is committed to provide quality and excellent academic programs responsive to the emerging global challenges. The university is dedicated to produce and foster competent world class graduates imbued with strong sense of ethical values ready to face the competitive world of business, science, technology, engineering and social sciences.

Vision:

American International University-Bangladesh continuously transform the students to become innovative and globally competitive with excellent, state-of-the-art and academic knowledge and skills nurturing their full potentials not only as future leaders in their respective fields of endeavor, but also as unique contributors to the society.

Nafiz A. Chisty| Head (UG), Dept of EEE; Associate Professor, Dept. of EEE & CoE

Nafiz A. Chisty| Head (UG), Dept of EEE; Associate Professor, Dept. of EEE & CoE

FE Mission

- Develop engineers with highest level of commitment toward the betterment of the society by applying knowledge of science and engineering
- Nurture young leaders with evolving perspectives and ethics
- Create and disseminate knowledge and skills using modern tools

FE Vision

The **Faculty of Engineering** will endeavor to nurture students for creativity and innovation dedicated to problem solving and lifelong learning for research, entrepreneurship, and professionalism

EEE Mission

- **M1** **Educate** young leaders for academia, industry, entrepreneurship and public and private organization through theory and practical knowledge to solve engineering problems individually and in teams.
- **M2** **Create** knowledge through innovative research and collaboration with multiple disciplines and societies.
- **M3** **Serve** the communities at national, regional and global levels with ethical and professional responsibilities.

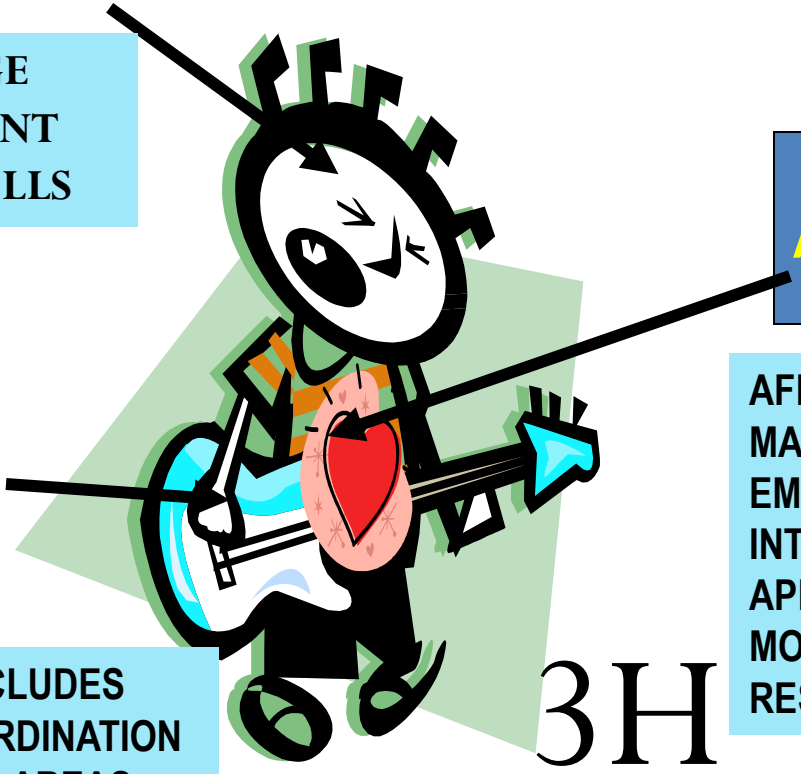
EEE Vision

- To become a front runner in preparing electrical and electronics engineering graduates to be nationally and globally competitive and there by contribute value for the knowledge-based economy and welfare for the people of the world.

The 3 Domains of Educational Goals

Cognitive
The Head

INVOLVES KNOWLEDGE AND THE DEVELOPMENT OF INTELLECTUAL SKILLS



Affective
The Heart

AFFECTIVE DOMAIN – INCLUDES MANNER WE DEAL WITH THINGS EMOTIONALLY (e.g. FEELINGS, INTERESTS, ATTITUDES, APPRECIATION, ENTHUSIASMS, MOTIVATIONS) - THAT MIGHT RESULT FROM INSTRUCTION)

Psychomotor
The Hand

PSYCHOMOTOR DOMAIN INCLUDES PHYSICAL MOVEMENT, COORDINATION & USE OF THE MOTOR SKILL AREAS

3H

Nafiz A. Chisty| Head (UG), Dept of EEE; Associate Professor, Dept. of EEE & CoE

Different Levels of Learning Outcomes

Program Educational Objectives (PEO)

Few years after Graduation – 3 to 5 years

Employer Survey, Alumni Survey

Competent engineers who are leaders in …..

↓

Program Outcomes (PO)

Upon graduation - Twelve (12) BAETE Program Outcomes

CO, Exit Survey, Prog.Survey

..will be able to demonstrate critical thinking skills to solve

↓

Course Outcomes (CO)

Upon course completion Use Bloom's Taxonomy of Learning Domains (C/A/P)

Sum/Form/Cont. Assessments

.. will be able to explain the physical principles of ……

↓

Weekly/Topic Outcomes

Upon topic completion Use Bloom's Taxonomy of Learning Domains (C/A/P)

Sum/Form/Cont. Assessments

.. will be able to explain Archimedes principle of ……

Adapted from Shahrin Mohamed, 2007

Nafiz A. Chisty| Head (UG), Dept of EEE; Associate Professor, Dept. of EEE & CoE

Program Educational Objectives (PEO)

EEE Graduates are expected, within a few years of graduation, to have demonstrated:	
PEO-1	Exhibit essential engineering knowledge in Electrical, Electronic, and other related fields through a career as a professional, academic, or entrepreneur.
PEO-2	Achieve leading roles in respective organizations and communities through teamwork, professional ethics, and effective communication.
PEO-3	Demonstrate lifelong learning through professional development, practical training, professional certification, and membership or pursuing higher studies.

12 Program Outcomes (PO)

a) Engineering knowledge
b) Problem analysis
c) Design/ Development of Solutions
d) Investigation
e) Modern tool usage
f) Engineer and society
g) Environment and sustainability
h) Ethics
i) Individual work and team work
j) Communication
k) Project management & finance
l) Life-long learning

Nafiz A. Chisty| Head (UG), Dept of EEE; Associate Professor, Dept. of EEE & CoE

COURSE OUTLINE

I. Course Core and Title: EEE 3101: Digital Logic and Circuits
II. Credit: 3 credit hours (3 hours of theory per week)
III. Nature: Core Course for EEE
IV. Prerequisite: EEE 2103: Electronic Devices

Objectives:

The objectives of the course can be grouped into two categories. The first one relates to understanding the basics of Boolean algebra and the operation of logic components, combinational, and sequential circuits.
The second set of objectives relates to the design of digital circuits and systems.

Course Description:

This is core course of Electrical and Electronic Engineering & Computer Engineering program that presents basic tools for the design of digital circuits. It serves as a building block in many disciplines that utilize data of digital nature like digital control, data communication, digital computers etc.

This course is designed to:
Manipulate Boolean algebraic structures, Implement the Boolean Functions using NAND and NOR gates, Simplify the Boolean expressions using Karnaugh Map, Analyze and design various combinational logic circuits, Study of Storage Elements: Introduction to the behavior and structure of latches, flip-flops, and registers, Understand the importance of state diagram representation of sequential circuits, Study Sequential Circuits: Analyze and design clocked sequential circuits, Perform Timing Analysis: Introduction to timing analysis of combinational and sequential circuits. Special characteristics of Digital logic families and their comparative discussion. Definition and Problem solving on Fan out, Noise Margin, Propagation Delay, Power Dissipation, Duty Cycle and Speed Power Product. Diode Logic Gates. Basic Diode Transistor Logic Gates: RTL, DTL, Modified DTL and HTL with operational detail.

MOS and CMOS Logic with operational detail. Basic memory units and operations. Memory system: RAM Family. Memory System: ROM Family. Memory System: Flash Memory, Magnetic storage, USB Flash Drive, SSD hard drive. DSP basics: Sample and Hold circuits. Digital to Analog Conversion with application. Analog to Digital Conversion with application. Operation and Mathematical operation of 555 integrated timer circuit: Monostable, Astable multi-vibrator. Charge Coupled Device (CCD)and LCD. Introduction to Programmable Logic Devices (PLDs): Advantages & disadvantages over discrete logic gates, Implementation of digital circuits using PLDs (using PAL and PLA).

Nafiz A. Chisty| Head (UG), Dept of EEE; Associate Professor, Dept. of EEE & CoE

Topics to be covered*:

Week	Topics
1	• Mission & Vision of AIUB, Dept. of EEE; Objective of DLD course. • Introduction to Integrated Circuit (IC). • Special Characteristics of digital logic families. • Binary Logic, Logic gates and their truth table. • Logic Gates using: DL, RTL, DTL, HTL, MOS and CMOS • Logic family mathematical problems
2	• Boolean algebra, Simplification using Boolean Algebra. • Implementing circuit from Boolean expressions • De-Morgan's law. • Universal gates and their applications.
3	• Canonical forms-maxterms and minterms. Sum of Product (SOP) and Product of Sum (POS) form. • Boolean expression in Simplifying using K – map.
4	• Adders and Subtractors. • Magnitude Comparators.
5	• Decoders, • Encoders, Priority Encoders, • Cascading of Decoders, Encoders
6	• Multiplexers, De-Multiplexer • Boolean Function implementation using Multiplexers, • Cascading of Multiplexers, De-Multiplexers
7	**MID-TERM WEEK**

* The faculty reserves the right to change, amend, add or delete any of the contents.

Nafiz A. Chisty| Head (UG), Dept of EEE; Associate Professor, Dept. of EEE & CoE

Week	Topics
8	• Sequential Logic circuit: Latches, Flip – flops • Timing Diagram.
9	• Counters: Asynchronous and Synchronous counters. • Modulus Counters, Binary Up-Down counter, Ripple Counter
10	• Designing Irregular Counters using State Diagram and State Equation. • Shift registers • Shift register Counters: Johnson counter, Ring counter
11	• Memory Systems: read, write operations • RAM family, ROM family • Flash memory programming, read & erase operation. Magnetic Storage: Hard Disk Drive (HDD), SSD R-L transient: Storage cycle; Related Problems.
12	• Operation of 555 integrated timer circuit: Monostable, Astablemultivibrator • Introduction to Programmable Logic Devices (PLDs): Advantages and disadvantages of PLDs over discreet logic gates. • Classification of PLDs
13	• Operation of 555 integrated timer circuit: Monostable, Astable multivibrator • Introduction to Programmable Logic Devices (PLDs): Advantages and disadvantages of PLDs over discreet logic gates. • Classification of PLDs
14	**FINAL-TERM WEEK**

* The faculty reserves the right to change, amend, add or delete any of the contents.

Textbooks/ References

Textbooks:

[1] Thomas L. Floyd, “Digital Fundamentals” 9th edition, Prentice Hall.
[2] M. Morris Mano, “Digital Logic & Computer Design” Prentice Hall.

References:

[1] Ronald J. Tocci & Neal S. Widmer, “Digital Systems” 7th edition, Prentice Hall.
[2] Digital design – Karim and Johnson
[3] Brian Holdsworth and Clive Woods, “Digital Logic Design”-Fourth Edition.
[4] Stephen Brown and Zvonko Vranesic, “Fundamentals of Digital Logic with VHDL Design with CD-ROM”
[5] William J. Dally and R. Curtis Harting, “Digital Design: A Systems Approach”
[6] Victor P. Nelson, H. Troy Nagle, Bill D. Carroll and David Irwin, “Digital Logic Circuit Analysis and Design”
[7] John P. Hayes, “Introduction to Digital Logic Design”
[8] Norman Balabanian and Bradley Carlson, “Digital Logic Design Principles”
[9] Enoch O. Hwang, “Digital Logic and Microprocessor Design with VHDL”
[10] Joseph Cavanagh, “Digital Computer Arithmetic: Design and Implementation (Computer Science)”

Course Requirements

At least **80%** class attendance and submission of ALL assignment/homework **within** the deadline decided by the course teacher is necessary.

Evaluation

Midterm:

Attendance and Performance: 10%
Quiz : 20%
Assignment : 30%
Mid Presentation & Viva : 40%

Final-term:

Attendance and Performance: 10%
Quiz : 20%
[OBE] Assignment : 30%
Final Assessment : 40%
(Quiz/Take home exam/Viva)

Final Grade/ Grand Total: - - - - - - - 40% of Midterm + 60% of Final Term

Assessment rationale:

The examinations will consist of questions regarding topics mentioned in the class schedule.

Quiz

- Due to internet connection problem, there will be Short quiz every week.
- Each quiz mark is 5.
- There will be 5 short quizzes. I will count best 4.
- No makeup quiz will be taken. (You must be serious from first to last).
- Each student should turn on the audio/video for the full duration of the quiz.
- The teacher will perform live online invigilation.
- Teachers will randomly ask the students to share the desktop.

Attendance

- At least 80% presence is necessary.
- Late in Class:10 minutes from the time of start of the class, full attendance. Otherwise late marking. (2 late is equal to one absent).
- Students must inform the course teacher regarding his/her absence before class through e-mail, MS Teams, or via guardian/friend/family to the course teacher.
- **If your attendance is very poor**, it will be informed to **OSA** and they **will contact with your guardian**.

Assignment and VIVA

- There might be 2/3 assignments (OBE/non-OBE) and one Viva.

Nafiz A. Chisty| Head (UG), Dept of EEE; Associate Professor, Dept. of EEE & CoE

Teaching Method

- Maximum topics will be covered from the textbook. For the rest of the topics, reference books will be followed. Some Class notes will be uploaded on the web.
- Students must study up to the last lecture before coming to the class and it is suggested that they should go through the relevant chapter before coming to the class. Just being present in the class is not enough- students must participate in classroom discussions.
- Formal lectures will provide the theoretical base for the subject as well as covering its practical application.
- A set of lecture notes, tutorial examples, with subsequent discussion and explanation, together with suggested reading will support and direct the students in their own personal study.
- Few assignments will be given to the students based on that class to test their class performance.

Teaching Materials

- Teacher would post the syllabus and the lecture notes on the course webpage in VUES.
- Students must store the teaching materials and the course outline/syllabus, as these might be required in future, especially for admission for higher studies.

Missing Evaluations

- Makeup for missing Quiz/Assignment/ etc… will be considered only through valid application procedures with pure evidence of reasoning.
- Student missing less than 40% of the total evaluation for each term (mid/final) will be given 'I' (incomplete) grade along with a strict deadline to complete the missing evaluations by the course teacher.
- Student missing more than 40% of the total evaluation for each term (mid/final), will be given 'UW' (Unofficial Withdraw) grade. Students must go through valid application procedures with pure evidence of reasoning to change 'UW' to 'I'.
- Except extreme cases (accident/hospitalized etc.), marks for attendance will not be considered. On extreme cases, partial/full marks (*judged by the course teacher*) may be given to the student.

During Class

- Students are encouraged to ask question at any moment during the lecture,
- The teacher might ask question to students,
- Students must have active headphone or mic/speaker,
- Teachers will randomly ask the students to share the desktop for checking student activity/ question's answer.

Nafiz A. Chisty| Head (UG), Dept of EEE; Associate Professor, Dept. of EEE & CoE

Consultation

- Students are Encouraged to use email/ MS Teams to communicate with the teacher for Consultation.
- You may communicate during the consulting hours of the teacher or at any time you feel comfortable. The teacher will revert back at his earliest possible time.
- Group/one-to-one consultation both are allowed.

Grading System

The grading system will be strictly followed as par the AIUB grading policy. The following grading system will be strictly followed in this class.

Letter	Grade Point	Numerical %	Remarks
A+	4.00	90 - 100	
A	3.75	85 - < 90	
B+	3.50	80 - < 85	
B	3.25	75 - < 80	Minimum Grade in a Course for Academic Scholarship & Award
C+	3.00	70 - < 75	
C	2.75	65 - < 70	
D+	2.50	60 - < 65	Graduation & Probation
D	2.25	50 - < 60	Retake to improve CGPA
F	0.00	< 50	
I		Incomplete	
W		Withdrawal	
UW		Unofficially Withdrawal	

To pass from AIUB minimum required CGPA is 2.5.

*Effective from Spring 2016 – 2017

Nafiz A. Chisty| Head (UG), Dept of EEE; Associate Professor, Dept. of EEE & CoE

Thanks


AIUB
EEE
FACULTY OF ENGINEERING
AIUB
Faculty of Engineering