EEE 3101: Digital Logic and Circuits

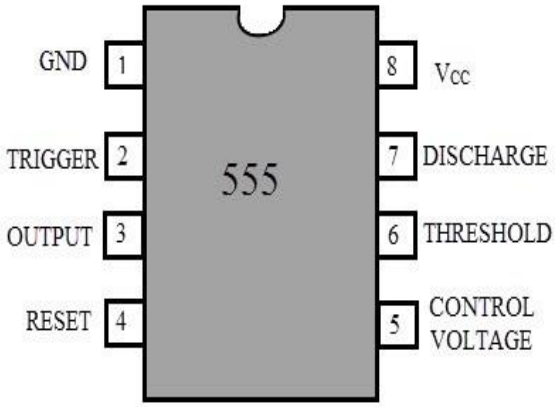
555 Timer

Course Teacher: Nafiz Ahmed Chisty

Head, Department of EEE
Associate Professor, Department of EEE & CoE
Faculty of Engineering
Room# D0105, D Building
Email: chisty@aiub.edu
Website: http://engg.aiub.edu/faculties/nafiz
Website: www.nachisty.com

Introduction

- 555 timer IC was first introduced around 1971 by Signetics Corporation.
- It was the called the “The IC Time Machine”.
- The IC 555 timer is used in different application like an oscillator, pulse generation, timer.
- The name is derived from the three 5k resistors in the IC.
- The operating range of the IC ranges from 4.5V – 15V DC supply.
- The functional parts of the 555 timer IC include flip-flop, voltage divider and a comparator.
- The main function of this IC is to generate an accurate timing pulse.



8-Pin DIP

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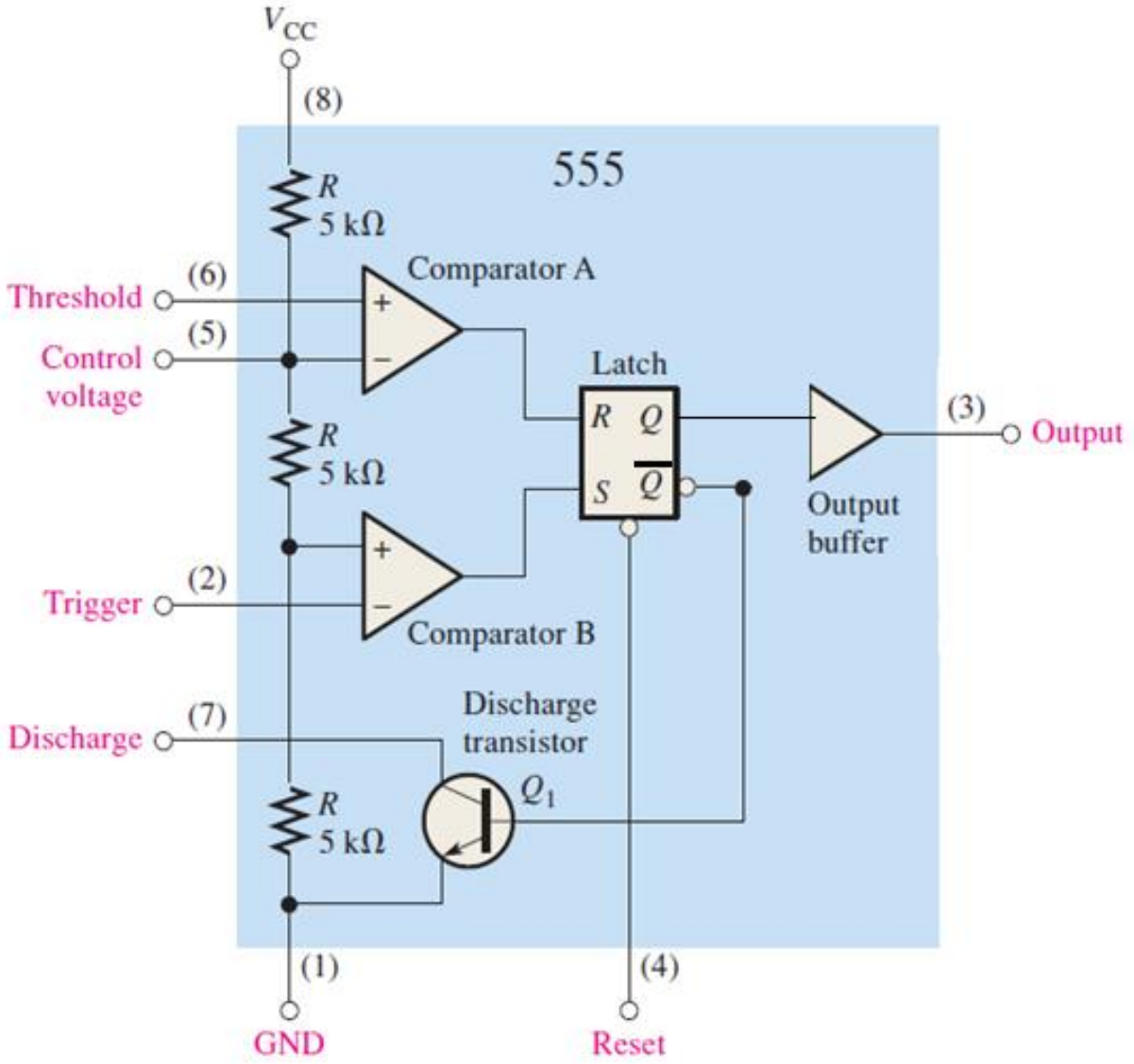
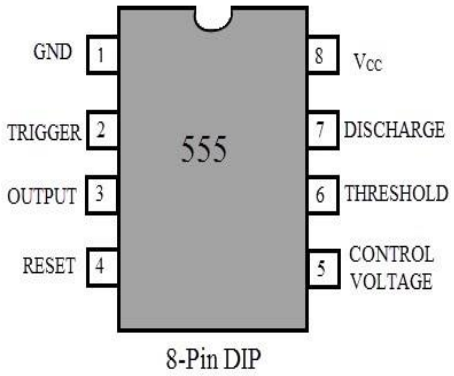
Functional Block Diagram





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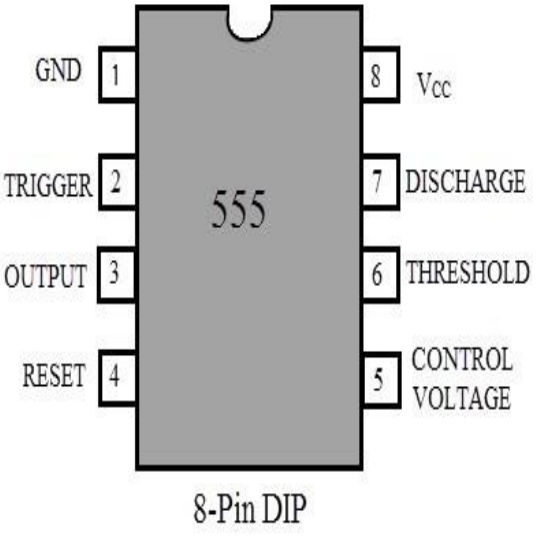
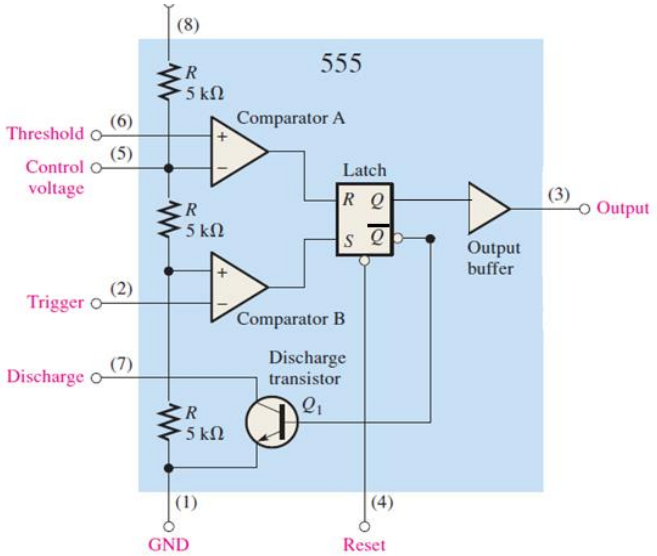
Pin Configuration

- **GND**: All voltages are measured with respect to this terminal.
- **TRIGGER**: The output of the timer depends on the amplitude of the external trigger pulse applied to this pin. When a voltage below $^1/_3$ V_{CC} is applied to this pin, the output of the timer becomes high. The output remains high as long as the trigger terminal is held at low voltage.
- **OUTPUT**: The output of the timer is measured here with respect to ground.
- **RESET**: The 555 timer can be disabled/ reset by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to $+V_{CC}$ to avoid any possibility of false triggering.

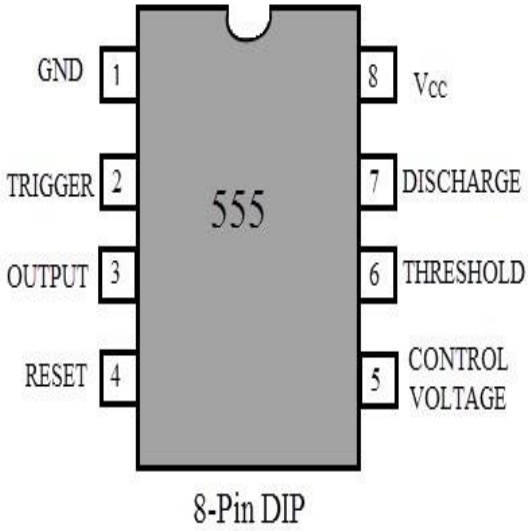


8-Pin DIP



Pin Configuration (contd…)

- **CONTROL VOLTAGE**: An external voltage applied to this terminal changes the threshold as well as the triggering voltage. Thus by imposing a voltage on this pin or by connecting a pot between this pin and ground, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with a 0.01µF Capacitor to prevent any noise problem.
- **THRESHOLD**: When the voltage at this pin is greater than or equal to the threshold voltage, $^2/_3\,V_{CC}$, the output of the timer is low.
- **DISCHARGE**: The pin is connected internally to the collector of transistor Q. When the output is high Q is OFF and acts as an open circuit to external capacitor C connected across it. On the other hand, when the output is low, Q is saturated and acts as a short circuit, shorting out the capacitor C to ground.
- **$+V_{CC}$**: The supply voltage of +5V to +18V is applied to this pin with respect to ground.



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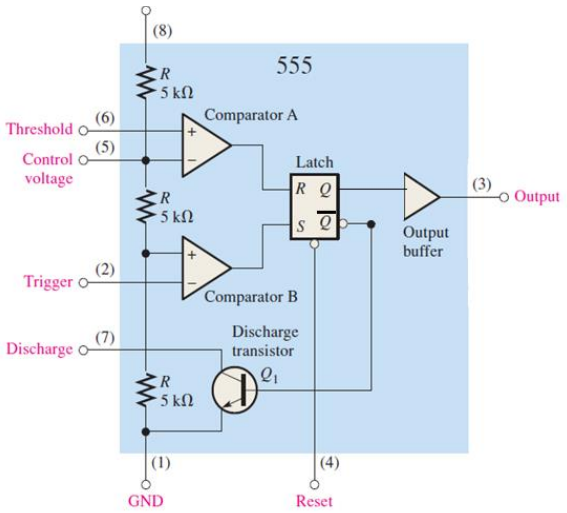

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Function of the Components

- **5K RESISTORS NETWORK**: The resistor network provide the two comparators with the reference voltage. Each resistor drops a voltage of $^1/_3\,V_{CC}$. So for the upper comparator the reference voltage is $^2/_3\,V_{CC}$ and for the lower comparator the reference voltage is $^1/_3\,V_{CC}$.

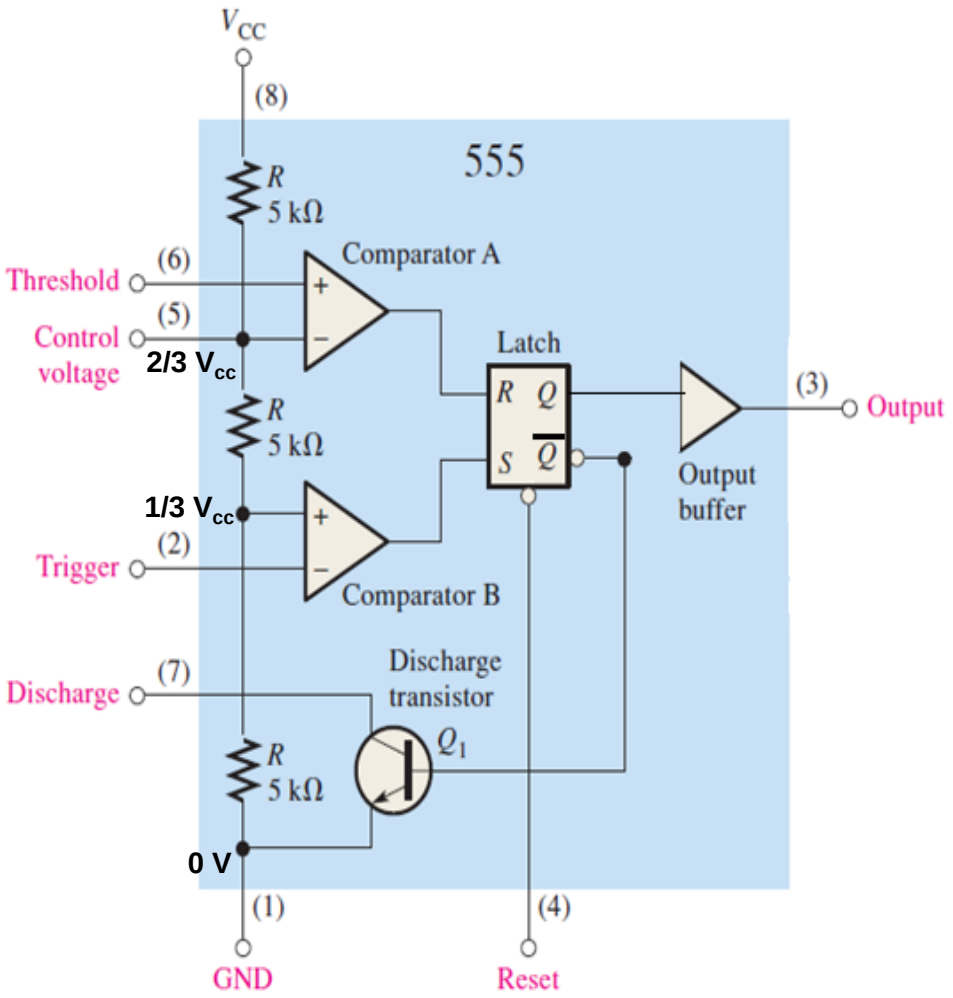
- **VOLTAGE COMPARATORS**: The voltage comparator gives a positive output when the voltage in the +ve input is higher than the –ve input. And when the –ve input is higher than the positive input, the output is 0. When the output of the upper comparator is high, it sets the Flip-Flop and when the output of the lower comparator is high, it resets the Flip-Flop.

- **R-S FLIP-FLOP**: The R-S Flip-Flop is used as a memory element to hold the output. $\bar{Q}$ is connected to the output pin and Q is connected to an NPN transistor.

- **NPN TRANSISTOR:** When a positive voltage is given to the NPN transistor, the NPN transistor goes to saturation. This shorts the emitter and collector terminals. Therefore the discharge pin gets shorted to the ground.

Basic Operation

- When the normally HIGH trigger input momentarily goes below 1/3 V_{CC}, the output of the comparator B switches from LOW to HIGH and sets the S-R latch (Q=1) causing the output (pin 3) to go HIGH and thus also turning the discharge transistor Q1 OFF.
- When the LOW threshold input goes above 2/3 V_{CC} and causes the output of comparator A to switch from LOW to HIGH. This resets the latch (Q=0), causing the output (pin 3) to go back to LOW and thus turning the discharge transistor ON.
- Note: The trigger and threshold inputs are controlled by external components to produce either monostable or astable operation.



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Modes of Operation

- **Astable Mode:** In this mode the output of a 555 timer switches between the two unstable states without any external trigger. The feature of the 555 timer can be used to generate continuous rectangular wave.

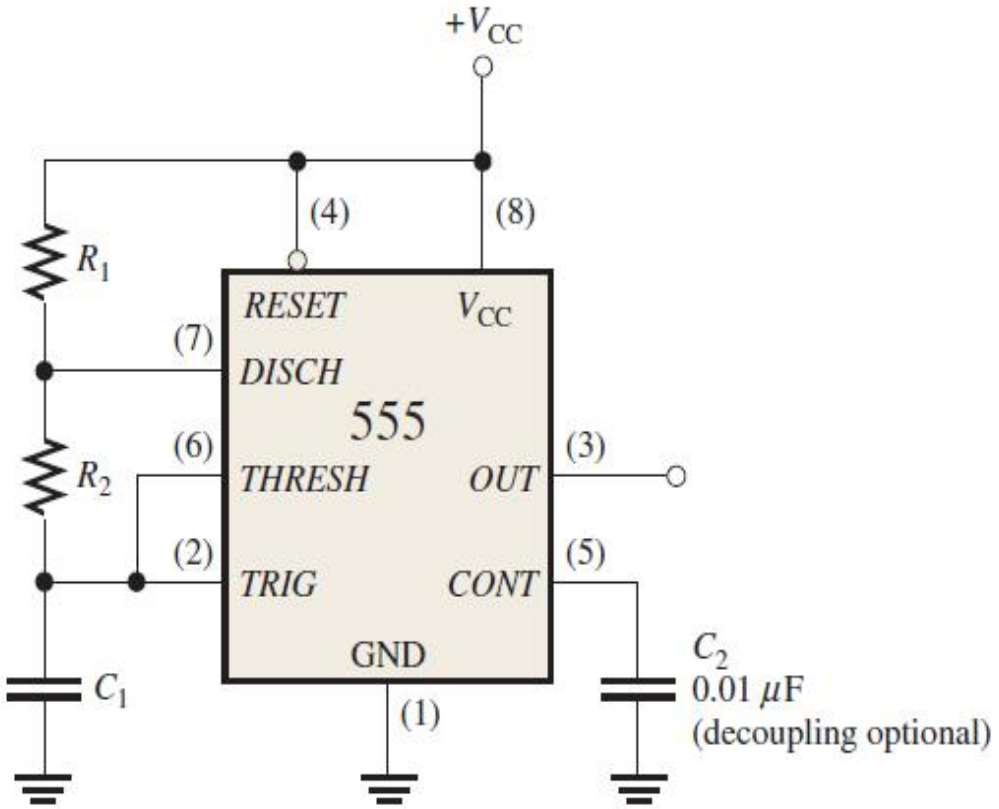
- **Monostable Mode (One-shot):** In this mode, the 555 timer has one stable state. Whenever, the trigger is made low, the 555 timer switches into the unstable state. Then after a certain time, determined by the external combination of resistor and capacitor, the 555 time returns to its stable state.

Astable Mode

Astable Mode Schematic:
The components which determine the operation are:

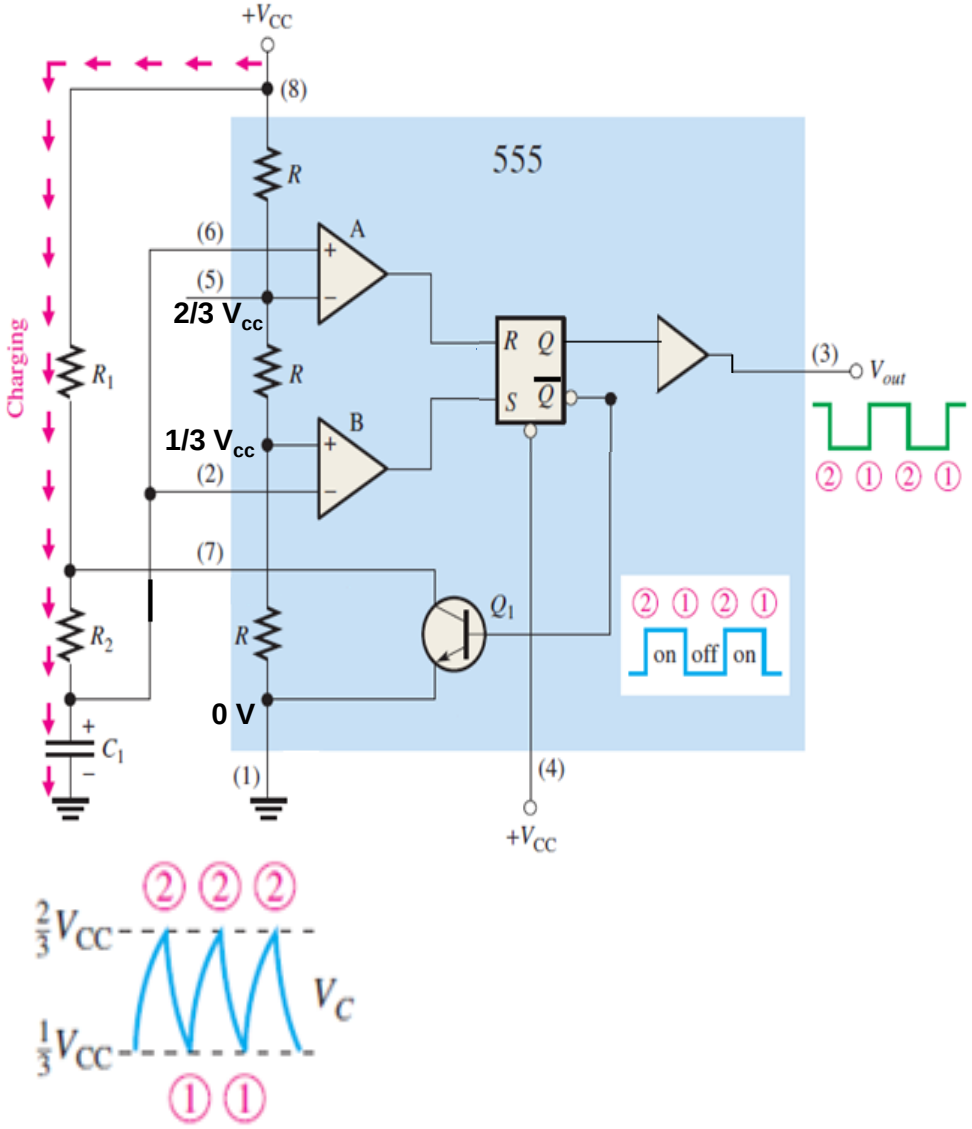
- Two resistors (R_1 and R_2)
- One capacitor (C_1)

The output of this circuit is a square wave pulse.



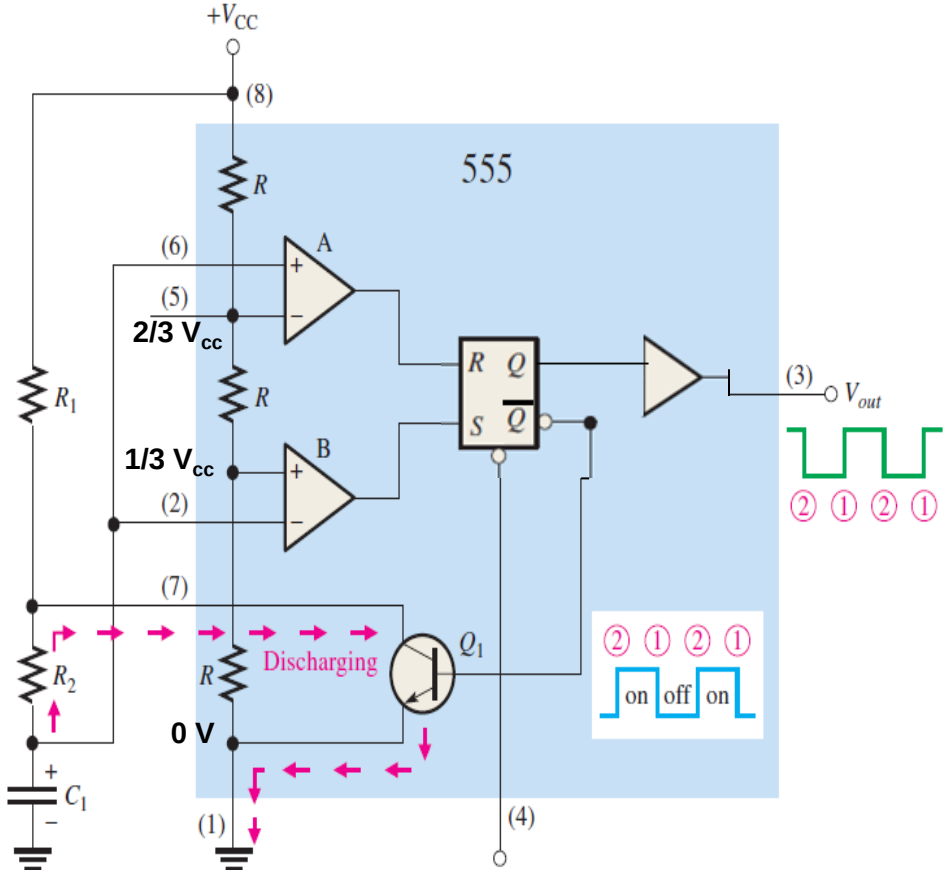
Astable Mode

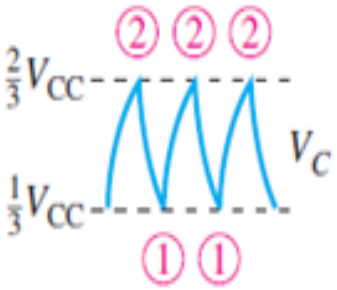
- Initially, when the power is just turned on, the capacitor (C1) remain uncharged and thus the trigger (pin 2) and threshold (pin 6) is at 0V. So, output of comparator A is 0 and comparator B is 1. Thus, Q1 is OFF.
- Now, C1 begins charging through R1 and R2, indicated in Figure. When C1 is just below 1/3 VCC, the output of comparator B is 1 and the flip-flop is set. Thus, the output (pin3) is 1.
- The transistor Q1 is OFF.
- When C1 charges beyond 1/3 VCC, then the output of comparator B is 0. However, the output (pin3) is still 1 and the transistor is still OFF.
- So during the charging phase the output (pin3) of the 555 timer remains HIGH.



Astable Mode

- Once the voltage of the C1 is just beyond 2/3 VCC, the output of the comparator A becomes 1.
- This resets the flip-flop. Thus the output (pin3) is 0. However, Q1 turns on and the capacitor starts discharging.
- Once the voltage of C1 is below 2/3 V_{CC}, the output of the comparator A becomes 0. However, the capacitor still discharges. And the output (pin 3) remains 0.
- Therefore, during the discharge phase the output of the 555 time is 0.
- When the capacitor C1 discharges just below 1/3 V_{CC}, the output of the comparator becomes 1 and the flip-flop is again set.
- Thus, again the charging cycle begins.





Astable Mode

- The capacitor charges through R1 and R2 and during the charging phase the output is HIGH. Thus, time of the HIGH pulse can be calculated as:

$$T_H = 0.693C_1(R_1 + R_2)$$

- The capacitor discharges through only R2 and during the discharging phase the output is LOW. Thus time of LOW pulse can be calculated as:

$$T_L = 0.693C_1(R_2)$$

- The time period of the oscillator is:

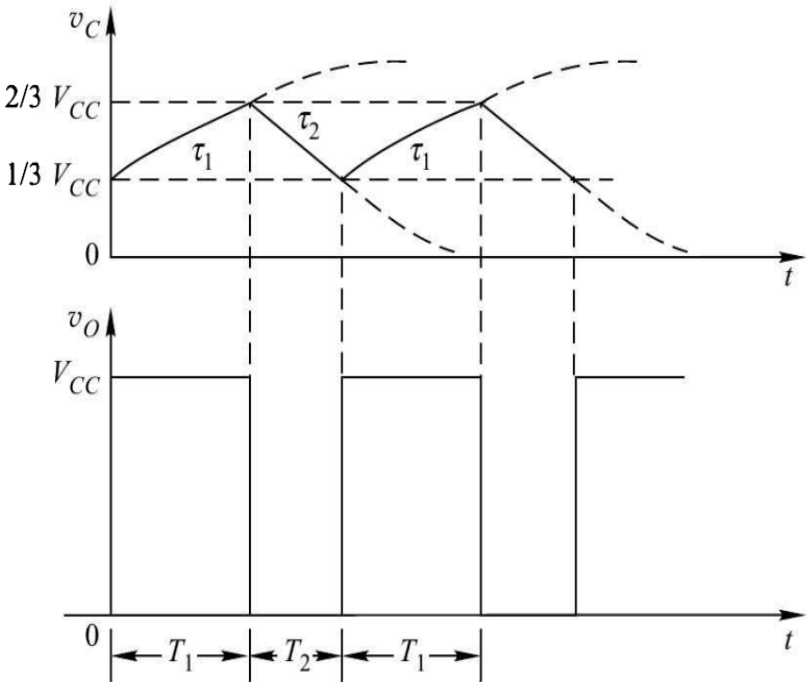
$$T = T_H + T_L = 0.693C_1(R_1 + 2R_2)$$

- Frequency of the oscillator is:

$$F = \frac{1}{0.693C_1(R_1 + 2R_2)}$$

- Duty cycle:

$$D.C. = \frac{T_H}{T_H + T_L}$$



$$\text{Duty cycle} = \left(\frac{R_1 + R_2}{R_1 + 2R_2}\right)100\%$$

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Mathematical Problem

- **Design an oscillator for a frequency of 200Hz with a duty cycle of 78%. Determine the time period, high & low time, R_2 and R_1 (assume $C_1 = 10\mu F$)**

Given:

F= 200Hz

D.C. = 78%= 0.78

C_1= 10μF

- Time Period (T):

$$T = \frac{1}{F} = \frac{1}{200Hz} = 0.005s$$

- Time HIGH and Time LOW:

$$T_H = .78 \times 0.005s = 0.0039s = 3.9ms$$
$$T_L = .22 \times 0.005s = 0.0011 = 1.1ms$$

- Value of R_2:

$$T_L = 0.693R_2C_1$$
$$1.1ms = 0.693 \times R_2 \times 10\mu F$$
$$R_2 = 158.7\Omega$$

- Value of R_1:

$$T_H = 0.693C_1(R_1 + R_2)$$
$$3.9ms = 0.693(R_1 + R_2)C_1$$
$$3.9ms = 0.693(R_1 + R_2)10\mu F$$
$$R_1 = 404.1\Omega$$

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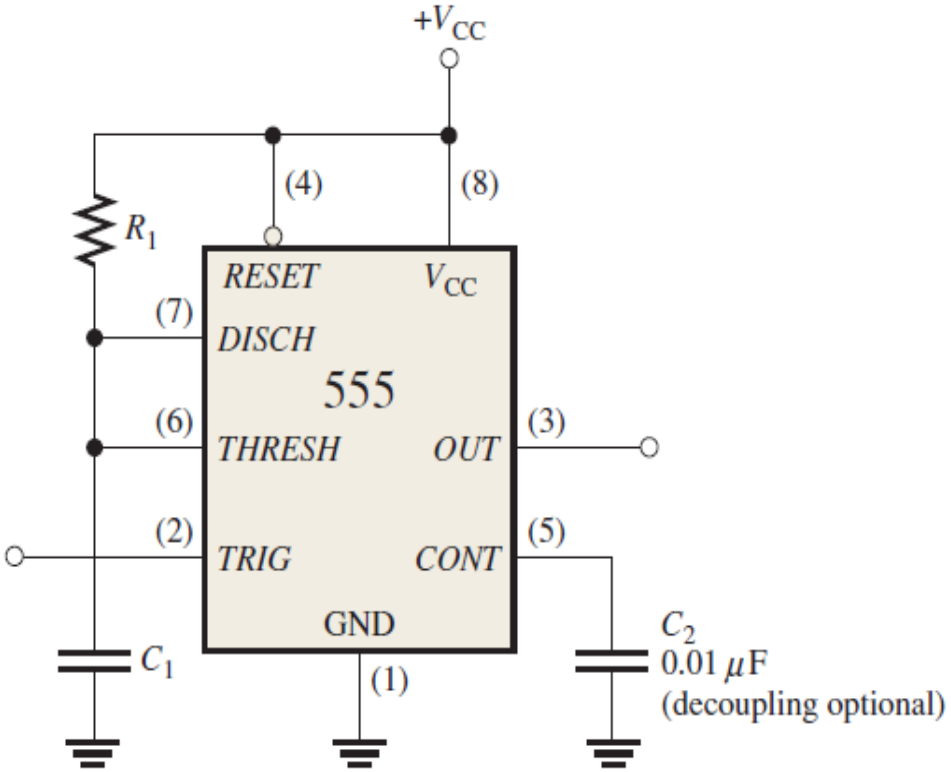
Monostable Mode

Monostable Mode Schematic:
The components which determine the operation are:

- One resistors (R_1)
- One capacitor (C_1)



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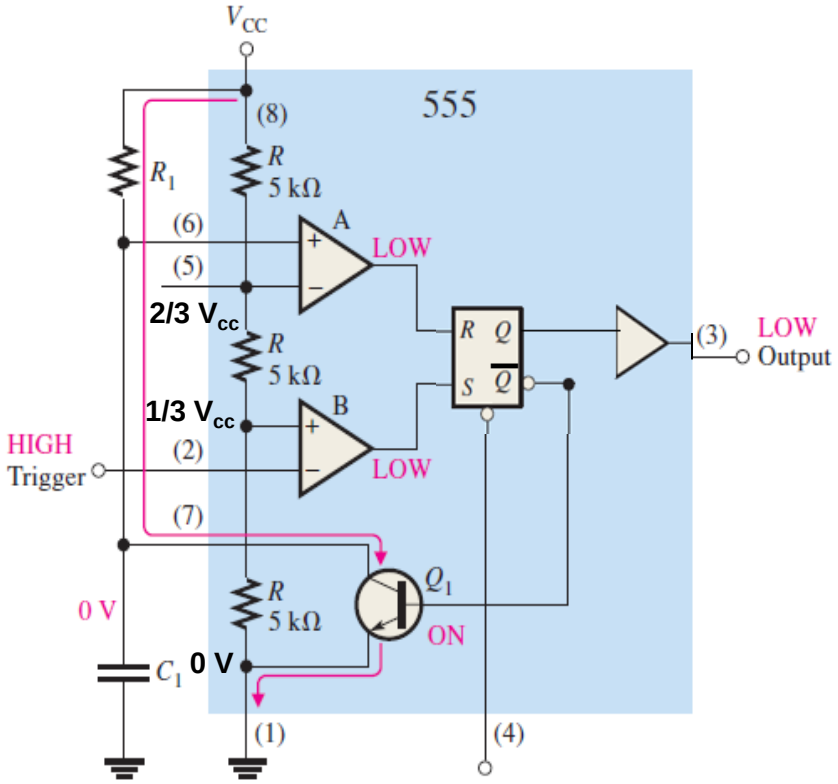
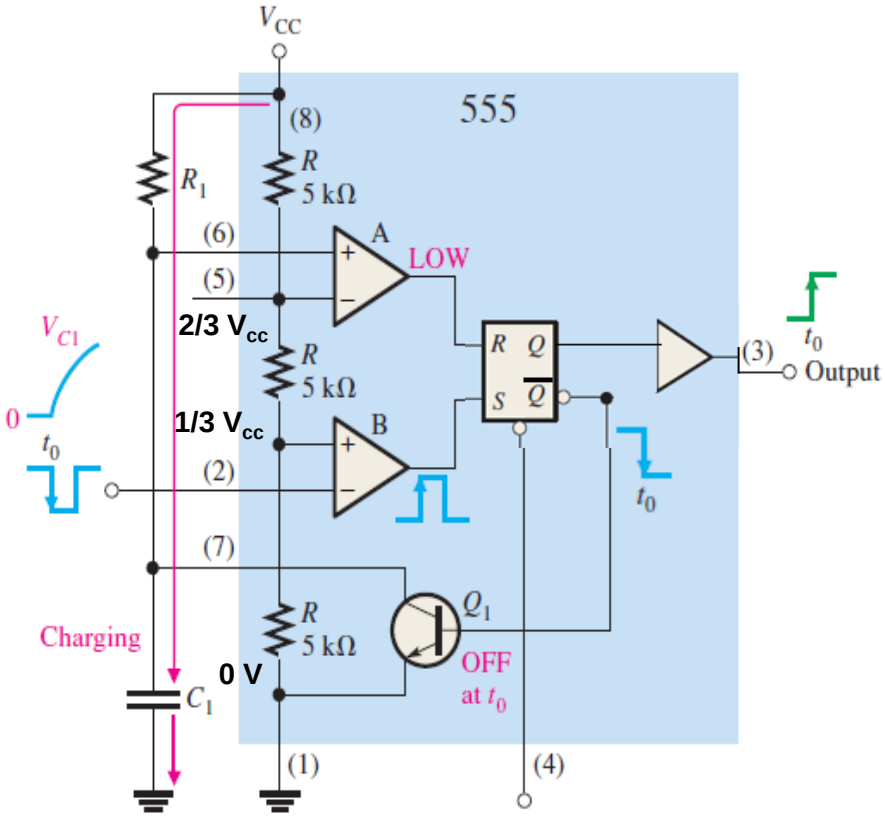
Monostable Mode

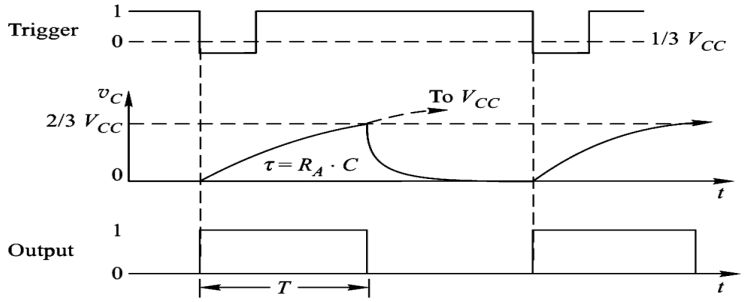
- Prior to triggering the output is LOW and is in the stable state.
- The discharge capacitor Q1 is ON.
- Thus C1 is bypassed and hence C1 do not charge.



Monostable Mode

- At time, t_0, a negative going triggering pulse is applied.
- Hence the trigger pin becomes less than 1/3 V_{CC}. Thus the output of comparator B becomes 1.
- This sets the flip-flop and the output (pin 3) is HIGH.
- Consequently, the transistor Q1 is OFF and the capacitor starts charging through R_1.
- The capacitor charges till it reaches 2/3 V_{CC}.
- The time required for the capacitor to charge till 2/3 V_{CC} determines the width of the HIGH pulse (unstable state)





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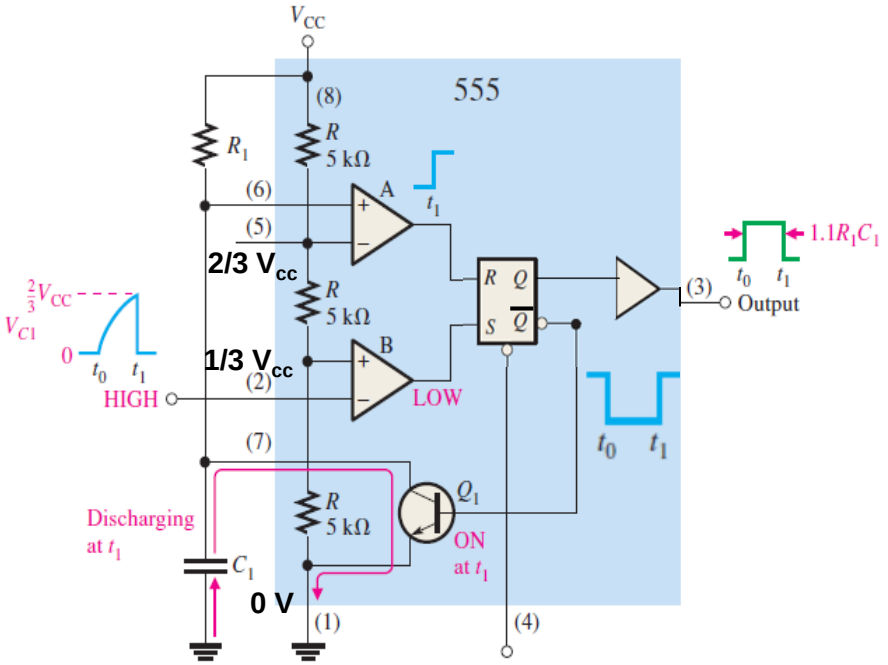
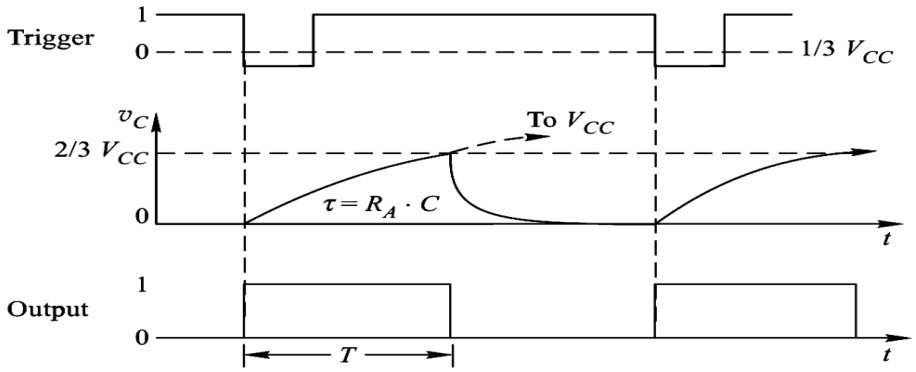
Monostable Mode

- At the end of the charging phase, at time t_1, the capacitor charge is just above 2/3 V_{CC}.
- Thus the output of the comparator A becomes 1 and the flip-flop resets.
- Consequently, at the same time, the output (pin3) becomes 0 and the transistor Q1 turns on.
- Thus, the capacitor starts discharging and finally discharges to zero.
- The width of the pulse is :

$$T_W = 1.1R_1C_1$$





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Reference:

[1] Thomas L. Floyd, "Digital Fundamentals" 11th edition, Prentice Hall.
[2] M. Morris Mano, "Digital Logic & Computer Design" Prentice Hall.
[3] Mixed contents from Vahid And Howard.

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Thanks