EEE 3101: Digital Logic and Circuits

Programmable Logic Devices

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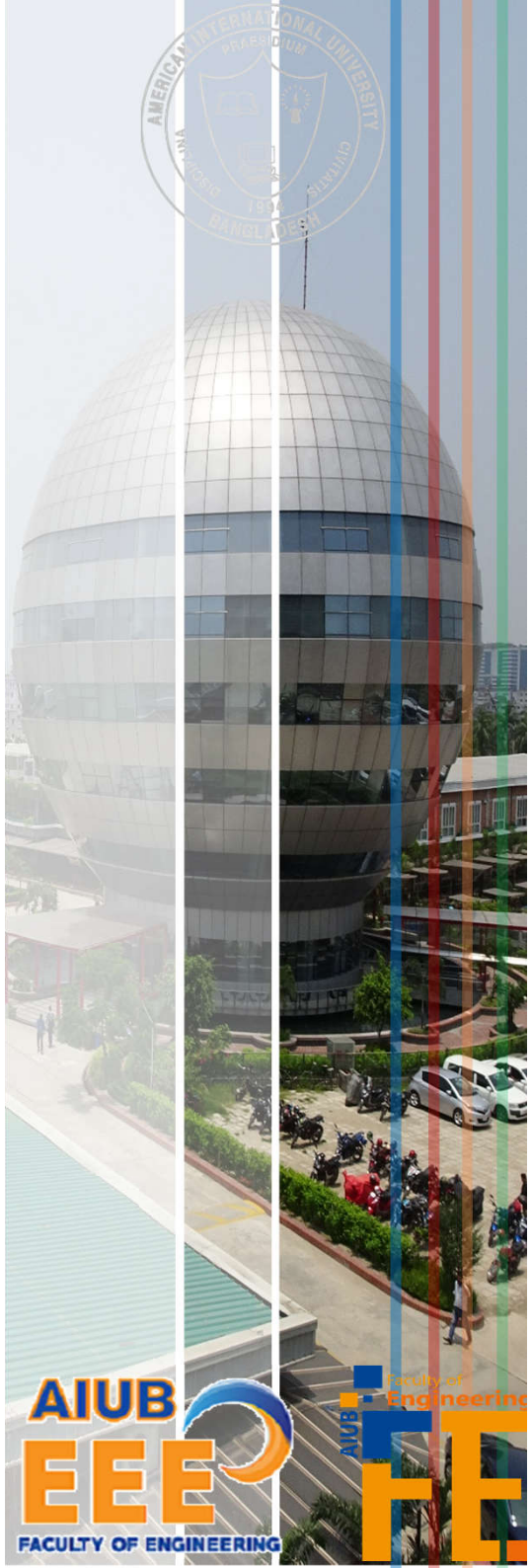

Introduction

- Programmable Logic Devices (PLD)
  - It is used to implement Boolean functions of digital systems.
  - General purpose chip for implementing circuits
  - Can be customized using programmable switches

- Advantages PLDs:
  - Less board space needed
  - Fewer printed circuit board
  - Smaller Enclosure
  - Programmability
  - Re-programmability

- Custom chips: standard cells, sea of gates

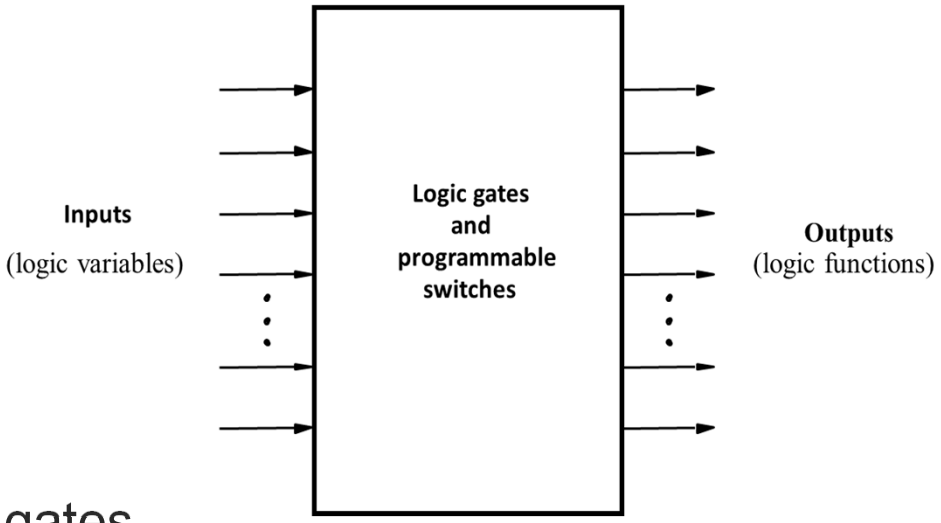

Fig: PLD as a Black Box

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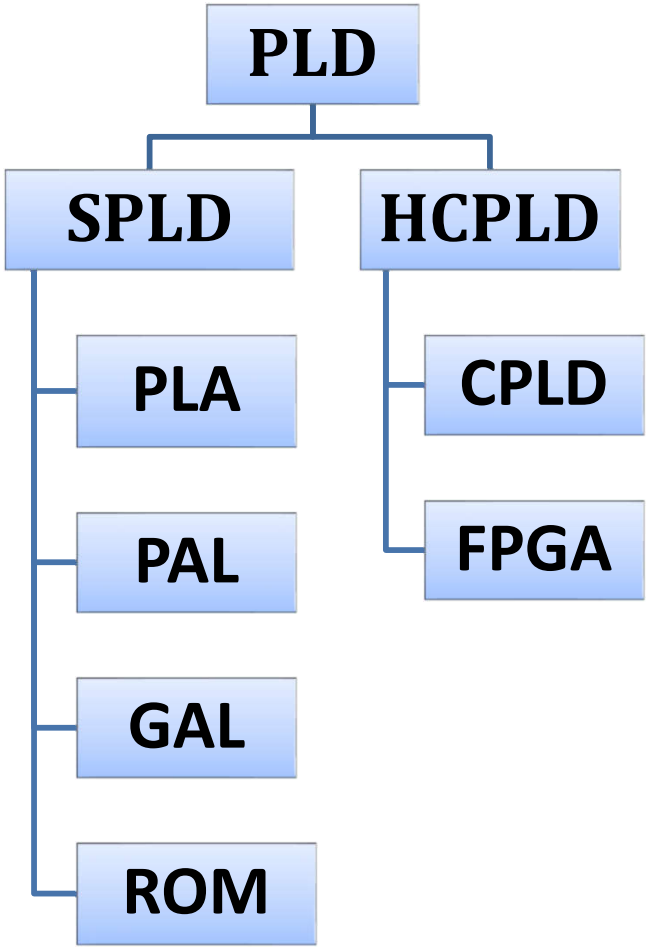
Classification of PLD



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Simple Programmable Logic Device (SPLD)

- SPLD stands for Simple Programmable Logic Device. PLA stands for Programmable Logic Array . PAL stands for Programmable Array Logic. GAL stands for Generic Array Logic.
- PAL is one time programmable (OTP). GAL is reprogrammable.
- Any SOP within a defined number of variables can be implemented using PLA, PAL and GAL.
- SPLDs must be programmed so that the switches are in the correct places
  - CAD tools are usually used to do this
    - A fuse map is created by the CAD tool and then that map is downloaded to the device via a special programming unit
  - There are two basic types of programming techniques
    - Removable sockets on a PCB
    - In system programming (ISP) on a PCB
      - This approach is not very common for PLAs and PALs but it is quite common for more complex PLDs

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An SPLD Programming Unit

- The SPLD is removed from the PCB, placed into the unit and programmed there

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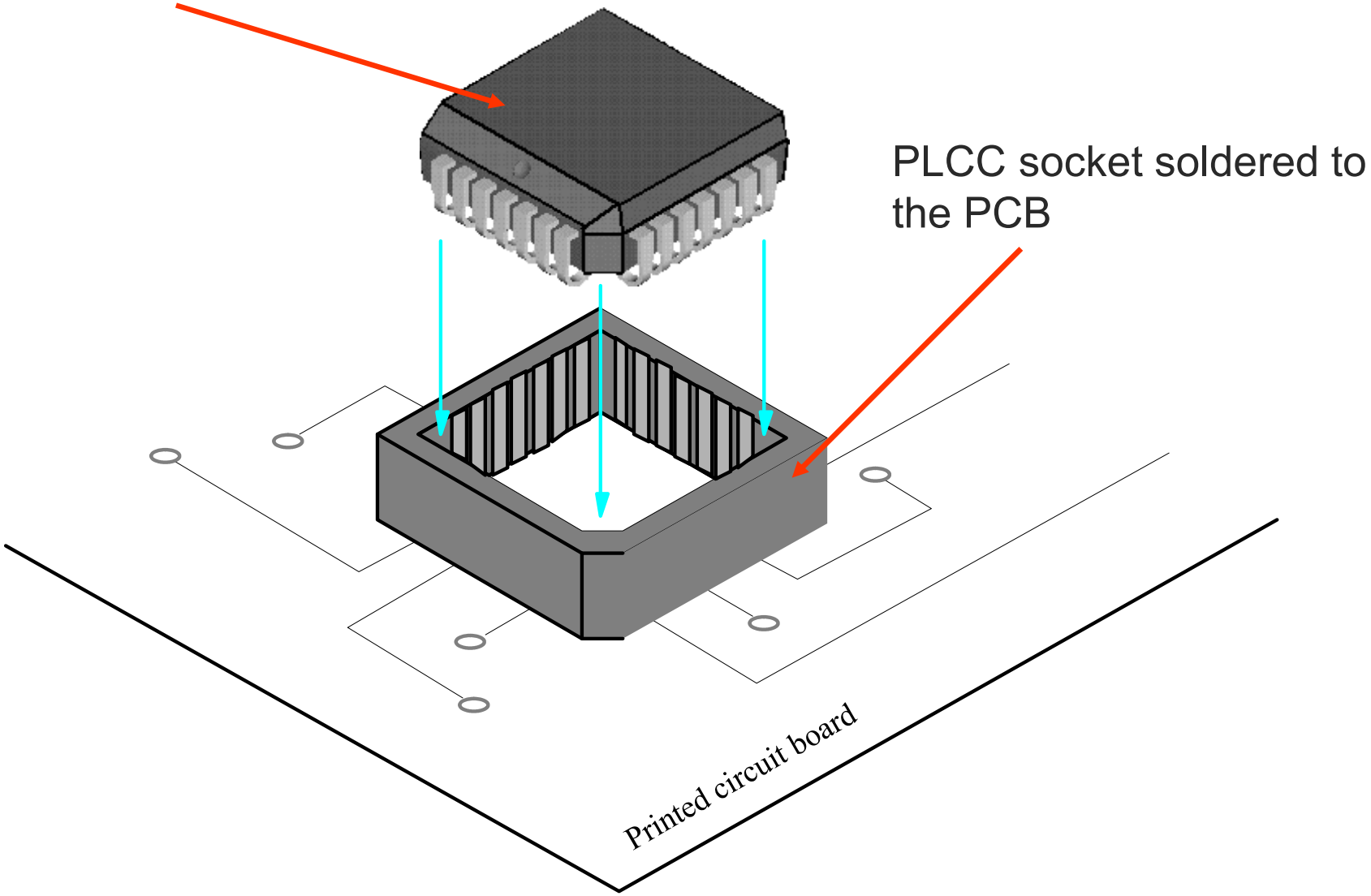
Removable SPLD Socket Package

- PLCC (plastic-leaded chip carrier)



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In System Programming (ISP)

- Used when the SPLD cannot be removed from the PCB
- A special cable and PCB connection are required to program the SPLD from an attached computer
- Very common approach to programming more complex PLDs like CPLDs, FPGAs, etc.

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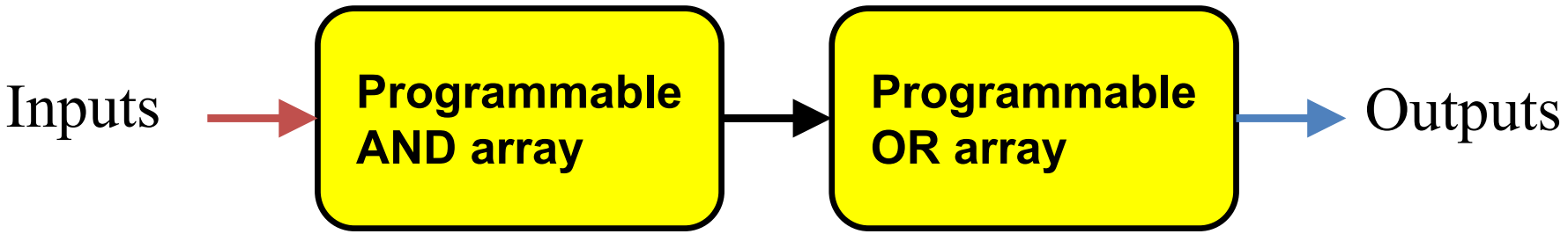
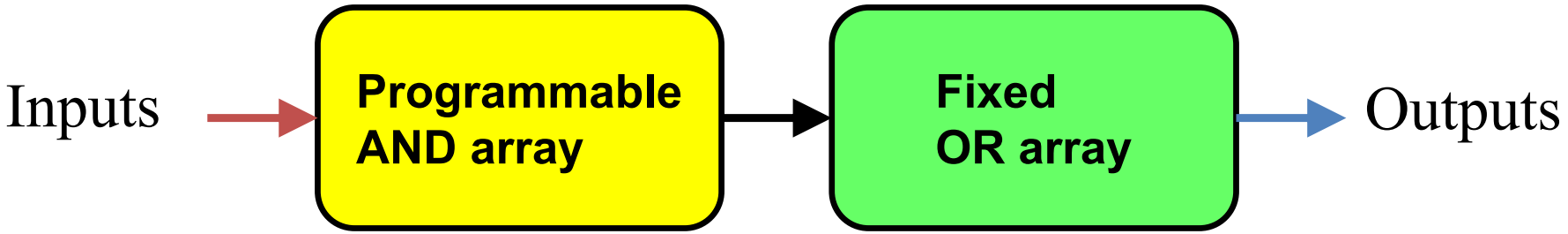
SPLD

- PLA



- PAL



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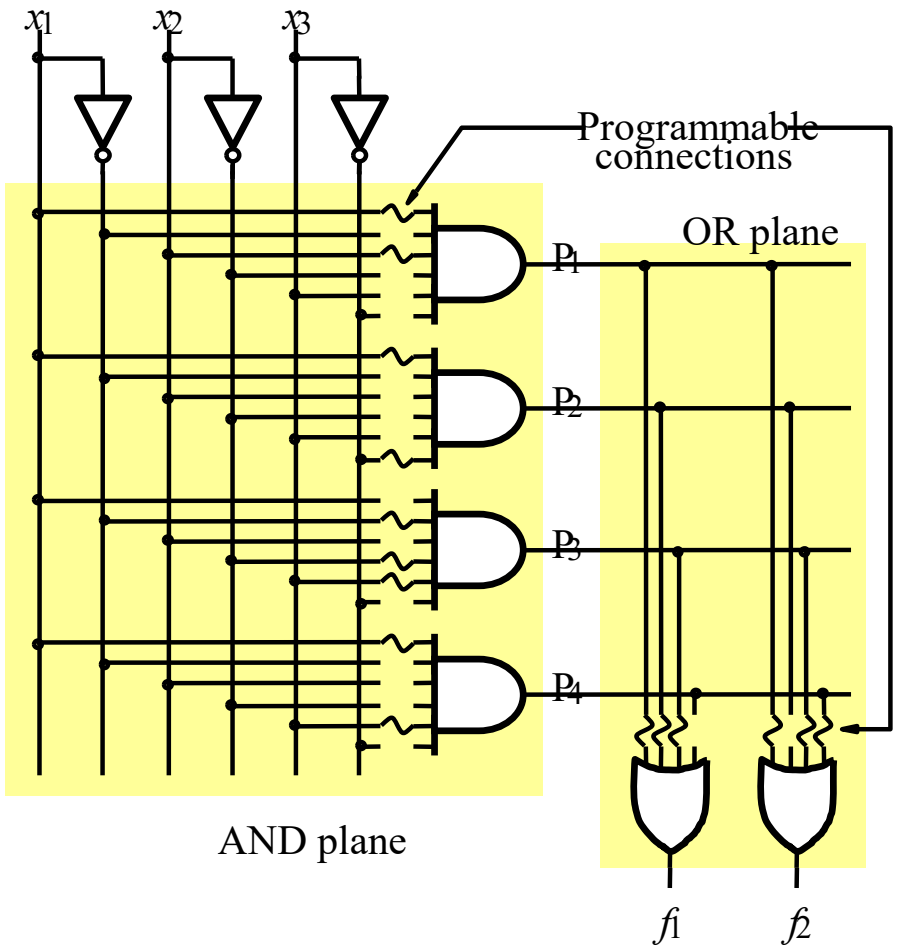
Programmable Logic Array (PLA)

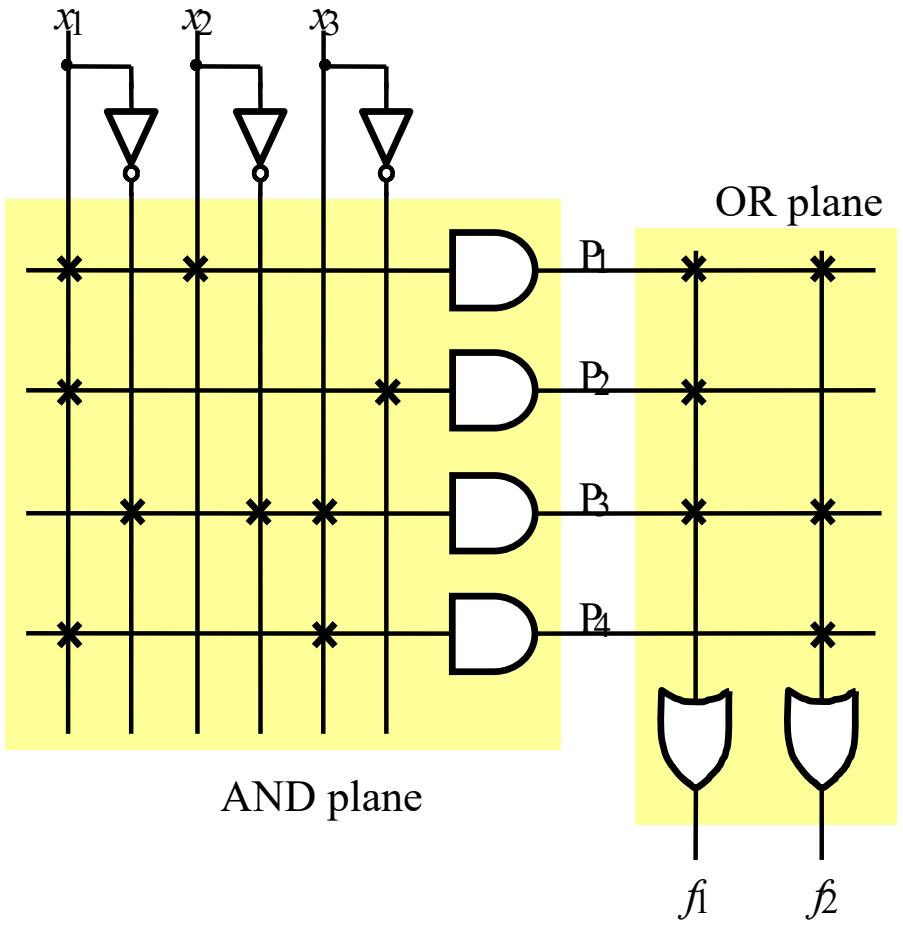
$$f_1 = x_1x_2+x_1x_3'+x_1'x_2'x_3$$

$$f_2 = x_1x_2+x_1'x_2'x_3+x_1x_3$$

- Gate Level Version of PLA



- Customary Schematic of a PLA



x marks the connections left in place after programming

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Limitations of PLAs

- PLAs come in various sizes
  - Typical size is 16 inputs, 32 product terms, 8 outputs
    - Each AND gate has large fan-in → this limits the number of inputs that can be provided in a PLA
    - 16 inputs → 3^{16} = possible input combinations; only 32 permitted (since 32 AND gates) in a typical PLA
    - 32 AND terms permitted → large fan-in for OR gates as well
      - This makes PLAs slower and slightly more expensive than some alternatives to be discussed shortly
    - 8 outputs → could have shared minterms, but not required

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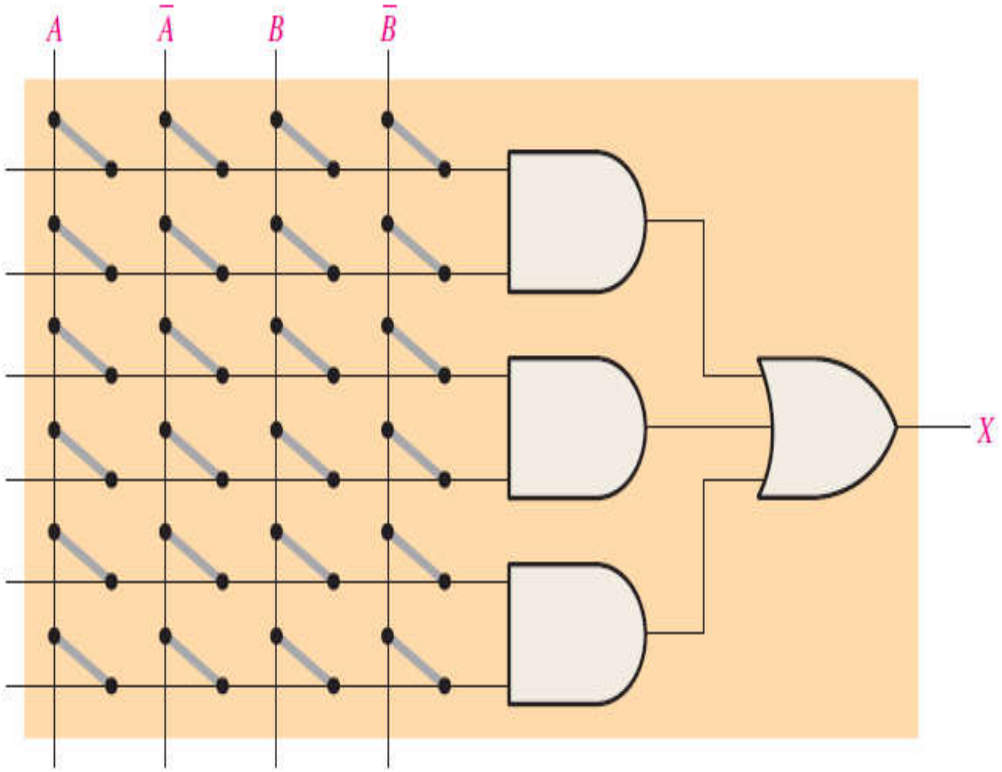
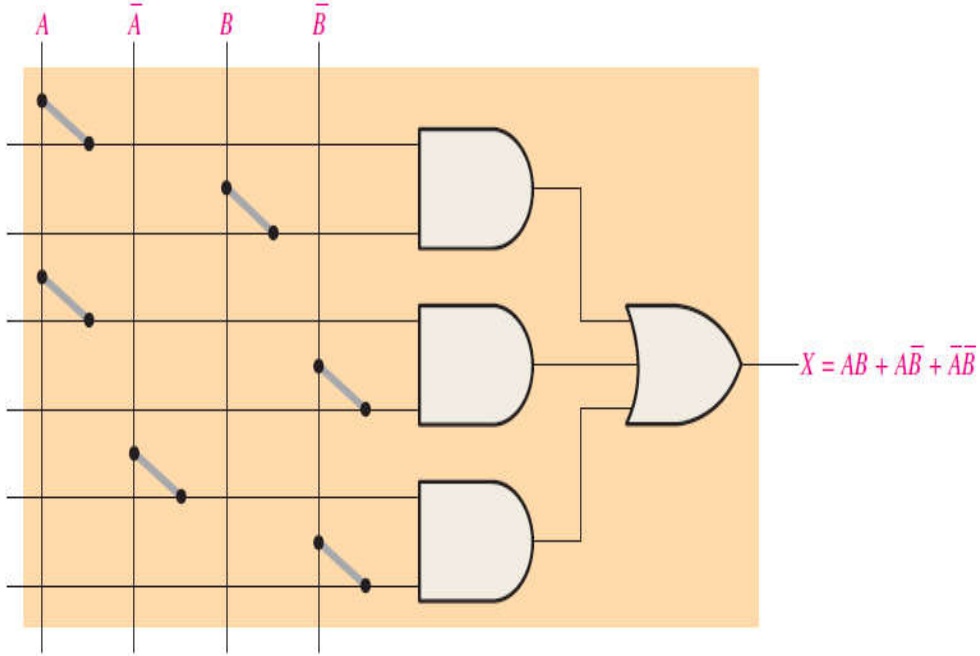
Programmable Array Logic (PAL)

- PAL stands for Programmable Array Logic.
- It is an one time programmable device.
- PALs have many inputs and outputs.
- Each programmable link, which is a fuse incase of a PAL, is called a cell.
- Each row is connected to the input of an AND gate.
- Each column is connected to the input variable or its complement.
- By programming the presence and absence of a fuse connection, any combination of input variables or complements can be applied to AND gates.
- Only SOPs can be implemented.





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Comparing PALs and PLAs

- PALs have the same limitations as PLAs (small number of allowed AND terms) plus they have a fixed OR plane → less flexibility than PLAs
- PALs are simpler to manufacture, cheaper, and faster (better performance)
- PALs also often have extra circuitry connected to the output of each OR gate
  - The OR gate plus this circuitry is called a *macrocell*

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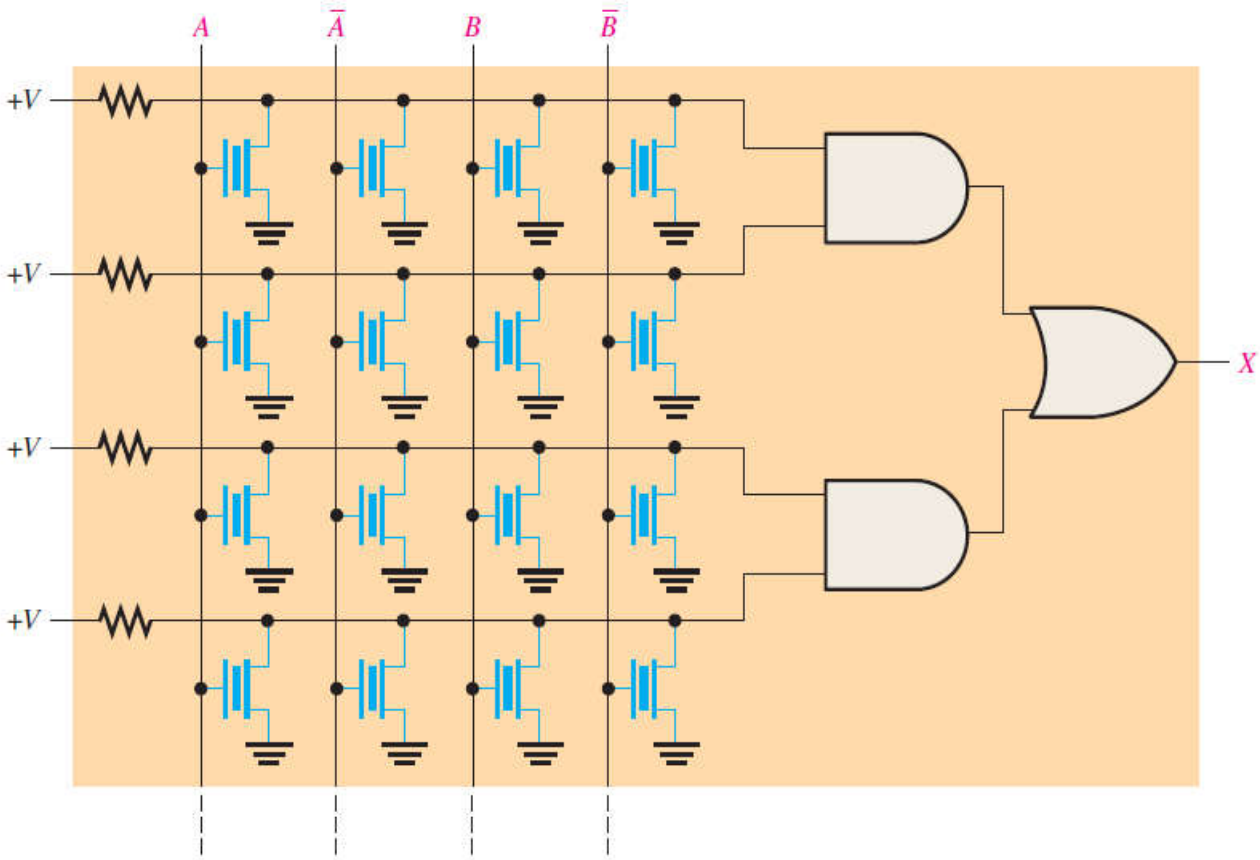
Generic Array Logic (GAL)

- GAL works almost the same way as PAL.
- It is reprogrammable.
- Instead of fuses it uses a programmable technology such as EEPROM.



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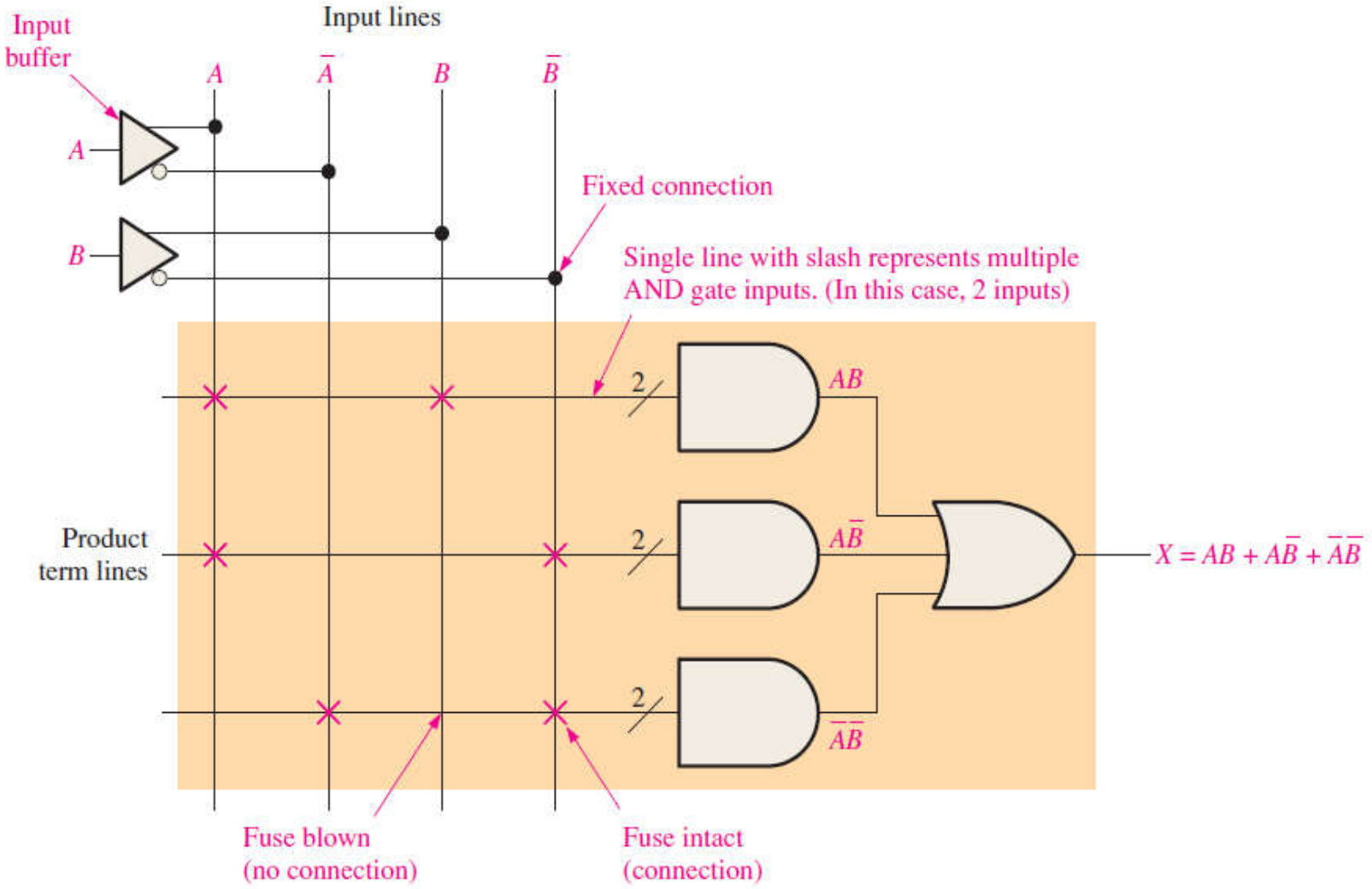
Simplified Notation for PAL/GAL



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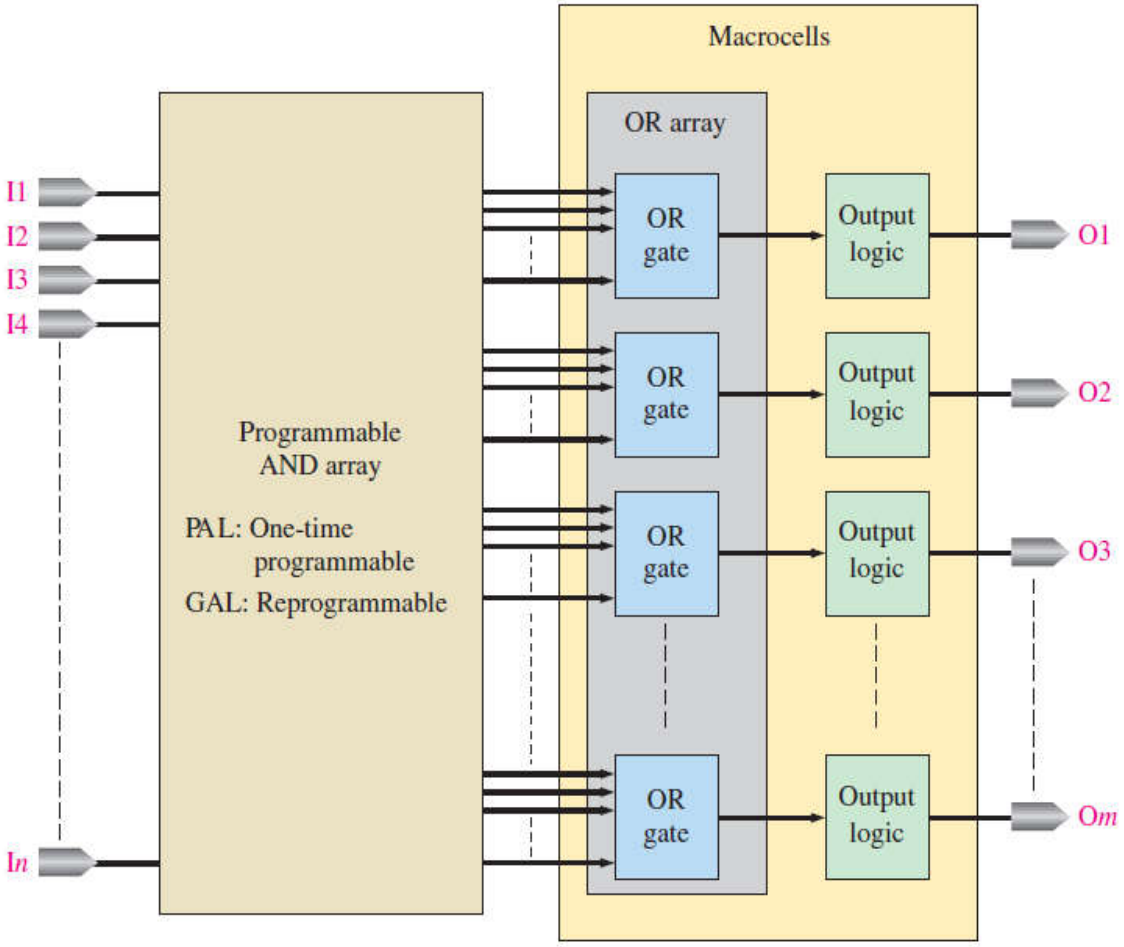
Generic Block Diagram for PAL/GAL

- The AND array is programmable.
- For PAL the AND array is one time programmable.
- For GAL the AND array is reprogrammable.
- The programmable AND array outputs go to fixed OR gates.
- OR gates are connected to additional output logic.
- An OR gate combined with Output logic is called Macro-cell.
- In GAL Macro-cell is often reprogrammable.



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CPLD

- Complex Programmable Logic Devices (CPLD)
- SPLDs (PLA, PAL) are limited in size due to the small number of input and output pins and the limited number of product terms
  - Combined number of inputs + outputs < 32 or so
- CPLDs contain multiple circuit blocks on a single chip
  - Each block is like a PAL: PAL-like block
  - Connections are provided between PAL-like blocks via an interconnection network that is programmable
  - Each block is connected to an I/O block as well

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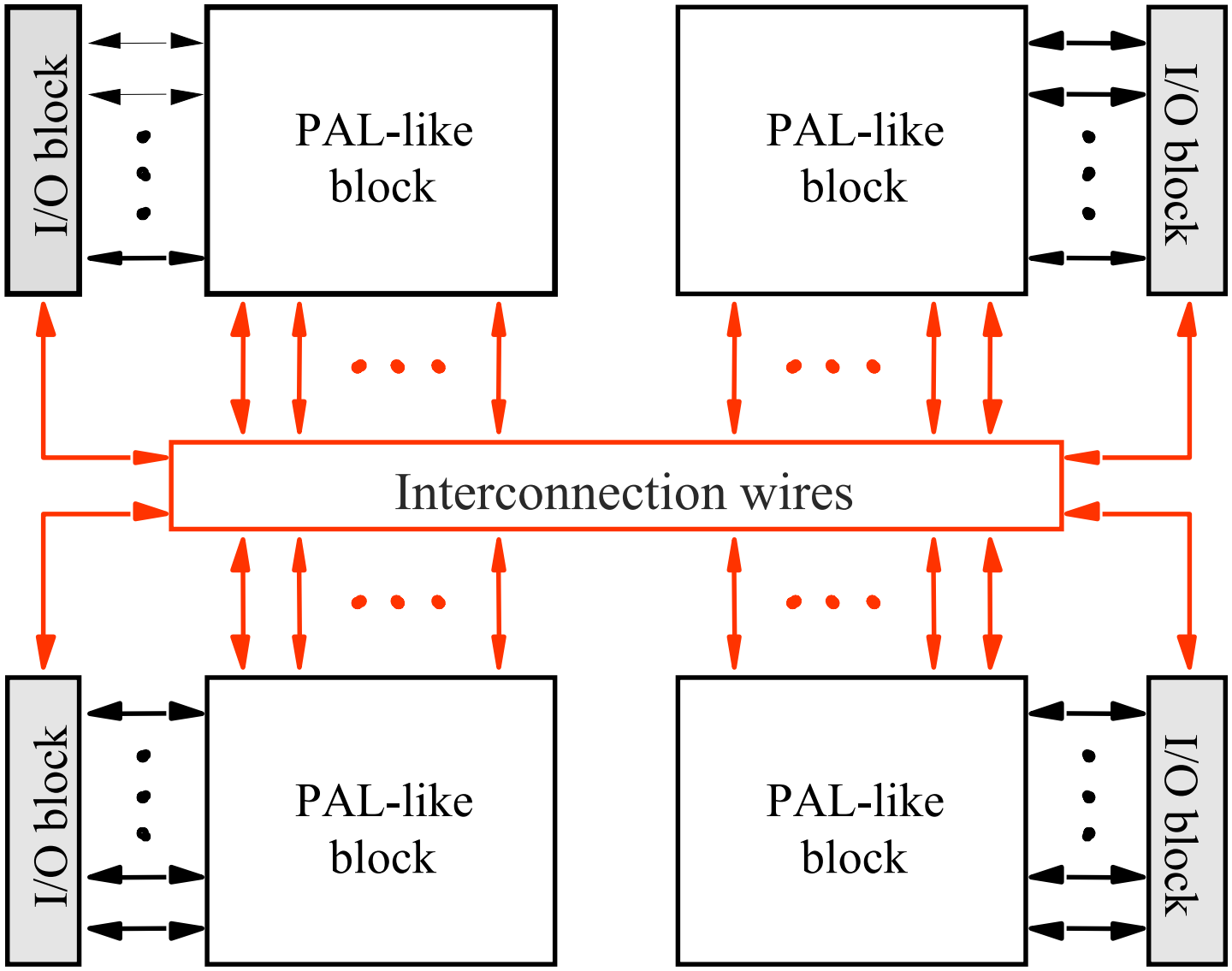
Structure of a CPLD



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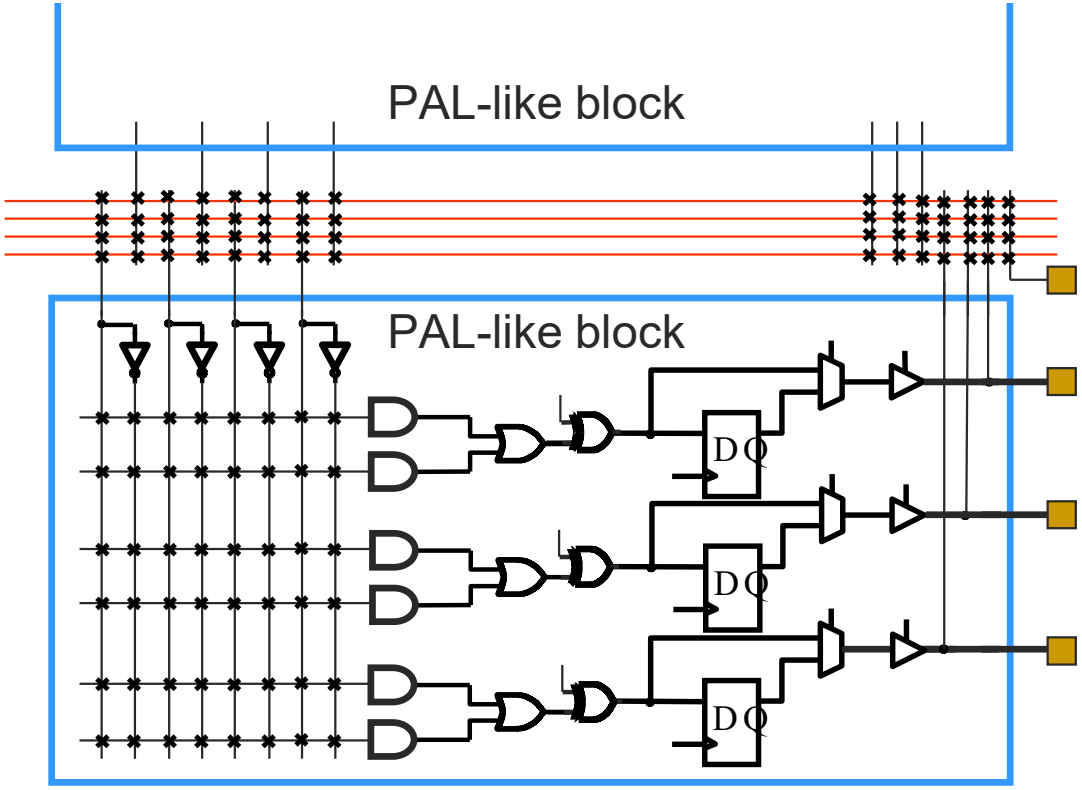
Internal Structure of a PAL-like Block

- Includes macrocells
  - Usually about 16 each
- Fixed OR planes
  - OR gates have fan-in between 5-20
- XOR gates provide negation ability
  - XOR has a control input



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More on PAL-like Blocks

- CPLD pins are provided to control XOR, MUX, and tri-state gates
- When tri-state gate is disabled, the corresponding output pin can be used as an input pin
  - The associated PAL-like block is then useless
- The AND plane and interconnection network are programmable
- Commercial CPLDs have between 2-100 PAL-like blocks

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Reference:

[1] Thomas L. Floyd, "Digital Fundamentals" 11th edition, Prentice Hall.
[2] M. Morris Mano, "Digital Logic & Computer Design" Prentice Hall.
[3] Mixed contents from Vahid And Howard.

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Thanks

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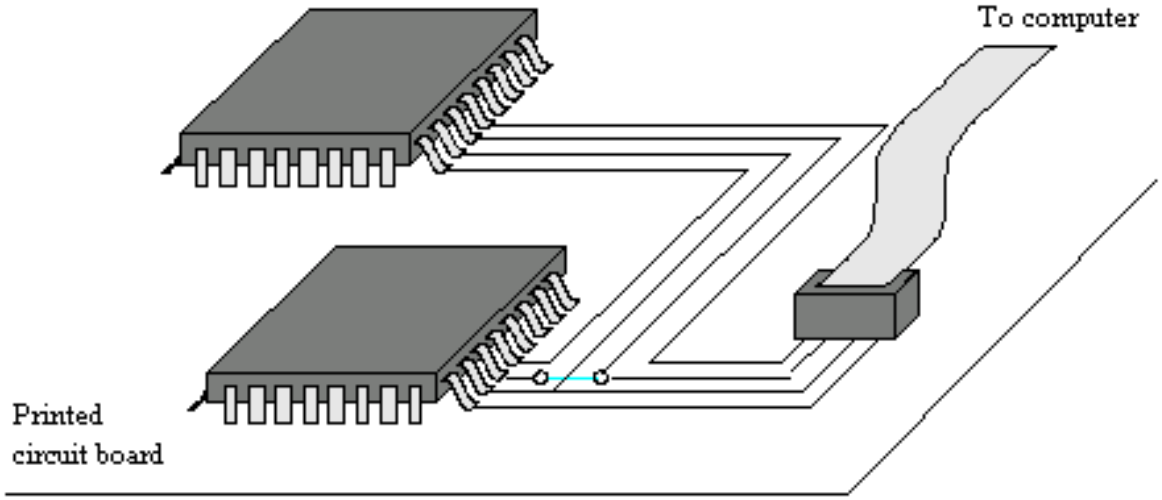
Programming a CPLD

OPTIONAL from this slide onwards

- CPLDs have many pins – large ones have > 200
  - Removal of CPLD from a PCB is difficult without breaking the pins
  - Use ISP (in system programming) to program the CPLD
  - JTAG (Joint Test Action Group) port used to connect the CPLD to a computer



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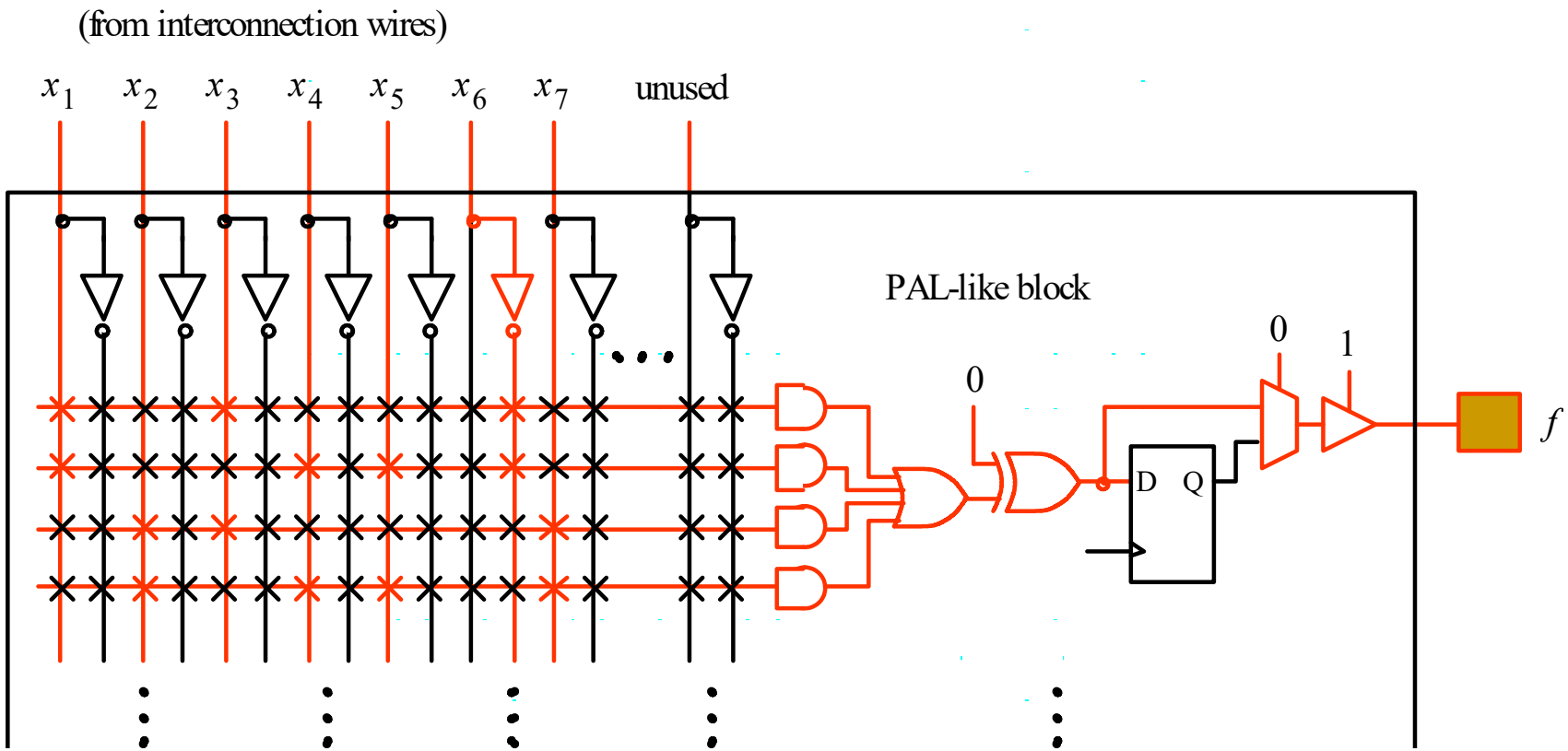
Example CPLD

- Use a CPLD to implement the function
  - $f = x_1x_3x_6' + x_1x_4x_5x_6' + x_2x_3x_7 + x_2x_4x_5x_7$



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FPGA

- SPLDs and CPLDs are relatively small and useful for simple logic devices
  - Up to about 20000 gates
- Field Programmable Gate Arrays (FPGA) can handle larger circuits
  - No AND/OR planes
  - Provide logic blocks, I/O blocks, and interconnection wires and switches
  - Logic blocks provide functionality
  - Interconnection switches allow logic blocks to be connected to each other and to the I/O pins

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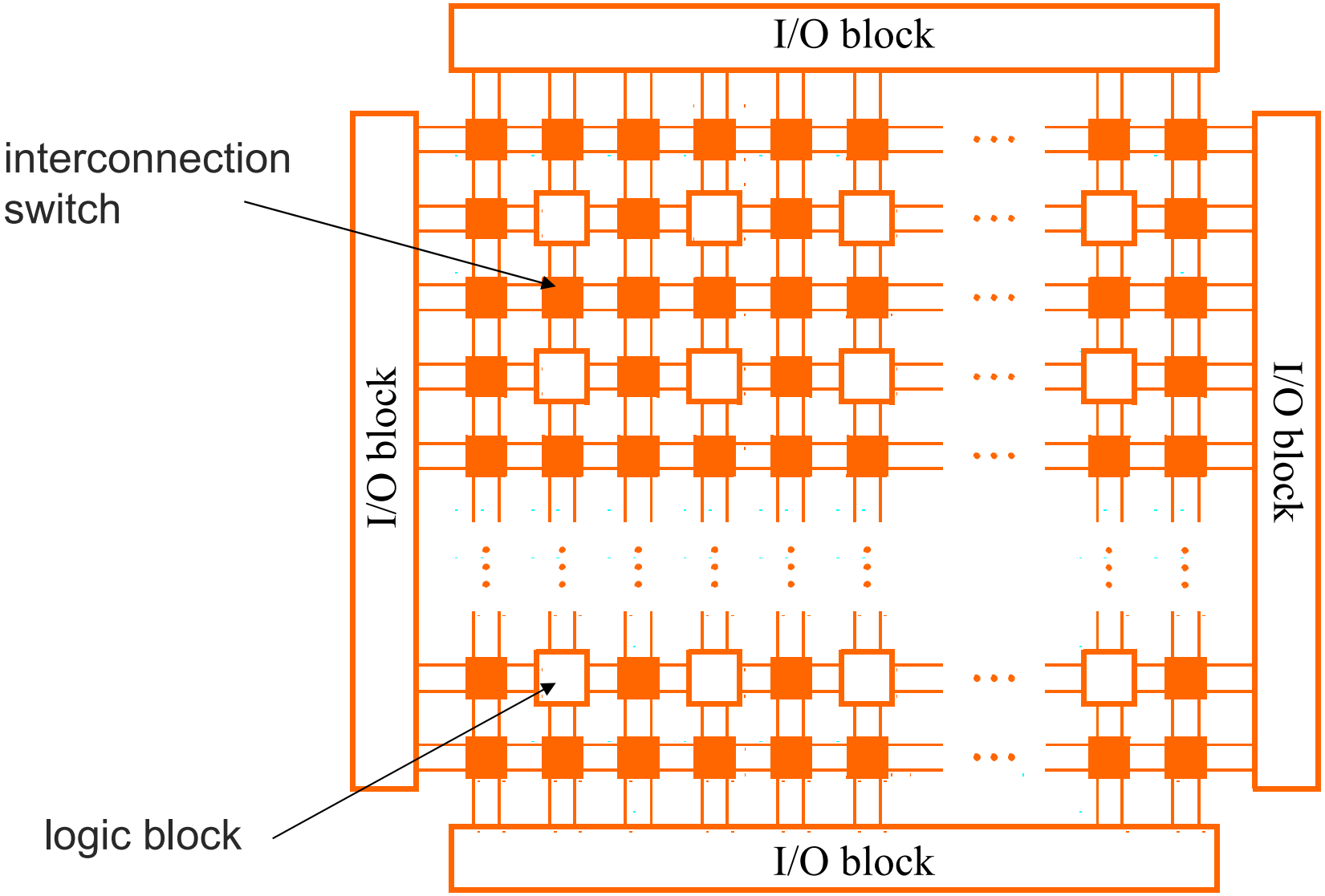
Structure of an FPGA



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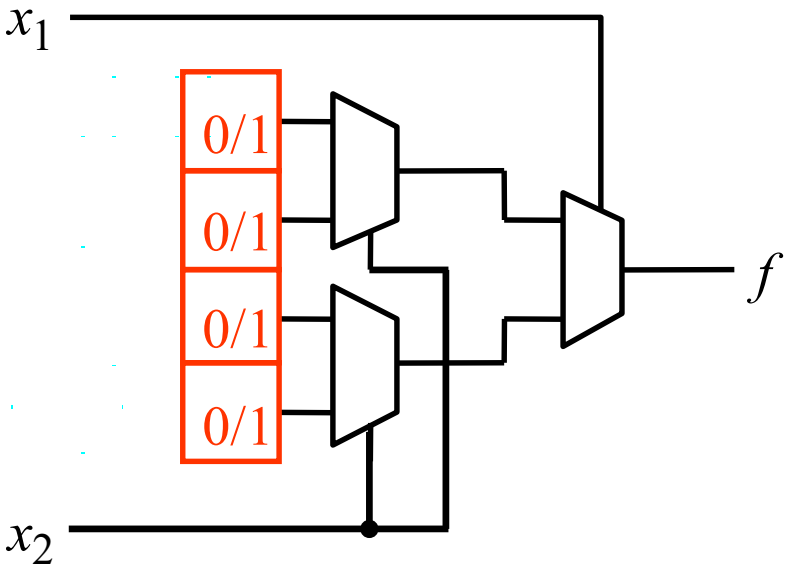
LUTs

- Logic blocks are implemented using a lookup table (LUT)
  - Small number of inputs, one output
  - Contains storage cells that can be loaded with the desired values
  - A 2 input LUT uses 3 MUXes to implement any desired function of 2 variables
    - Shannon's expansion at work!



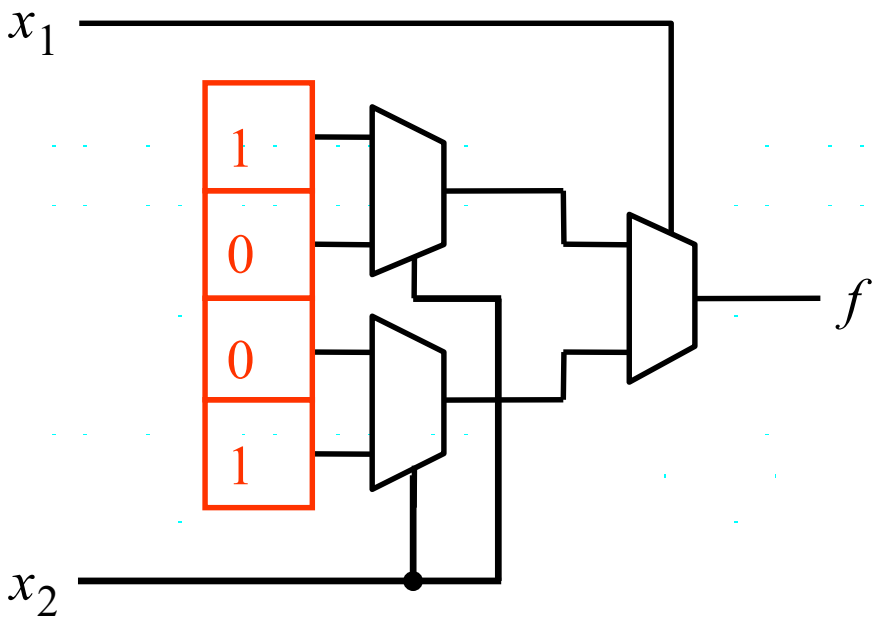
Example 2 Input LUT

x_1	x_2	f
0	0	1
0	1	0
1	0	0
1	1	1

$f = x_1'x_2' + x_1x_2$, or using Shannon's expansion:

$f = x_1'(x_2') + x_1(x_2)$

$= x_1'(x_2'(1) + x_2(0)) + x_1(x_2'(0) + x_2(1))$



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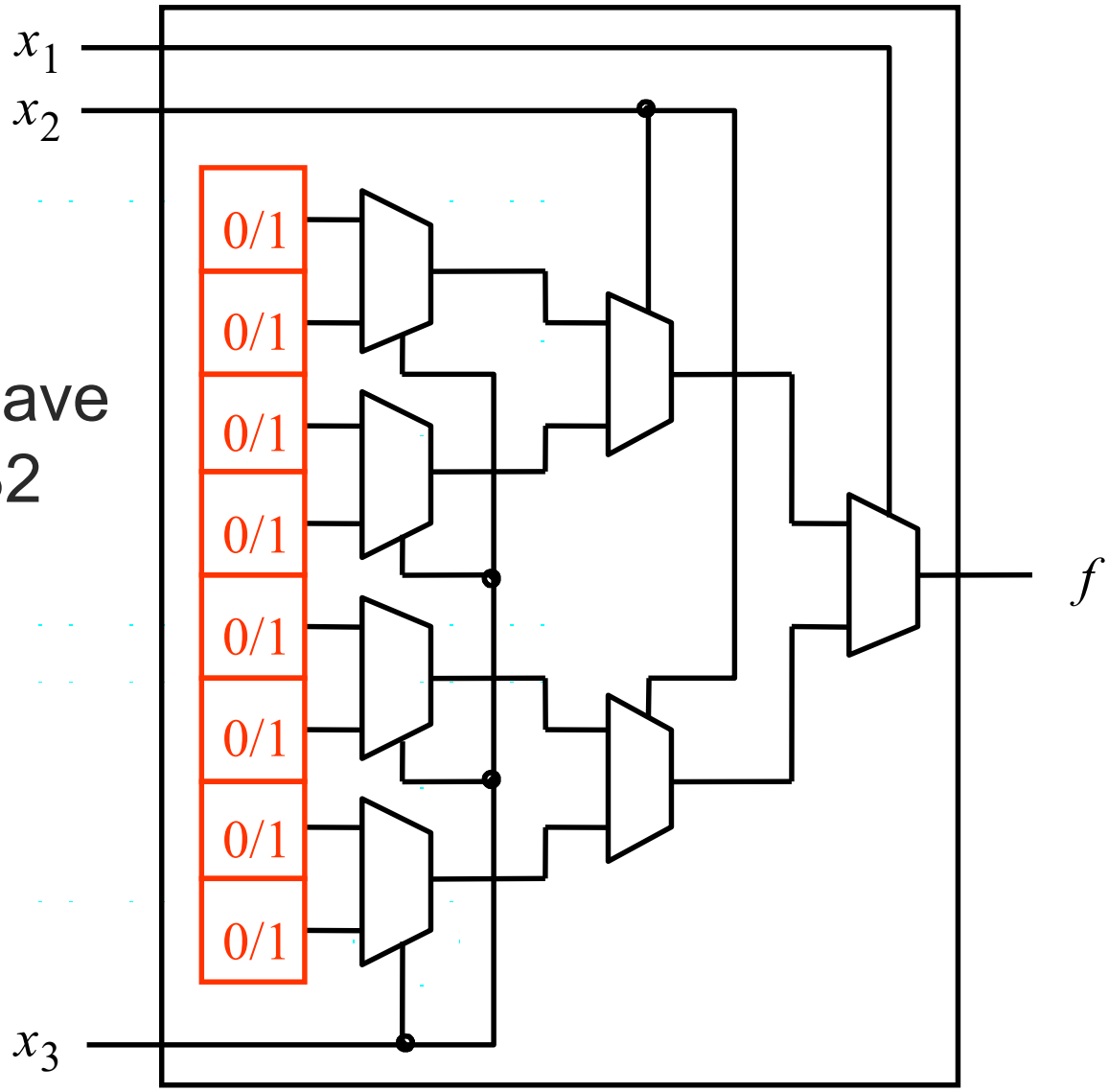
3 Input LUT

- 7 2x1 MUXes and 8 storage cells are required
- Commercial LUTs have 4-5 inputs, and 16-32 storage cells



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Programming an FPGA

- ISP method is used
- LUTs contain volatile storage cells
  - None of the other PLD technologies are volatile
  - FPGA storage cells are loaded via a PROM when power is first applied
- The UP2 Education Board by Altera contains a JTAG port, a MAX 7000 CPLD, and a FLEX 10K FPGA
  - The MAX 7000 CPLD chip is EPM7128SLC84-7
  - EPM7 → MAX 7000 family; 128 macrocells; LC84 → 84 pin PLCC package; 7 → speed grade

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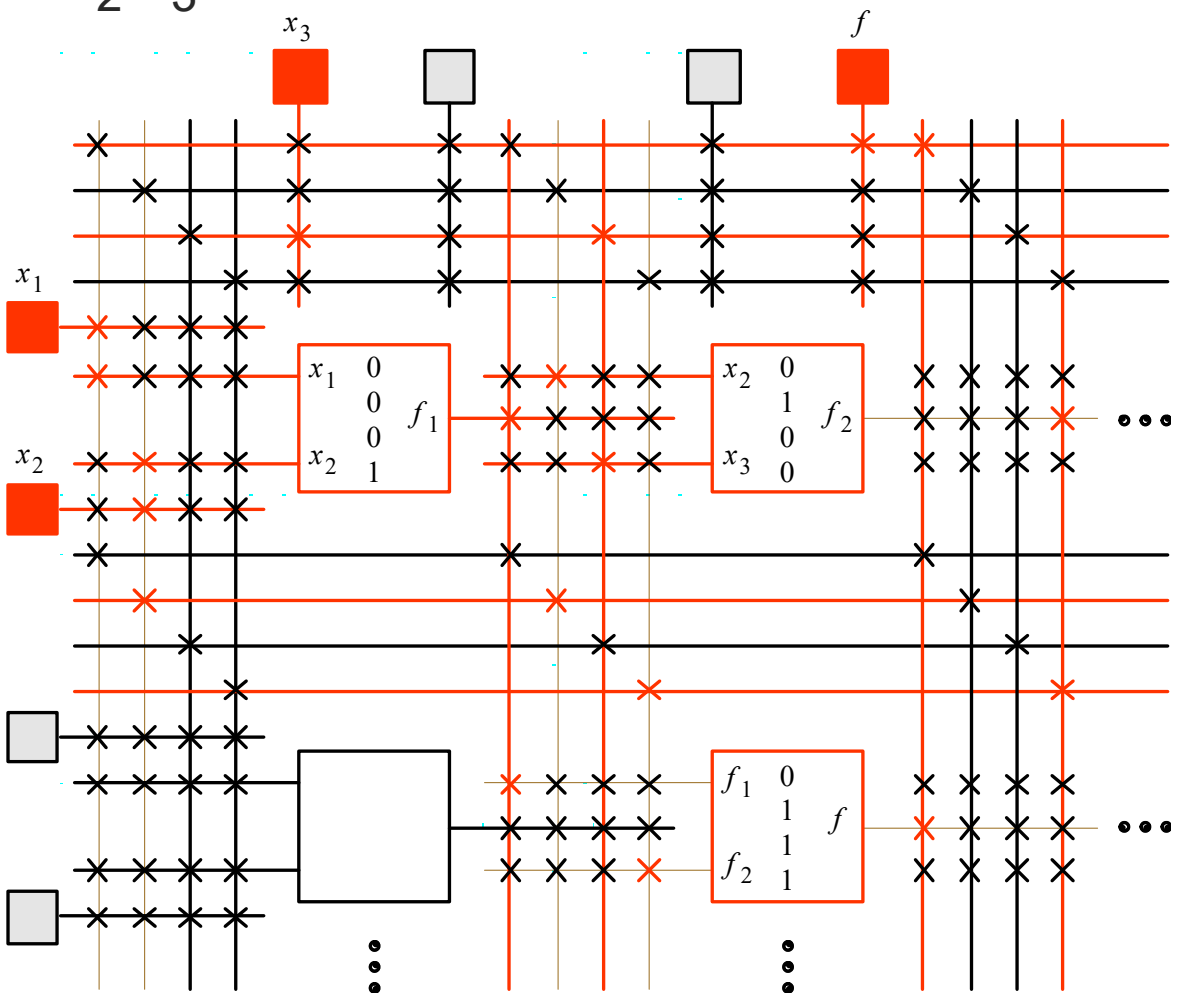
Example FPGA

- Use an FPGA with 2 input LUTS to implement the function $f = x_1x_2 + x_2'x_3$
  - $f_1 = x_1x_2$
  - $f_2 = x_2'x_3$
  - $f = f_1 + f_2$



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Another Example FPGA

- Use an FPGA with 2 input LUTS to implement the function $f = x_1x_3x_6' + x_1x_4x_5x_6' + x_2x_3x_7 + x_2x_4x_5x_7$
  - Fan-in of expression is too large for FPGA (this was simple to do in a CPLD)
  - Factor f to get sub-expressions with max fan-in = 2
    - $f = x_1x_6'(x_3 + x_4x_5) + x_2x_7(x_3 + x_4x_5)$
      $= (x_1x_6' + x_2x_7)(x_3 + x_4x_5)$
  - Could use Shannon's expansion instead
    - Goal is to build expressions out of 2-input LUTs

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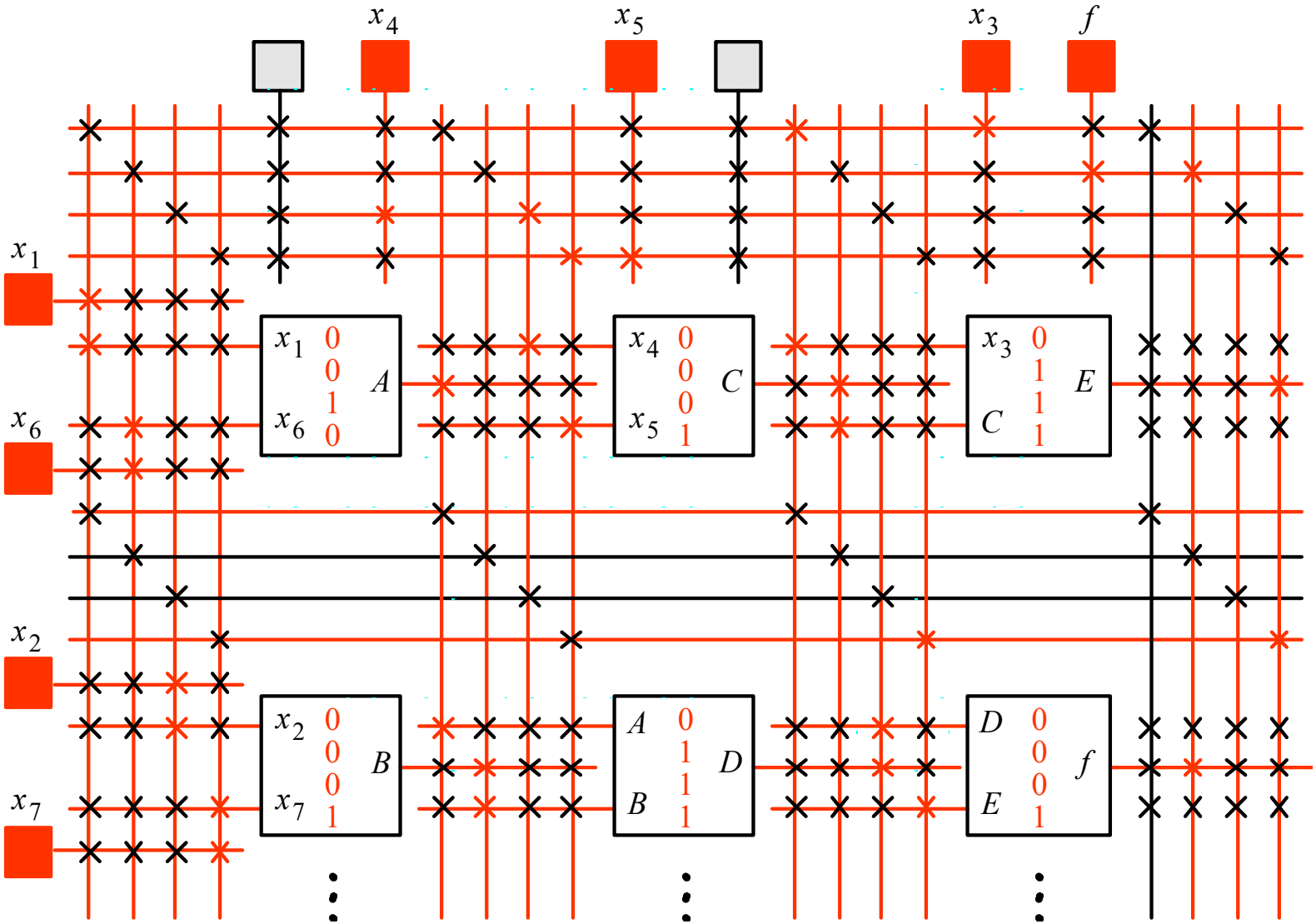
FPGA Implementation

- $f = (x_1x_6' + x_2x_7)(x_3 + x_4x_5)$



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Custom Chips

- PLDs are limited by number of programmable switches
  - Consume space
  - Reduce speed
- Custom chips are created from scratch
  - Expensive → used when high speed is required, volume sales are expected, and chip size is small but with high density of gates
  - ASICs (Application Specific Integrated Circuits) are custom chips that use a standard cell layout to reduce design costs

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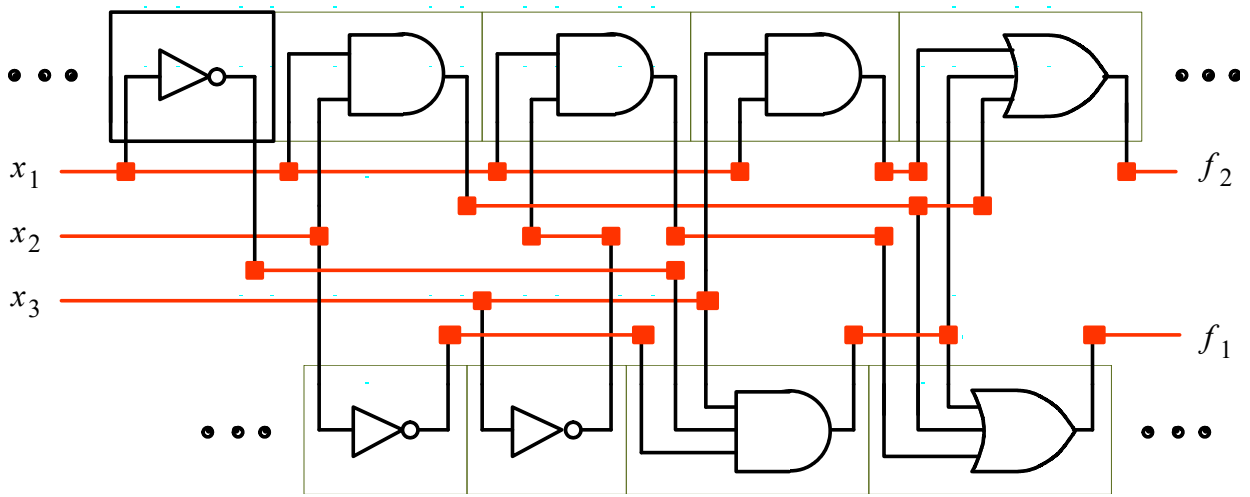
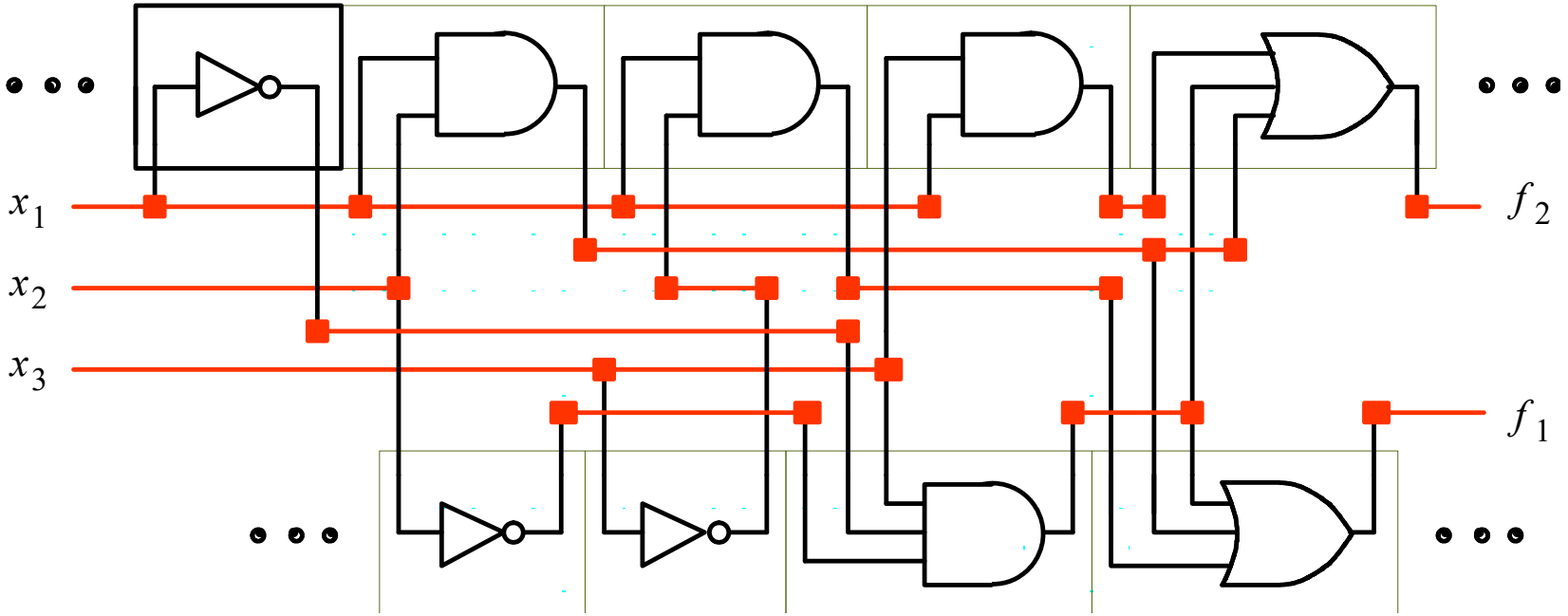
Standard Cells

- Rows of logic gates can be connected by wires in the *routing channels*
  - Designers (via CAD tools) select prefab gates from a library and place them in rows
  - Interconnections are made by wires in routing channels
    - Multiple layers may be used to avoid short circuiting
    - A hard-wired connection between layers is called a *via*



Example: Standard Cells

- $f_1 = x_1x_2 + x_1'x_2'x_3 + x_1x_3'$
- $f_2 = x_1x_2 + x_1'x_2'x_3 + x_1x_3$



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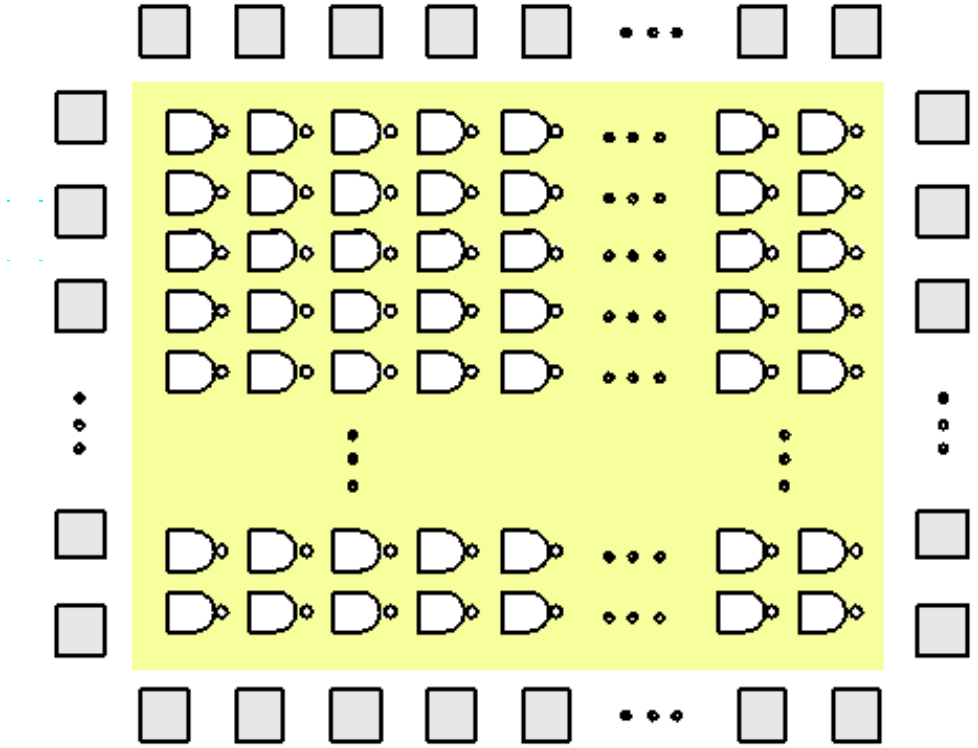
Sea of Gates Gate Array

- A Sea of Gates gate array is just like a standard cell except all gates are of the same type
  - Interconnections are run in channels and use multiple layers
  - Cheaper to manufacture due to regularity



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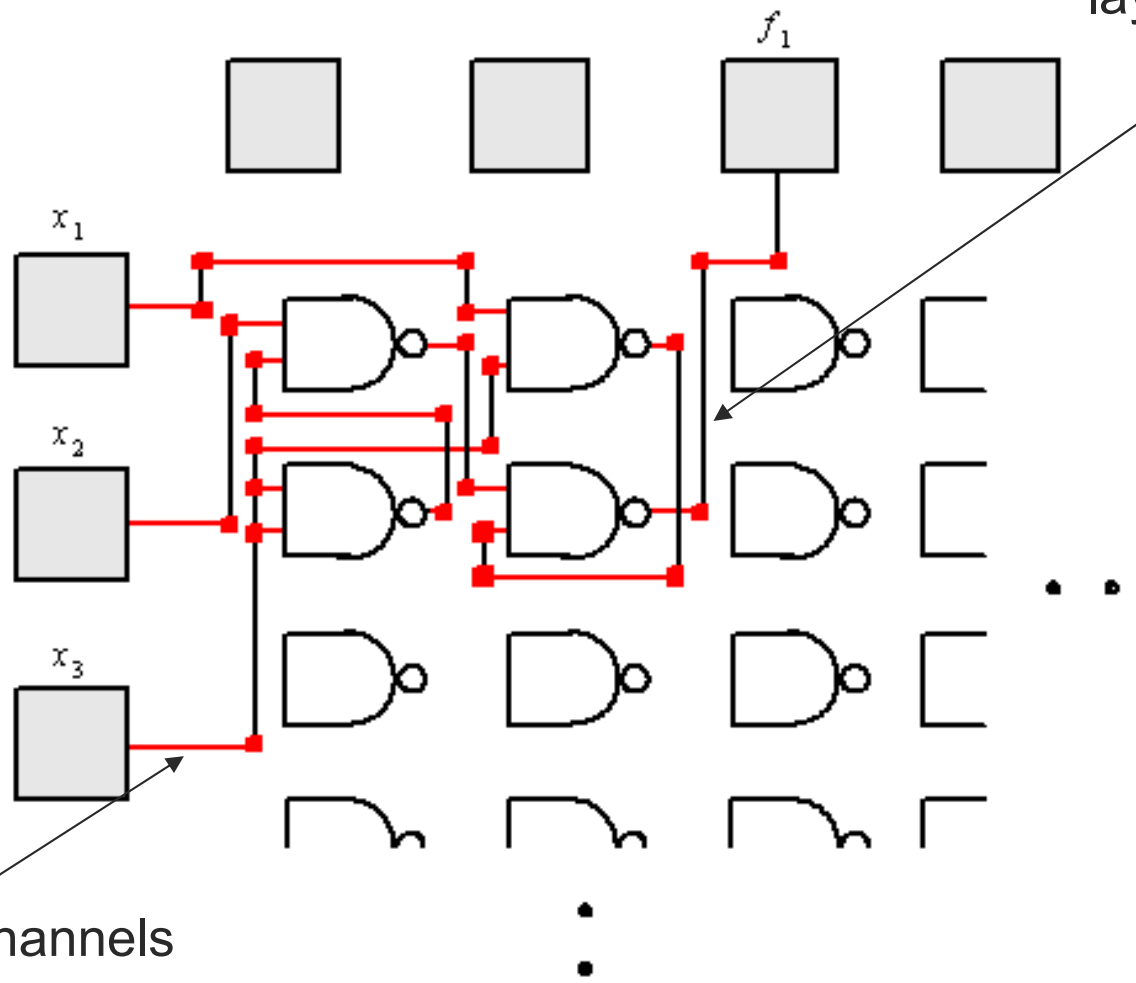
Example: Sea of Gates

- $f_1 = x_2x_3' + x_1x_3$



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Digital Logic Technology Tradeoffs